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# Reliability Investigations of MOSFETs using RF Small Signal Characterization

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**Talha Chohan**

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*Vorsitzender:*
Prof. Dr. Stefan Mannsfeld
*Gutachter:*
Prof. Dr.-Ing. Thomas Mikolajick
*Gutachter:*
Prof. Dr. Jurriaan Schmitz

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*"Then which of the favours of your Lord will ye deny?."*

The Qur'an (Surah Ar-Rahman 55:13)

# *Abstract*

Modern technology needs and advancements have introduced various new concepts such as Internet-of-Things, electric automotive, and Artificial intelligence. The crux and dependency of all these technologies are connectivity and efficient computing. Both of these parameters translate into fast signal processing which is analogous to the speed of a transistor. Furthermore, with increased human and machine interaction, more and more sensor technologies are integrated within the computing process. This implies an increased activity in the electronics domain of analog and RF design and performance. For such high frequency and high-power applications, III-V semiconductors have widely been used. However, due to aggressive scaling and development of various device concepts, Silicon devices have emerged as a cost-effective and good performance solution for such diverse applications. As these silicon devices are pushed towards higher performance, there is a continuous need to improve fabrication, power efficiency, variability, and reliability. Often, a direct trade-off of higher performance is observed in the reliability of semiconductor devices. Reliability characteristics and ensuring the specified functionality over the entire device/circuit lifetime are driven through various assumptions and acceleration-based methodologies. The acceleration-based methodologies are the adequate time-saving solution for the lifetime's extrapolation but come with uncertainty in accuracy. Thus, the efforts to improve the accuracy of reliability characterization methodologies run in parallel. The work presented in this dissertation is also an effort to serve the purpose mentioned above by exploring reliability effects in the high-frequency domain. This study highlights two goals that can be achieved by incorporating high-frequency characterization into the reliability characteristics. The first one is assessing high-frequency performance throughout the device's lifetime to facilitate an accurate description of device/circuit functionality for high-frequency applications. Secondly, to explore the potential of high-frequency characterization as the means of scanning reliability effects within devices.

In this work, high-frequency transistors are used for performance and reliability characterization. S-parameters are measured as a high-frequency device's response and mapped onto a small-signal model to analyze different components of a fully depleted silicon-on-insulator MOSFET. The self-heating assessment is done for various device geometries using the RF-conductance-based method. Thermal resistance, which serves as an indicator of self-heating, is modeled as a function of device layout parameters. The internal device temperatures are computed as a prerequisite for investigating temperature-dependent degradation mechanisms based on the thermal resistance model. The studied devices are then subjected to two important DC stress patterns, i.e., Bias temperature instability stress and hot carrier stress. The hot carrier stress, which inherently suffers from the self-heating effect, resulted in the transistor's geometry-dependent magnitudes of hot carrier degradation. It is shown that the incorporation of the thermal resistance model is mandatory for the investigation of hot carrier degradation. S-parameter characterization is performed before and after stress to investigate the impact on the high-frequency small-signal model components. It was found that for the bias temperature instability stress, the changes in small-signal model components are directly correlated with the threshold voltage shift and transconductance. The property of direct translation of small-signal parameter degradation to DC

parameter degradation is used to develop a new S-parameter-based bias temperature instability characterization methodology. In the case of hot carrier stress, most of the small-signal model components can be explained with the shift in DC metrics except for the gate-related small-signal capacitances. The changes in gate-related small-signal capacitances after hot carrier stress reveals a distinct signature due to local change of flat-band voltage. The measured effects of gate-related small-signal capacitances post-stress are validated through transient physics-based simulations in Sentaurus TCAD. Based on measured and simulated responses of small-signal capacitances and resistances, an empirical-based deconvolution technique is demonstrated to distinguish the individual contribution of hot carrier and bias temperature instability stress.

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# Symbols

| Symbol | Description | Unit |
|---|---|---|
| $I$ | current | A |
| $V$ | voltage | V |
| $Z_{\mathrm{o}}$ | characteristic impedance | Ω |
| $I_{\mathrm{t}}$ | incident current | A |
| $I_{\mathrm{r}}$ | reflected current | A |
| $V_{\mathrm{t}}$ | incident voltage | V |
| $V_{\mathrm{r}}$ | reflected voltage | V |
| $P_{\mathrm{in}}$ | input power | W |
| $f$ | frequency | Hz |
| $R_{\mathrm{g}}$ | gate resistance | Ω |
| $R_{\mathrm{s}}$ | source resistance | Ω |
| $R_{\mathrm{d}}$ | drain resistance | Ω |
| $R_{\mathrm{co}}$ | contact resistance | Ω |
| $R_{\mathrm{r,s/d}}$ | raised source/drain resistance | Ω |
| $R_{\mathrm{e,s/d}}$ | source/drain extension resistance | Ω |
| $R_{\mathrm{ac}}$ | accumulation resistance | Ω |
| $R_{\mathrm{ch}}$ | channel resistance | Ω |
| $C_{\mathrm{ox}}$ | oxide capacitance | F |
| $C_{\mathrm{gs}}$ | gate-source capacitance | F |
| $C_{\mathrm{gd}}$ | gate-drain capacitance | F |
| $C_{\mathrm{gb}}$ | gate-back-gate capacitance | F |
| $C_{\mathrm{gg}}$ | total gate capacitance | F |
| $C_{\mathrm{sd}}$ | drain-source capacitance | F |
| $C_{\mathrm{bd}}$ | drain-back-gate capacitance | F |
| $g_m$ | transconductance | S |
| $g_{m,\mathrm{max}}$ | peak transconductance | S |
| $g_{\mathrm{ds}}$ | output-conductance | S |
| $f_{\mathrm{t}}$ | transit-frequency | Hz |
| $f_{\mathrm{max}}$ | maximum oscillation frequency | Hz |
| $I_{\mathrm{g}}$ | gate current | A |
| $I_{\mathrm{d}}$ | drain current | A |
| $I_{\mathrm{d,lin}}$ | linear drain current | A |
| $I_{\mathrm{d,sat}}$ | saturation drain current | A |
| $I_{\mathrm{s}}$ | source current | A |
| $l_{\mathrm{g}}$ | gate length | m |
| $w_{\mathrm{g}}$ | gate width | m |
| $w_{\mathrm{f}}$ | width per finger | m |
| $nf$ | number of fingers | |
| $c$ | ratio of source/drain contact area to source and drain region area | |
| $V_{\mathrm{ds}}$ | drain to source voltage | V |

| Symbol | Description | Unit |
|---|---|---|
| $V_{\mathrm{d}}$ | drain voltage | V |
| $V_{\mathrm{gs}}$ | gate to source voltage | V |
| $V_{\mathrm{s}}$ | source voltage | V |
| $V_{\mathrm{stress}}$ | stress voltage | V |
| $V_{\mathrm{th}}$ | threshold voltage | V |
| $V_{\mathrm{th,lin}}$ | linear $V_{\mathrm{th}}$ | V |
| $V_{\mathrm{th,sat}}$ | saturation $V_{\mathrm{th}}$ | V |
| $Q_{\mathrm{g}}$ | gate charge | C |
| $R_{th}$ | normalized thermal resistance | $\mathrm{KmW}^{-1}$ |
| $G_{th}$ | normalized thermal conductance | $\mathrm{WK}^{-1}\mathrm{m}^{-1}$ |
| $C_{th}$ | thermal capacitance | $\mathrm{JK}^{-1}$ |
| $Z_{th}$ | thermal impedance | |
| $\tau_{th}$ | thermal time constant | s |
| $T$ | temperature | K |
| $T_{device}$ | internal device temperature | K |
| $k_B$ | Boltzmann constant | $\mathrm{eVK}^{-1}$ |
| $g_{\mathrm{ds,HF}}$ | $g_{\mathrm{ds}}$ at high-frequency | S |
| $g_{\mathrm{ds,LF}}$ | $g_{\mathrm{ds}}$ at low-frequency | S |
| $f_{th}$ | thermal characteristic frequency | Hz |
| $V_{\mathrm{ZTC}}$ | gate-bias at the ZTC point | V |
| $t_{\mathrm{Si}}$ | SOI thickness | m |
| $t_{\mathrm{BOX}}$ | BOX thickness | m |
| $f_{\mathrm{spac}}$ | spacing between fingers | m |
| $G_{th,lg}$ | thermal conductance factor for gate length | $\mathrm{WK}^{-1}\mathrm{m}^{-2}$ |
| $G_{th,wf}$ | thermal conductance factor for gate width | $\mathrm{WK}^{-1}$ |
| $G_{th,nf}$ | thermal conductance factor for number of fingers | $\mathrm{WK}^{-1}\mathrm{m}^{-1}$ |
| $G_{th,fspac}$ | thermal conductance factor for fingers spacing | $\mathrm{WK}^{-1}\mathrm{m}^{-2}$ |
| $G_{th,c}$ | thermal conductance factor for contacts | $\mathrm{WK}^{-1}\mathrm{m}^{-2}$ |
| $w_{\mathrm{eff}}$ | total effective width | m |
| $w_{\mathrm{rx}}$ | individual active area island width | m |
| $\mu_{\mathrm{eff}}$ | effective mobility | $\mathrm{cm}^2/\mathrm{Vs}$ |
| $t$ | time | s |
| $V_{\mathrm{md}}$ | small signal voltage at drain | V |
| $V_{\mathrm{ms}}$ | small signal voltage at source | V |
| $v_{\mathrm{ac}}$ | small signal potential | V |
| $l_{\mathrm{eff}}$ | effective channel length | m |
| $E_{\mathrm{g}}$ | energy bandgap | eV |
| $E_a$ | activation energy | eV |
| $\phi_{\mathrm{F}}$ | fermi potential | eV |
| $Q_{\mathrm{dep}}$ | depletion charge | $\mathrm{Ccm}^{-2}$ |
| $v_{\mathrm{sat}}$ | saturation velocity | $\mathrm{cm\,s}^{-1}$ |

# Acronyms

| Acronyms | Description |
|---|---|
| AC | alternating current |
| BEOL | back-end-of-line |
| BJT | bipolar junction transistor |
| BOX | buried-oxide |
| BTI | bias temperature instability |
| C-V | capacitance-voltage |
| DC | direct current |
| DIBL | drain induced barrier lowering |
| DUT | device under test |
| DUT_D | structure with shared drain |
| DUT_N | structure with no shared S/D |
| DUT_S | structure with shared source |
| ETSOI | extremely-thin SOI |
| FDSOI | fully-depleted silicon on insulator |
| FEOL | front-end-of-line |
| FinFET | fin-field-effect transistor |
| FC | fixed charges |
| FoMs | figures of merit |
| GIDL | gate-induced drain leakage |
| GSG | ground-signal-ground |
| HC | hot-carrier |
| HCD | hot-carrier degradation |
| HCI | hot-carrier injection |
| HVT | high $V_{th}$ |
| IF | intermediate frequency |
| ITC | interface trap charges |
| LRRM | line-reflect-reflect-match |
| LVT | low $V_{th}$ |
| MOL | middle-of-line |
| MOSFET | metal oxide semiconductor field effect transistor |
| MP | multi-particle |
| NBTI | negative bias temperature instability |
| $N_{it}$ | density of interface states |
| n-MOSFET | N-type metal-oxide-semiconductor field-effect transistor |
| NREP | number of repetitions along gate poly line |
| NRX | number of active area slices |
| OTF | on-the-fly |
| P | permanent component |
| PBTI | positive bias temperature instability |
| PCell | parameterized cell |

| Acronyms | Description |
|---|---|
| PDSOI | partially depleted silicon on insulator |
| p-MOSFET | P-type metal-oxide-semiconductor field-effect transistor |
| R | recoverable component |
| RDF | random dopant fluctuation |
| RF | radio frequency |
| RVT | regular $V_{\text{th}}$ |
| S-parameter | scattering parameter |
| SILC | stress-induced leakage current |
| SLVT | super-low $V_{\text{th}}$ |
| SMU | source measure unit |
| SOI | silicon on insulator |
| SOLT | short-open-load-through |
| SOTB | silicon on thin BOX |
| **S**OTF-BTI | S-parameter based OTF BTI characterization technique |
| SP | single-particle |
| SRAM | static random access memory |
| SS | subthreshold swing |
| STI | shallow trench isolation |
| TCAD | technology computer-aided design |
| TDDB | time-dependent dielectric breakdown |
| TDDS | time-dependent defect spectroscopy |
| TRL | through-reflect-line |
| U | Mason's gain |
| UTB | ultra-thin body |
| UTBB | ultra-thin body and BOX |
| UTBOX | ultra-thin BOX |
| UTSOI | ultra-thin SOI |
| VNA | vector network analyzer |
| Y-parameter | admittance parameter |
| Z-parameter | impedance parameter |
| ZTC | zero temperature coefficient |

# Chapter 1

# Introduction

Recently, with the rapid advancement in wireless technologies, there has been growing interest in nano-scale devices' performance and reliability characterization. Silicon devices have emerged uninterruptedly into the high-frequency application domain due to their high performance, low cost, and scalability. The demand for circuit performance and efficiency has been conventionally served by aggressive scaling and increased packaging density. These miniaturization trends address the performance needs but come at the cost of short channel effects, increased leakage through dielectrics, and tighter reliability constraints. Several strategies have been introduced to cope with the scaling challenges, such as silicon on insulator (SOI) technologies, new materials like high-k gate dielectrics, strain engineering, and novel device concepts and architectures such as fully-depleted silicon on insulator (FDSOI) technologies. FDSOI with thin buried-oxide (BOX) offers low substrate parasitics, good electrostatic control of short channel effects, and variable threshold voltage tuning functionality, enabling high-performance analog and radio frequency (RF) applications [1]–[4]. With the wide recognition and applications of the FDSOI technology, these devices' reliability study plays a vital role in gaining a deeper understanding and developing them further for future technology nodes. Physical mechanisms governing the operation and reliability of ultra-scaled devices have evolved and need closer attention. So far, the direct current (DC) reliability methods extensively applied assuming quasi-static approximation, which requires guard bands for most usage cases. However, as the technology reaches scaling limits, the devices are pushed for higher performance resulting in tighter guard bands.

Multi-finger and multi-cell devices are widely used for RF and analog applications to achieve high power, reduce the physical size, lower gate resistance, and improve device matching. A simple logic device's reliability investigations should be extended to accommodate multi-finger structures having different layout variations addressing the needs of high-frequency and high power applications. With the increasing interest in RF reliability, multi-finger devices are now frequently used for reliability characterization, further narrowing the gap between reliability models and real usage cases.

Thus along with the efforts of improving reliability and performance, it is also becoming essential to characterize the aging of devices not only for conventional DC operation but also in dynamic and high-frequency operation. Two of the dominant degradation mechanisms in metal oxide semiconductor field effect transistors (MOSFETs) are bias temperature instability (BTI) and hot-carrier degradation (HCD). Scattering parameter (S-parameter) measurements serve as the tool for assessing high-frequency response. Study of the degradation in terms of S-parameter characterization enabled unveiling and monitoring the changes in

high-frequency parameters, which were not visible under conventional DC characterization methodology. The assessment of degradation effects under the transistor's dynamic and high-frequency operation is necessary for comprehensive understanding and modeling small-signal behavior due to various stress modes. S-parameter characterization has also eased the understanding of degradation mechanisms and underlying physical perturbation effects due to various stress conditions. It is worthwhile to explore the capabilities of S-parameters as a characterization tool to complement reliability investigations.

The focus of this dissertation is broadly classified in two domains, i.e., to diagnose the impact of key degradation mechanism on the small-signal behavior of a MOSFET and to explore the potential of S-parameters as a reliability analysis tool. It is worth mentioning that the presented experimental data is readily shown on an arbitrary scale (a.u). It is often challenging to draw quantitative comparisons using an arbitrary scale. However, for this study, arbitrary scales are chosen to ensure that the qualitative/relative conclusions are not hampered and reflect the true nature of the results. The content presented in this document is organized as follows: Beyond this short introduction of the topic, Chapter 2 presents a brief introduction to the fundamental concepts involved within the scope of this work. Starting from basic scaling challenges to understand the operation of devices under investigation followed by an account of various degradation mechanisms and reliability concerns. Chapter 3 presents the methodology used to measure S-parameters and extraction of small signal characteristics. In the subsequent chapter, these extracted small-signal parameters are frequently discussed under the influence of different stresses. Before analyzing of any stress impact, it is important to account for the self-heating effects as the degradation mechanisms under investigation strongly depend on the temperature. Chapter 4 presents the characterization scheme and results of extracted thermal performance. Chapter 5 mainly discusses the impact of BTI stress on small-signal performance and model components. In the same chapter, a small signal parameter is identified, which then can be used to develop an on-the-fly BTI characterization technique. The analysis of hot-carrier (HC) stress on DC and small-signal parameters is discussed in Chapter 6. The correlation between self-heating and the resultant impact on the degradation mechanism is analyzed. Based on the observed unique degradation signature, a de-convolution technique for HCD and BTI components of a degraded device is demonstrated in Chapter 7. Finally, the conclusions and recommendations for future work are summarized in Chapter 8.

# Chapter 2

# Fundamentals

This chapter reviews the basic concepts related to this dissertation and the work presented in the following chapters. The first section of this chapter starts with an introduction of MOSFET scaling and a technological overview of the used FDSOI transistors for characterization. The subsequent sections discuss various reliability challenges of MOSFET, including degradation mechanisms in advanced semiconductor devices and a focused account on the broad nature of reliability in terms of RF.

## 2.1 MOSFETs Scaling Trends and Challenges

Since the invention of three-terminal active devices, semiconductor and transistor technology have experienced tremendous evolution. The transition from very first vacuum tubes into solid-state electronics happened almost over seven decades ago with demonstration of point-contact transistor in 1947 by Bardeen and Brattain [5]. After the design improvement by Shockley [6], the bipolar junction transistor (BJT) was in widespread usage in the 1950s. The concept of Field-Effect-Transistor was patented by Edgar [7] in 1928, well before the BJT. However, Edgar could not practically execute the idea of filed-effect due to surface states. The breakthrough in surface passivation due to thermally grown silicon-dioxide by Atalla, Tannenbaum, and Scheibner [8] in 1959, led to the demonstration of the first p-channel silicon MOSFET in 1960 by M M. Atalla and Dawon Kahng [9]. Although the idea of a field-effect transistor was envisioned at the time of vacuum tubes, it is not until the 1970s that MOSFETs were deployed largely in electronics. The slower speed and relatively inferior performance compared to well-established competitor BJT refrain the development of MOSFET until the quest for low energy footprint [9], [10]. The emergence of the computer industry and integrated circuits embark MOSFET on the journey of miniaturization and showcase its immense potential. In 1965, Gordon E. Moore predicted that the density of components on a chip and performance doubles each year [11], and later in 1975, he revisited the renowned Moore's Law by relaxing the timeline to 2 years [12], [13]. The term doubling complexity inherits better performance, scaled-down feature size, complex fabrication process, and reduced cost per transistor. In recent years with a slow-down in scaling trends, Moore's law demise or alive nature is often a point of discussion among the scientific community [14]–[17].

The miniaturization journey progressed throughout the years at an ample pace; however, the efforts, research, and hurdles cannot be underestimated. The lithographic way of scaling down to small feature size benefited the semiconductor technology in terms of performance, cost, and footprint until the early 2000s when the technology node began to shrink beyond sub 100 nm. At such dimensions, further scaling of gate length ($l_g$) poses several challenges [18]–[21] which includes

increased leakage currents through gate dielectrics, low carrier mobility due to high doping level and interface effects, degradation of subthreshold swing (SS), drain induced barrier lowering (DIBL) due to proximity of source and drain regions, and increased reliability concerns [22]–[24] caused by high electric fields. New materials and various device designs are deployed to counter these scaling and short channel effects. As with the reduction of $l_g$, the gate oxide thickness had to be reduced in proportion, leading to tunneling currents through the gate dielectric. High-k dielectric material with metal gate [25], [26] is introduced to gain better electrostatic control of the channel and reduce gate leakage. For improving the carrier mobility, strain engineering [27], [28], and device architectures enable low doped channel region to be deployed. SOI technology shows a promising approach for better electrostatic control, reduced substrate parasitics, and diminution of leakage currents [29]–[32]. Other technological solutions include halo implants [22], [33], shallow drain/source extensions [34], [35], beyond silicon channel materials [36]–[39] and alternative device structures [40]–[43].

Another phenomenon in addition to the short channel effects is the variability of MOSFET electrical characteristics, which is caused by the variation in the number of dopants in the channel (also known as random dopant fluctuation (RDF)) [44], [45]. On average, there exist approximately 100 dopant atoms in a channel of MOSFET fabricated in 100 nm technology [46]. For advanced technology nodes, this is translated to few dopant atoms per device. Due to the inherent nature of the doping process, the resultant random placement of dopant atoms causes device to device variability. With the scaling of gate length, RDF poses a considerable amount of variability in threshold voltage ($V_{th}$) and on-state current, [45], [47] limiting the scalability and needs the circuit design to tolerate the variability [48]–[50].

### 2.1.1 Silicon on Insulator Technology

The introduction of an insulator (BOX) layer in the substrate, which separates the source and drain region from a bulk substrate, enables to overcome the barrier for further scaling of advanced technology node. Due to the central bulk region's isolation, better electrostatic control of the channel and reduction of short channel effects is achieved, thereby improving performance by increasing dynamic power efficiency [31], [51]. For high-frequency applications, the reduction of junction parasitic capacitances offers better RF characteristics. SOI technology also offers execution of similar fabrication processes as used for the conventional bulk technology while having an opportunity to reduce the number of fabrication steps as separate n-well and p-well formation is not required [31].

In SOI technology, two basic parameters i.e., SOI thickness ($t_{Si}$) and BOX thickness ($t_{BOX}$) serve as further knobs to influence the device characteristics. In terms of SOI thickness, partially depleted silicon on insulator (PDSOI) and FDSOI technologies were proposed having $t_{Si}$ larger and in the same order of magnitude as the depletion region respectively. The doping concentration and $t_{Si}$ determines the channel depletion region depth. Having a $t_{Si}$ small enough to form a partially or fully depleted channel enables lowering of doping concentrations to improve carrier mobility and RDF. In PDSOI devices, due to partially depleted region, floating body effects and history effects are a few of concerns causing the fluctuation of electrical characteristics [52]–[55]. FDSOI solves the shortcomings of PDSOI floating body effects having $t_{Si}$ to cover the depleted region entirely [56]–[59]. In addition to $t_{Si}$, $t_{BOX}$ can be a further knob to control short channel effects, substrate coupling, enhanced thermal dissipation, and the possibility of

bottom-gate channel control. The respective structures can be classified into thick BOX and ultra-thin BOX, as shown in Fig. 2.1. Devices fabricated with ultra-thin BOX shows reduced short channel effects [20], [31], [59], [60] and potential for the back gate biasing for effective control of channel and adaptive $V_{th}$ for application-specific requirements [1], [4], [42], [61].

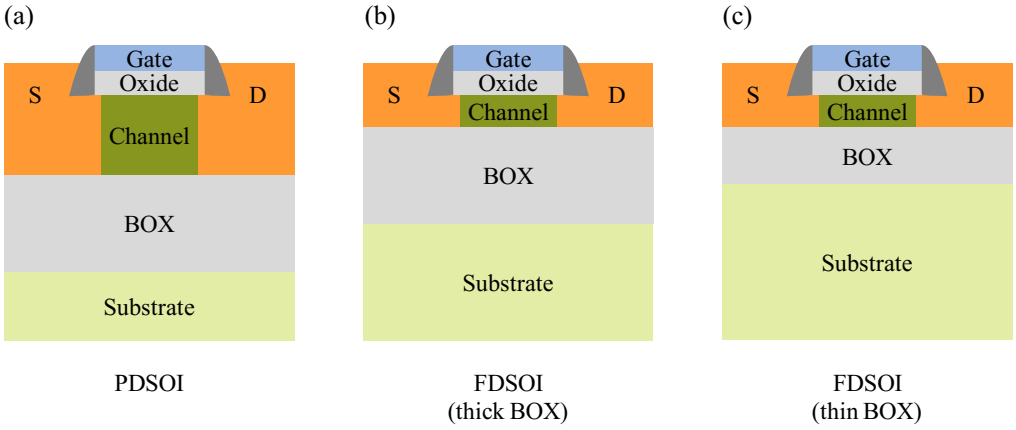


FIGURE 2.1: Cross section of (a) PDSOI, (b) FDSOI with thick BOX, (c) FDSOI with ultra-thin BOX MOSFET. In these structures $t_{Si}(a) > (t_{Si}(b) = t_{Si}(c))$ and smallest $t_{BOX}$ in (c).

### 2.1.2 FDSOI Technology

In the 1980s, the advantages of FDSOI technology started to gain attention over conventional bulk and PDSOI technology [62], [63]. With the progress of semiconductor technology, the process is adopted and deployed to obtain precise and ultra-scaled FDSOI technology nodes. Technologies such as FDSOI and fin-field-effect transistor (FinFET) have become the basis of scaling nowadays. FDSOI offers simple, cost-effective fabrication processes and uses almost 90% of conventional bulk processing technology [64]. In literature different terminologies are used to mention FDSOI devices and technologies based on their $t_{Si}$ and $t_{BOX}$ such as; ultra-thin body (UTB) , ultra-thin body and BOX (UTBB) [65]–[67] (same as UT2B [68], [69] and UTB$^2$ [70], [71] ),ultra-thin BOX (UTBOX) [72], [73], ultra-thin SOI (UTSOI) [74], [75], extremely-thin SOI (ETSOI) [76]–[78], and silicon on thin BOX (SOTB) [47], [79]. Later on, with advancement in technology node generations, FDSOI term with node size is generally mentioned [2], [3], [80]–[84]. The salient features of the FDSOI transistors are as follows:

- **Thin silicon layer**: FDSOI MOSFET features thin SOI film in order of approximately one-third of the gate length [85], [86] resulting in better channel control evident from improved SS [87]. SS value is closer to the theoretical minimum value of 60 mV/dec, translated into decrement in gate leakage currents [88]. The depth of the source and drain region is also reduced to the value of $t_{Si}$, which helps to reduce the short channel effect, especially DIBL [85], [86], [88], [89].

- **Substrate isolation with oxide**: BOX isolating the source/drain regions eliminates the leakage currents to the substrate reducing the static power consumption [90]. Thin SOI layer isolated with BOX beneath limits the depth of source and drain region, reducing the parasitic junction capacitances [85].

Reduction of parasitic capacitances benefits analog application where parasitics are detrimental to the high-frequency characteristics. In digital logic applications, reduced parasitic translates to switching with less energy improving the dynamic power consumption [85]. In conventional bulk technology, as neighboring devices are connected with a common substrate, the latch-up effect can occur in specific conditions, which is destructive in nature [91]. BOX isolation in FDSOI devices, along with shallow trench isolation (STI), eliminates the latch-up effect.

– **Undoped channel**: Isolation of substrate with BOX and thin SOI opportune eliminating doping obligation; thus getting rid of RDF. Better mobility and lower scattering are achieved from the undoped channel [92]. Elimination of RDF considerably reduces one of the key variability challenges in scaled devices [76], [89], [93]. Reduced variability translates into less difference between process corners (fast-fast and slow-slow). Very low gate-induced drain leakage (GIDL) is attributed to the undoped channel region [76], [94].

– $V_{th}$ **flavors**: FDSOI having thin BOX behaves almost like a double gate MOSFET where the channel region can be biased from back-gate underneath the BOX. An independent bias control of the back-gate can modulate the $V_{th}$ of the device. The option of modulated $V_{th}$ makes it adaptable to the low power and high-performance applications where higher $V_{th}$ (reduced static power consumption) and lower $V_{th}$ are needed, respectively. The desired flavor of $V_{th}$ is obtained by doping the well underneath the BOX, acting as a back-plane [1], [4]. A doped well underneath BOX acting as a ground plane reduces the substrate coupling effects [95]. Further control of $V_{th}$ is offered through active biasing of the back-plane, which can dynamically vary the device characteristics [3]. Depending on the polarity and doping concentration of the underneath well, GlobalFoundries 22FDX® technology offers super-low $V_{th}$ (SLVT), low $V_{th}$ (LVT), regular $V_{th}$ (RVT), and high $V_{th}$ (HVT) device flavors [1], [3]. Schematic of different $V_{th}$ flavor for N-type metal-oxide-semiconductor field-effect transistor (n-MOSFET) and P-type metal-oxide-semiconductor field-effect transistor (p-MOSFET) are shown in Fig. 2.2.

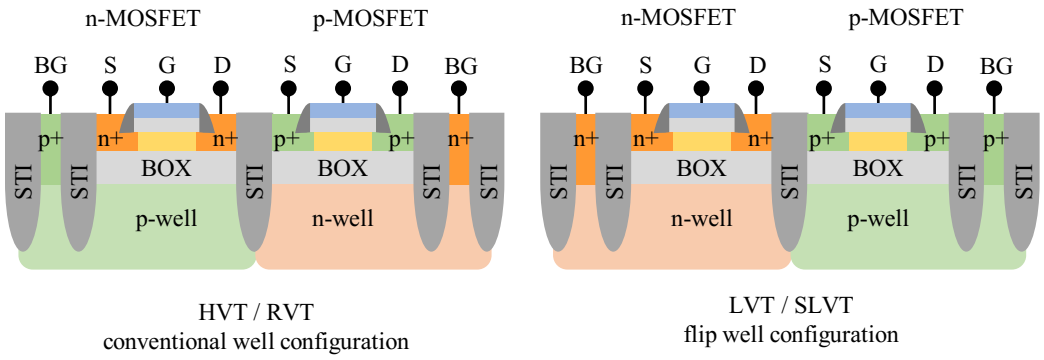


FIGURE 2.2: Cross-section of device construction for different $V_{th}$ flavor of FDSOI transistors with conventional well and flip well configuration.

The investigation and characterization reported in this dissertation are performed on FDSOI MOSFETs. High-performance SLVT flavor devices are mainly used. The details of test structure configuration are presented in Chapter 3.

## 2.2 Reliability of Semiconductor Devices

Reliability is a broad term to describe the specified functionality of a particular device, product, process, or system in the resolution of time. In this sense, the specific definition of reliability depends on which level it is being discussed. However, central to the whole reliability domain is the device level reliability, which can be scaled up to product or system level and serve as an indicator of process-level implications. In reliability, a certain margin for the drift of device characteristics is tolerated, and beyond that, device failure is considered. The time to reach this margin is known as device lifetime. Depending on the failure mechanism, a device may not exhibit complete failure and could still be operational (with degraded specifications). However, as the circuit/system is designed to tolerate a limited specification drift, it could result in circuit/system failure. The standard for the device lifetime is based on performance and safety requirements which are often attributed to the applications such as consumer electronics, mobile, automotive, military, and space grade [96]–[100].

A good enough prediction of a product lifetime requires an accurate description of reliability, scalable reliability models, and characterization methods that closely fit actual usage conditions. Several tools, including statistical algorithms and physical failure analysis, are readily used to examine and improve lifetime calculations. Understanding the failure mechanism involved in the degradation of a device is crucial for the extrapolation of a lifetime. The knowledge about these degradation mechanisms is achieved through characterization methods. As the actual device lifetime under normal operating conditions is in the range of several years, it is unrealistic to characterize the reliability under those normal boundary conditions. Usually, an accelerated degradation scheme is used in reliability characterization methods which stress the device beyond normal use conditions. The accelerated stress methods yield the degraded device parameters in reasonable time scales. The data acquired by applying several stress conditions for various boundary conditions can then be modeled to extrapolate the device characteristics to the normal usage. Therefore, an appropriate selection of stress conditions is essential to ensure that the device is experiencing a similar degradation mechanism as it should under normal usage. Several characterization methods exist to assess the device's reliability and subject to continuous development in order to achieve better precision and more in-depth information about various degradation phenomena.

Aggressive scaling of the semiconductor technology driven by performance factors comes with its reliability challenges. Following an ideal scaling trend to the next generation (doubling transistor density) under constant electric field assumption, the dynamic power reduces by 50%, gate delay is 30% decreased, and voltage scales down by 30% [101], [102]. The resultant impact is the same power density and dynamic power for the same die size. However, in reality, the supply voltages have not scaled down in an ideal manner due to the following reasons: (i) in order to achieve competitive frequency growth, the supply voltage is retained at relatively higher values (ii) by reducing the supply voltage the ratio of threshold to supply voltage increases leading to basic noise immunity issues in logic and static

random access memory (SRAM) designs. Reducing threshold voltage by gate oxide thickness scaling results in increased sub-threshold and gate current leakage. The gate oxide scaling translates into increased static power consumption and deteriorating gate oxide reliability, eventually leading to gate oxide breakdown [103], [104]. Increased transistor density per chip also scaled down the interconnect vias and lines cross-sectional area along with the introduction of metals with lower resistivity. In very large-scale integration technologies with multiple routing metal levels, this has resulted in electromigration reliability issues of interconnect metallization [105]–[109].

## 2.3 RF Reliability

Lately, the term RF reliability has gained traction and has been discussed in literature since the 1970s [110]–[117]. However, a concrete definition for such a topic is still not clear. For the first time, it is attempted to discuss the terminology itself and how different studies in literature consolidate with this term. The term RF reliability has been used in different contexts and specifies different reliability aspects. One thing common to all the studies is the inclusion of RF signals in either stress patterns or device characteristics. For a better perspective, the topic of RF reliability can be classified in two ways (i) based on stress sequence (ii) based on characterization methodology. Any of these or both of these can be done in the RF domain. From stress pattern perspective, the stress sequence can be DC, alternating current (AC) (also known as low-frequency stress), RF small signal, and RF large-signal stress. In terms of characterization, DC, RF small signal, and RF large signal analysis can be performed. Besides this classification, another level of complexity is added when circuits or systems are subject to testing instead of standalone discrete devices. In those cases, it is essential to differentiate between ruggedness tests and scalable reliability investigation. During the ruggedness test, the circuits/system are operated in an accelerated stress fashion but within certain constraints of operating conditions. Such probing aims to ascertain the long-term operation under specified operating conditions. Conventionally, in the reliability (DC and AC domain), it is often encouraged to build scalable reliability models which can be applied or scaled up to the circuit/system level. The approach for such reliability model development is associated with a better understanding of underlying degradation mechanisms. To date, there are very few attempts to build scalable reliability models applicable in the RF domain. In general practice, the existing reliability models based on DC and AC experiments are deployed to the RF domain using various simulation tools assuming quasi-static approximation.

The work done in this dissertation is an attempt in the direction of scalable RF reliability models by gaining more in-depth knowledge of the impact of different degradation mechanisms in RF small-signal performance. At the same time, RF measurements are explored to gain more insights or complement the reliability investigations. In the past, few studies demonstrated S-parameter measurements as a tool for reliability assessment [118]–[122]. It is also evident from the growing literature that the interest in RF reliability is increasing. The reasons for this rising interest are due to (i) increase in deployment of RF devices in modern electronics, predominantly due to advancements in communication technologies, internet of things, conversion of fossil fuel-based technologies into electric based (ii) with such broad application, the reliability constraints are getting tighter. The guard band

methodology is limiting the exploitation of modern semiconductor technology to its full potential.

## 2.4 MOSFET Degradation Mechanisms

Several degradation mechanisms exist in MOSFETs which can deteriorate their electrical characteristics. The root cause for virtually all of them can be traced back to the material's atoms, and molecules shifted from their designated positions under boundary conditions. Many of these degradation mechanisms are part of device intrinsic reliability. They are responsible for perturbation mainly in gate oxide and the channel region, namely: HCD, BTI, stress-induced leakage current (SILC), and time-dependent dielectric breakdown (TDDB). The work done in this dissertation is focused on the resultant effects of the former two and will be discussed in the next section. Besides these degradation mechanisms whose origin lies inside the intrinsic MOSFET, other degradation mechanisms such as electromigration, stress migration, and electrostatic discharge are also detrimental to the device reliability.

### 2.4.1 Hot Carrier Degradation

In broader terms, hot-carriers (HC) refer to the particles gaining high kinetic energy due to the acceleration under an applied electric field. The interaction of these HC with forbidden regions of a MOSFET result in the degradation of MOSFET's parameters such as $V_{\text{th}}$, drain current ($I_{\text{d}}$), SS, transconductance ($g_m$), and gate current ($I_{\text{g}}$) leakage. The phenomenon of HCD is known for several decades [123], and its physical origin has been studied extensively throughout the years [124], [125]. Semiconductor scaling also benefited in terms of developing the understanding of HCD physics [126]. Typically, HCD is linked to the generation of interface traps/states [127], [128] and oxide traps charging/discharging [128]–[130]. These electrically active traps can then get charged and cause a drift of the device parameters.

At the silicon and oxide interface, structural defects result in dangling bonds that can capture a carrier and get charged. These dangling bonds acted as the interface traps and passivated by incorporating hydrogen. These passive Si-H bonds are prone to rupturing by the interaction of carriers during MOSFET operation, resulting in electrically active dangling bonds. Being able to capture the carrier, the existing and generated interface traps distort the device's electrostatics. The dissociation energy of Si-H bonds is reported in the literature to be above 1.5 eV [131], [132]. While considering the bond dissociation kinetics, two factors on which this process can depend are the carrier's energy and the activation energy of bond dissociation. One of the earliest explanations of HCD originates from the concept of "lucky-electron model" [133]. According to the lucky-electron model, an electron needs to surmount a threshold potential barrier to trigger impact-ionization. An electron gaining sufficient energy (surmounting $Si/SiO_2$ potential barrier due to applied electric field) is redirected to $Si/SiO_2$ interface by phonon scattering end up breaking Si-H bond through impact ionization [133], [134]. Such bond-breaking kinetics conventionally named "hot carrier injection (HCI)". Later on, it was reported that the probability of interface trap generation depends on the starting energy distribution of hot carriers instead of the electric field [135], [136]. This led to the introduction of an empirical model by Rauch,

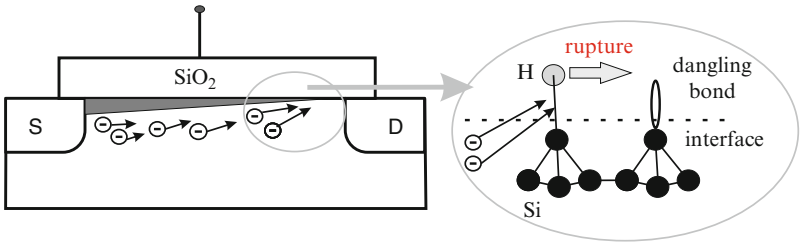


FIGURE 2.3: Illustration [145] of localized HCD mechanism in a MOSFET due to hot electron interaction with passivated Si-H bond and creation of interface traps. Resulted dangling bonds act as traps for electrons/holes and locally disturb the device electrostatics.

Guarin, and LaRosa called the energy-driven paradigm [137]. The energy-driven model demonstrated that the maximum electric field could not explain the HCD in technology nodes beyond 180 nm, and the carrier energy distribution must be introduced. The interface defect generation and impact ionization in this model is given by the integral of carrier energy distribution function and reaction cross-section [137], [138]. Recently, it is reported that the peak of the generated density of interface states ($N_{it}$) is neither directly related to the maximum electric field nor the average carrier density. Rather, an integral involving carrier energy distribution function, reaction cross-section, and carrier velocity accounting for primary and secondary generated carriers described the peak $N_{it}$ [126]. Hess model [139]–[141], energy-driven paradigm [137], [138], [142], Bravaix model [131], [143] , and carrier transport based model [144], [145] are some well known physics-based HCD models.

Rewinding to the physical mechanism of HCD, it can be assumed that if only HC with sufficient energy accelerated by high electric field can result in the interface trap generation (as shown in Fig. 2.3), then scaling down of supply voltage should suppress the HCD. In ultra-scaled devices with shorter gate lengths, the supply voltage is even less than 1 V, where it is unlikely for a carrier to become hot enough. However, HCD does not disappear with the technology scaling and is still one of the key reliability aspects in ultra-scaled devices [139]. This is due to the change of HCD kinetics and can be explained by the carrier exchange mechanism within the carrier packet/ensemble through various types of scattering events. The energy exchange through scattering forms a fraction of HC in the carrier ensemble, causing bond dissociation. The bond dissociation involving a single collision is known as the single-particle (SP) process. In addition to the SP, in an ultra-scaled

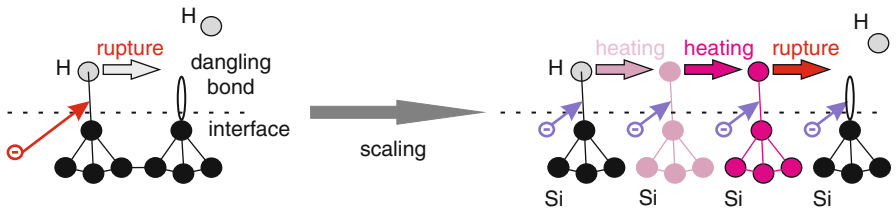


FIGURE 2.4: Schematic [145] illustrating the evolution of bond dissociation mechanism under HC stress from single-particle (SP) process to multi-particle (MP) process in ultra-scaled devices. In the SP process, a carrier having enough energy to rupture the Si-H bond can create an interface trap. In the MP process, several colder particles are bombarding and eventually leading to multiple vibrational bond dissociations.

modern device, the HCD is mainly governed by the multi-particle (MP) process in which several cold carriers bombard the interface triggering multi-vibration excitation of the bond, causing the bond rupturing, as illustrated in Fig. 2.4 [126]. Thus, even with low supply voltages of ultra-scaled technologies, the MP process acts as a dominant HCD mechanism [145]. Along with interface traps, the contribution of switching oxide traps in HCD is not extensively reported in the literature. This is due to their nature of recovering after removing stress, as in the case of BTI. However, the observed turn-around effect in HCD is explained by the oxide states and will be discussed in Chapter 6. HCD is typically modeled as a function of the gate to source voltage ($V_{gs}$), drain to source voltage ($V_{ds}$), and temperature ($T$). The evolution of the bond dissociation process explains the change of HCD worst-case condition in short channel devices from $V_{gs} \approx V_{ds}/2$ to $V_{gs}$=$V_{ds}$. In a long channel device, the maximum substrate current, which serves as an indicator of the impact ionization rate, occurs at mid-$V_{gs}$ condition [146]. In other words, the amount of HCD in long channel devices is proportional to the average carrier energy [147], [148]. However, in the ultra-scaled devices, the carrier flux instead of carrier energy governs the MP process, which is dominant at $V_{gs} \approx V_{ds}$ [126], [149].

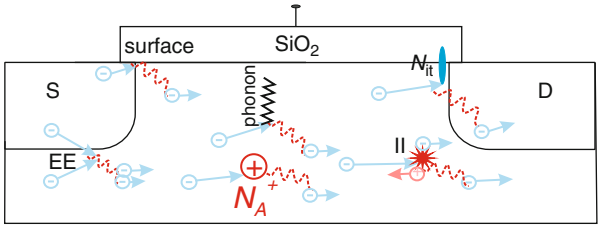


FIGURE 2.5: Schematic representation of different scattering mechanisms in a MOSFET [145]. EE and $N_A$ referred to electron-electron and electron-ionized impurity scattering, respectively.

Temperature dependence of HCD is an important aspect, and with the technology scaling, different dependence is observed for long channel and short channel devices. With the increase of temperature, HCD in long channel devices decreases [150], while for the short channel devices, it increases [149], [151]–[153]. Both temperature behaviors are associated with scattering events. As the carriers are accelerated under the electric field in a MOSFET, different scattering events occur. The rate of scattering events intensifies with the increase of temperature. Fig. 2.5 depicts the electron-electron scattering, surface scattering, electron-phonon scattering, electron scattering with ionized impurities, impact ionization, and electron scattering with charged interface traps. In long channel devices where the SP process is the dominant HCD mechanism, the scattering events decrease the fraction of hot enough carriers, explaining the suppression of HCD at high temperatures. On the other hand, electron-electron scattering is the dominant mechanism [137], [142], [154], [155] that populates the carrier ensemble's hot carrier fraction in short channel devices. As scattering is proportional to temperature, the MP process also scales with higher temperatures [145]. In ultra-scaled devices having channel length comparable to the electron mean free path, the probability of electron-electron scattering is more than other scattering events. However, the contribution of other scattering mechanisms such as impact ionization and phonon scattering cannot be ruled out [156]–[158].

### 2.4.2 Bias Temperature Instability

The phenomenon of BTI is known for almost six decades. In the 1960s, Miura and Matukura observed an increase of electron density under positive temperature treatment of MOSFET's gate and linked this behavior to the vacancies in the oxide [159]. This instability phenomenon later got more interest when nitrogen was introduced in the gate stack in scaled devices, leading to significant distortion of device characteristics under gate stress [160], [161]. BTI, as its name suggests, is a function of gate bias, temperature, and time. BTI in MOSFETs is typically characterized under relatively higher gate bias (voltage acceleration) with no drain bias at elevated temperatures (temperature acceleration). Depending on the bias polarity, the stresses can be classified as negative bias temperature instability (NBTI) and positive bias temperature instability (PBTI). Both NBTI and PBTI stress can be applied to n-MOSFETs and p-MOSFETs, resulting in a respective behavioral impact on device characteristics. Due to a more pronounced effect on device performance, NBTI in p-MOSFET and PBTI in n-MOSFET are the subjects of greater interest [162]–[164]. Typically impacted device parameters due to BTI stress are $V_{\text{th}}$, $I_{\text{d}}$, SS, and $g_m$ decrement related to effective mobility ($\mu_{\text{eff}}$) degradation [163], [165]. Oxide defects and interface defects are associated with the $V_{\text{th}}$ shift and mobility degradation, respectively. Oxide defects or bulk oxide traps can be pre-existing oxide traps or newly generated traps. BTI constitutes a degradation component that is instantly recovered as soon as the stress is removed. Another degradation component, termed as permanent component (P), is also referred to as quasi-permanent. However, it has been shown in the literature that under opposite bias pulses and annealing temperatures, complete recovery and reverse recovery effects can be observed [166]. An agreement on a precise definition of permanent component and associated plateau level is yet to be reached [165], [166]. The physical mechanisms governing the BTI degradation has still not yet reached consensus in the scientific community. However, the two mainly discussed perspectives are known as the *Reaction-Diffusion* model [167] and *Defect-Centric* model [168], [169].

The reaction-diffusion model assumes the dissociation of the Si-H bond at the interface by the channel holes (in the case of NBTI) under vertical electric field stress. The resulting dangling bonds then act as an interface trap/state. The initial dissociation of passivated bonds is termed a forward reaction. As the atomic H concentration increases at the interface, a backward reaction occurs, which then passivates the existing dangling bond. Within 1 s, an equilibrium is reached for the forward and backward reaction. After this phase, a diffusion-limited regime starts in which $H_2$ diffuses away from the interface resulting in an increase of interface traps that follows a power law. $H_2$ is formed by the reaction of released H with another hydrogen passivated defect at the interface at any of the following bulk or interface: $Si/SiO_2$, $SiO_2$, $SiO_2$/poly-Si, $SiO_2$/high-k dielectric, or high-k dielectric [165]. This reaction results in bulk defects in addition to interface defects. It is observed that the interface trap generation is the dominant mechanism under low-stress voltages and low temperatures. In contrast, oxide trap concentration becomes significant at higher stress voltages and higher temperatures [167]. The recovery effect in the reaction-diffusion model is associated with the passivation of Si dangling bonds by $H_2$ at the channel/oxide interface and interface of oxide with other dielectric or poly-Si (internal interface). Longer recovery times are explained by the reduction in the density of un-passivated bonds at the internal interface with time [167], [170]. The longer recovery time is the main critique of the

reaction-diffusion model. The recovery is governed by the back diffusion of hydrogen and should occur in similar time frames as the stress time. Moreover, the recovery and stress time should scale accordingly. In time-dependent defect spectroscopy (TDDS), this should translate into a shift of $V_{th}$ recovery steps to longer relaxation times for longer stress times. On the contrary, this correlation has not been observed, and emission times (relaxation time for the $V_{th}$ recovery step) do not relate to the stress times [171], [172]. In addition to that, the bond dissociation energy of Si-H and energy barrier for Si passivation with $H_2$ assumed in the reaction-diffusion model is considerably lower compared to the literature values [165]. On the other hand, the reaction-diffusion model holds basis due to consistent time exponent (1/6) for the $V_{th}$ shift associated with interface trap generation among several devices [173] and average $V_{th}$ shift behavior (typically in large area devices) during the stress phase based on reaction-diffusion theory.

The defect-centric model or charge trapping mechanism attempts to explain the experimental data of recovery behavior which were not aligned with the theory of the reaction-diffusion model [163], [174], [175]. The de-trapping events observed during recovery in TDDS for shorter time scales are attributed to the existence of oxide traps because interface state passivation does not occur in such time scales. The recovery effect accelerated by the application of bias also does not fit with the bias independent recovery mechanism of passivation by $H_2$ back diffusion [168]. Discrete recovery steps in ultra-scaled devices also contradict diffusion-limited processes and are aligned with the emission of individual holes based on a first-order reaction-rate process [176], [177]. The defect-centric model involves the concept of charge trapping in the oxide defects supported by a multi-photon emission process [178]. The most recent version of this model is the four-state switching trap model having neutral, charged, and two meta-stable states. During stress and recovery, the charge transfer reactions based on the physical chemistry model describe the bias and temperature dependence [165]. Recent studies show that the dominant contribution in NBTI degradation arises from hole trapping [174], [176], [179]–[182].

In terms of BTI characterization, among other degraded parameters, typically, the $V_{th}$ of a MOSFET is tracked throughout the stress time. For an accurate characterization, capturing the recoverable component (R) is very important and challenging as the degradation is significantly relaxed just within few milliseconds [23] (even happening in microseconds time scales [174], [183]). The improvements in the characterization methods are ranked by the fast-tracking ability of R, the shortest interruption of stress, or ideally having continuous stress. Having a precise quantification of BTI effects is crucial for a better understanding of the degradation mechanism and an accurate prediction of device lifetimes. Several characterization schemes have been developed and improved in these terms [163], [184], [185], and one such attempt is also a part of this dissertation using an alternate measurement approach (i.e., RF measurements).

## 2.5 Self-heating

Self-heating or joule heating in semiconductor devices is commonly referred to as heating of the lattice through scattering events. Under an applied electric field, the carrier accelerates and encounters several scattering mechanisms, as shown in Fig. 2.5. As a result of scattering, the loss of electron energy generates optical and acoustic phonons. Optical phonons act as a stationary elements and do not

contribute to heat transport. The heat transport is dominated by acoustic phonons[186], [187]. Optical phonons are slow and decay into faster acoustic phonons, which carry the heat away following the heat gradient. The time scales of electron-phonon scattering and optical to acoustic phonon decay are in the order of 1/10 of picoseconds and picoseconds, respectively [188]. Depending on the rate of electron-phonon scattering due to the current flow and rate of optical to acoustic phonon decay, the electron transport can be affected due to the non-equilibrium build-up of the optical mode density shown in Fig. 2.6.

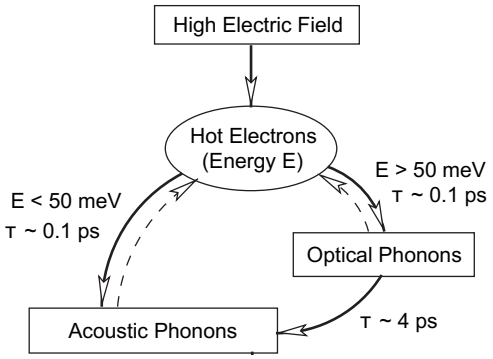


FIGURE 2.6: Representation [189] of phonon generation along with time scales and energy dependence in silicon. For carriers with energy > 50 meV, the dominant mechanism of relaxation is scattering with optical phonon, leading to even more scattering events until the optical to acoustic phonon decay [190]. The dotted line represents the transfer of energy from phonon to electrons through parallel scattering events.

The scaling of semiconductor technology had greatly impacted the power density and critical dimensions of the devices. The rate of generation of heat and rate of transfer defines the amount of equivalent lattice heat. Along with the thermal conductivities of the used materials within the device, the device design also plays a crucial role in determining the amount of self-heating. Scaling trends such as short channel lengths, thinner oxides, different dielectric materials, SOI technologies, strained layers, and highly doped regions significantly impact self-heating. In bulk silicon, the mean free path for electrons and phonons is in the range of 5-10 nm and 200-300 nm, respectively [186], [191]. Modern ultra-scaled devices are in a similar order of dimension of these mean free paths. At such scaled dimensions, ballistic conditions dominate resulting in increased surface and boundary scattering [192]. This leads to a local hot spot and much higher temperatures as computed by the classical heat diffusion equation [193], [194]. The thermal conductivity of $SiO_2$ is two orders of magnitude lower than that of bulk silicon [195]. Thermal conductivity of Si, $SiO_2$, and $HfO_2$ reduces dramatically in nano-scaled dimensions [192], [195], [196]. The confine geometries imply a larger surface to volume ratio having a strong boundary resistance impact. The thermal conductivity of Ge is 60% lower as compared to that of Si. The introduction of Ge dopants in the silicon to increase the channel mobility results in reduced thermal conductivity. In SOI technologies, the oxide layer separating the heat source (channel) from the substrate worsens heat dissipation. In FDSOI devices, having a thicker BOX obstructs the heat dissipation while reducing the BOX thickness compromises its thermal conductivity [197]. However, thinner BOX is shown to have improved thermal characteristics [192]. Doping in semiconductors also influences the thermal characteristics and is prone to enhance scattering, resulting in poor thermal conductivity. In the literature several simulation and experimental

studies are devoted to the investigation of the self-heating effect in FDSOI devices [95], [192], [198]–[201]. For the characterization of self-heating effects in ultra-scaled devices having thermal time constants in the range of few nanoseconds, RF measurement is readily deployed because of the limited accuracy of pulsed measurement techniques [202]–[205].

Self-heating affects the performance of a device due to increased temperature. The temperature-dependent material parameters mainly impact device characteristics. One such parameter which is often associated with self-heating is $\mu_{\text{eff}}$ according to equation 2.1 [206]. Increased temperatures result in enhance scattering, which degrades the carrier mobility. Mobility degradation in a MOSFET is an interplay between four different scattering mechanisms, i.e., phonon scattering, surface roughness scattering, bulk charge coulombic scattering, and interface charge coulombic scattering [207].

$$\mu_{\text{eff}} = \mu_{\text{eff}0}\left(\frac{T}{T_0}\right)^{-k} \tag{2.1}$$

where $\mu_{\text{eff}0}$ is $\mu_{\text{eff}}$ at ambient temperature ($T_0$), T is the average channel temperature, and k is the mobility degradation factor. The most fundamental property of a material is the energy bandgap ($E_g$) which is again dependent on temperature. $V_{\text{th}}$ is the device parameter that is directly affected by $E_g$, fermi potential ($\phi_F$), and depletion charge ($Q_{\text{dep}}$) [208]. In the FDSOI device, $Q_{\text{dep}}$ dependence on temperatures arises from Fermi potential, which is affected by temperature-dependent intrinsic concentration. With the increase of temperature, the intrinsic carrier concentration increases, causing the Fermi potential to decrease, eventually reducing the $V_{\text{th}}$ [208]. Another temperature-dependent property governing the on current is the saturation velocity ($v_{\text{sat}}$) [209] which is modeled in BSIM4 device model as [210]:

$$v_{\text{sat}}(T) = v_{\text{sat}0}\big(1 - \alpha_{v_{sat}}(T - T_0)\big) \tag{2.2}$$

where $\alpha_{v_{sat}}$ is the saturation velocity temperature coefficient. Due to increased scattering at higher temperatures, $v_{\text{sat}}$ is degraded. Depending on the dominant governing mechanism at different operating conditions, the device will experience corresponding effects. In addition to device characteristics, self-heating can have detrimental effects on device reliability. Many of the degradation mechanisms are the function of temperature and usually get worse at higher temperatures. It is important to note that MOSFETs have thermal characteristic frequency ($f_{th}$) above which the device stop following the instantaneous voltage changes. In digital applications, if the operating frequencies are above $f_{th}$, heat is effectively low-pass filtered, and self-heating does not remain a concern. However, in analog applications with larger voltage swings, self-heating should be carefully considered. Depending on the operating frequency range, an aggravated self-heating effect can influence device analog/RF performance, especially at frequencies < $f_{th}$ [211].

# Chapter 3

# RF Characterization of fully-depleted Silicon on Insulator devices

Characterization is one of the first steps that enable the path to developing, optimizing, and modeling transistor technologies. For the high-speed digital, RF, and analog applications, the assessment of transistor performance and model parameters at high frequencies is needed. Scaling, the introduction of new materials, and novel device concepts enable the operating speeds of MOSFETs in the range of hundreds of GHz [1], [2], [84], [212]–[216]. An accurate and reliable characterization of such high-frequency devices under different operating conditions is essential. This chapter presents the RF characterization flow, equivalent small-signal model, and the extraction of those model parameters used throughout the dissertation.

## 3.1 Scattering Parameters

A convenient way to understand and predict the behavior of an electrical device or a circuit is to express its operation in terms of mathematical equations and expressions. If these circuits or devices consist of linear components, they can be described using linear equations involving current and voltages as independent and dependent quantities. This approach can be used to define any device or complex circuit by masking it as a black box with single or multiple input and output ports. The black box is also referred to as a network with n number of ports. The performance n-port linear network is primarily characterized by the admittance parameters (Y-parameters) and impedance parameters (Z-parameters). These parameters can be measured and described in terms of current ($I$) and voltage ($V$) at the input and output ports. At higher frequencies, the accurate measurement of $I$ and $V$ quantities becomes very difficult due to the probe impedance itself and hard to achieve ideal open and short terminations. A non-ideal termination can lead to oscillation or self-destruction in an active device [217].

Consequently, to avoid these drawbacks and obtain accurate measurements at high frequency, another set of parameters is used, known as scattering parameters. S-parameters were first mentioned in 1920 [218], [219], and later on, applied for solving microwave design problems in circuits [220]. S-parameters quantify the reflection and propagation of RF energy through a multi-port network by measuring incident, reflected, and transmitted power waves at 50 Ω termination. The characteristic impedance ($Z_o$) usually equals 50 Ω and is easier to realize as

compared to an ideal open or short and a good compromise for non-ideal ground and capacitive open. $Z_o$ = 50 Ω is historically selected as a reference due to the fact that the coaxial cable exhibits minimum losses at such impedance [221, Chapter 3]. Unlike terminal voltages and currents, the magnitude of traveling waves does not vary along a lossless transmission line and can be reliably measured by measurement equipment located at some distance from the device. Obtained S-parameters then can be converted into other parameters such as Y, Z, h (hybrid), ABCD (chain), and T (chain transfer) as explained in [222], [223].

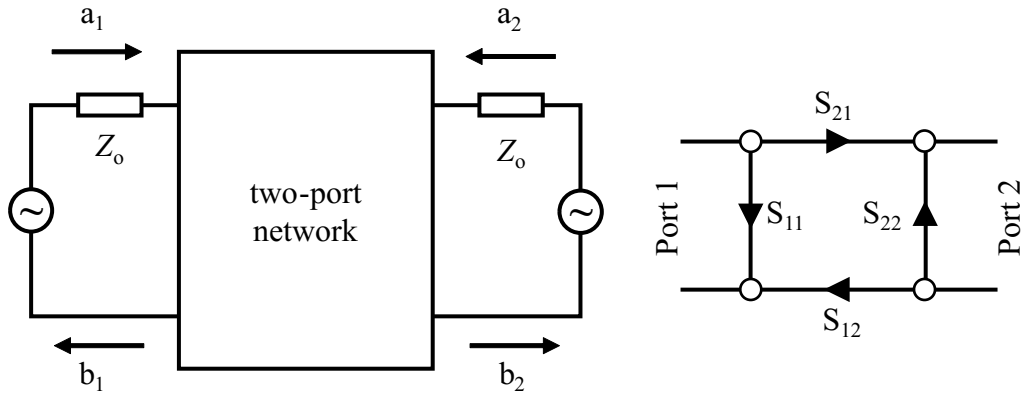


FIGURE 3.1: S-parameter definition of a two-port network showing incident ($a_1$, $a_2$) and reflected ($b_1$, $b_2$) power waves (right). Signal flow graph of a two-port network (right).

S-parameters for the two-port network shown in Figure 3.1 are defined as:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{3.1}$$

where $a_1$ and $a_2$ are the incident power at port 1 and port 2, while $b_1$ and $b_2$ are the reflected power from port 1 and port 2. The S-matrix in expression (3.1) has four coefficients for the two-port network, representing possible input and output paths. Similarly, an n-port network contains $n^2$ coefficients. The individual S-parameter coefficients can be expressed as:

**Input reflection coefficient**

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0}$$

**Reverse transmission coefficient**

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0}$$

**Forward transmission coefficient**

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0}$$

**Output reflection coefficient**

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0}$$

Conventionally in S-parameter coefficients, the number followed by S represents the port where the signal emerges and the second number where the signal is entered. S-parameters are complex numbers containing information about the magnitude and phase of the signal. The magnitude and phase of the incident reflected and transmitted power waves are measured at one port by terminating the

other port with perfect $Z_o$ load. Terminating a port with $Z_o$ ensures that there is no power fed from that port, and at a given time, only one source is active. However, when the device or fixture is connected for the measurement, the termination is not always a perfect load in practical applications. This impedance mismatch influences the accuracy of the S-parameters measurement, and in order to correct the impedance mismatch, the two-port calibration is required. The magnitude (1, 0, -1) of reflection coefficients $S_{11}$ and $S_{22}$ corresponds to the impedance of $\infty$ Ω (all power reflected), 50 Ω (perfect match, no reflection), and 0 Ω (all power inverted and reflected) respectively. $S_{12}$ and $S_{21}$ representing the reverse and forward transmission coefficients, can have positive or negative magnitude. The negative magnitude of the transmission coefficients is attributed to the phase inversion. The magnitude of 0 represents no signal transmission, $0 \leq x \leq +1$ means damping of the input signal, +1 represents the transmission of a signal without amplification, or damping $x \geq +1$ represents amplification of the input signal. To comprehend the two-port network in terms of voltage and current waves, the normalized waves can be expressed as the function of incident current ($I_t$), reflected current ($I_r$) or incident voltage ($V_t$), and reflected voltage ($V_r$). For example, in the two-port network shown in Fig. 3.1 with values of $i$ and $j$ as 1 and 2, the normalized power waves are defined as

$$a_i = \frac{1}{2}\left(\frac{V_{i,t}}{\sqrt{Z_o}} + I_{i,t}\sqrt{Z_o}\right), \tag{3.2}$$

$$b_i = \frac{1}{2}\left(\frac{V_{j,r}}{\sqrt{Z_o}} - I_{j,r}\sqrt{Z_o}\right). \tag{3.3}$$

In this work, the studied transistors are configured in a two-port network. Measured S-parameters of such a two-port network can describe the behavior of various individual components of the studied transistor, which then are used to understand and analyze its performance.

## 3.2 S-parameters Measurement Flow

The S-parameter measurement is performed using a vector network analyzer (VNA). VNA is an instrument that has deployed the network analysis technique to characterize linear devices in the frequency domain since the late 1950s. From the very first simple and manually operated test setups, VNA has developed to be highly sophisticated and automated measurement systems extending the measurement frequency up to THz [224]–[228].

The basic measurement principle of the VNA is that it measures the magnitude and phase of the incident, transmitted, and reflected wave quantities. While measuring S-parameters, the power of the applied incident signal is low enough (small-signal) to ensure the linear response of the device under test (DUT). The incident signal is generated by a high-frequency signal generator, also known as an RF synthesizer, and fed into the DUT alternatively through port 1 and port 2. The reflected and transmitted signal through the DUT is then measured by the receiver on both ports. Directional couplers are deployed to detect the incident and reflected signal at the same port. The received signals are then down-converted to an intermediate frequency (IF) for further processing in the VNA. A schematic representation of the S-parameters measurement test setup is shown in Fig. 3.2. A

constant voltage is applied via the source measure unit (SMU) to set an operating point of the DUT. Both DC bias and high-frequency small-signal are fed into the bias-tee, which outputs an RF signal overlapping on a constant DC bias voltage. The bias-tee consists of an inductor (for DC) and a capacitor(for high frequency) to protect against feeding the signals of VNA and SMU into each other. The DUT shown in Fig. 3.2 is configured in a ground-signal-ground (GSG) pad layout, which prevents resonance loops with symmetrical grounds [229] and enables higher bandwidth [230]. The most commonly used VNA measurement settings in this work are frequency ($f$) = 10 MHz to 50 GHz (depending on the type of analysis), input power ($P_{\text{in}}$) = -25 dBm, and IF filter bandwidth = 100 Hz. For small-signal measurements, the magnitude of input power is chosen as such that the device response remains linear. Measurement of S-parameters at higher frequencies is susceptible to the signal perturbation introduced by setup fixtures and interconnects. To obtain an accurate measurement of the DUT, these parasitic elements must be measured and eliminated. Hence, the first step of the measurement flow is to calibrate the VNA to account for the external test fixtures. The calibration step is then followed by a de-embedding procedure in which the contact pad and interconnect parasitic elements of the wafer are measured and removed.

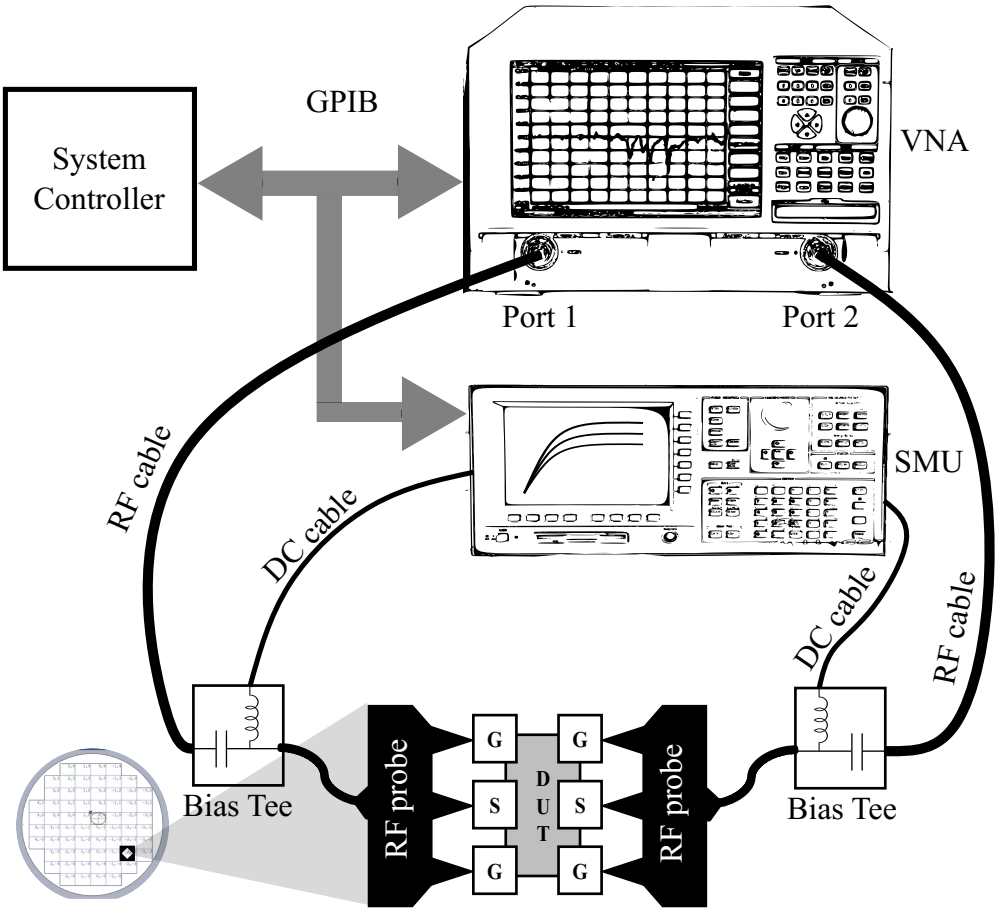


FIGURE 3.2: RF characterization test setup used for measuring S-parameters of a two-port network at the wafer level.

### 3.2.1 Calibration

Calibration is performed before the measurement of the DUT to remove systematic errors introduced by the accessories and fixtures attached with the VNA. Commonly used fixtures for the on-wafer measurement are coaxial cables, coaxial adapter, and RF probes (Fig. 3.2). Initially, before calibration, the measurement boundary, also known as the reference plane, is set at the ports of the VNA. The calibration procedure shifts the reference plane to the probe needles. After connecting all the required fixtures, the S-parameters of the known calibration standards are measured to compute the error terms. The calibration standards are provided in the form of a calibration substrate, which contains open, short, through, line, and load structures of known impedance. The most commonly used calibration standards are shown in Fig. 3.3. Various calibration algorithms, such as short-open-load-through (SOLT), line-reflect-reflect-match (LRRM), and through-reflect-line (TRL), etc., are used depending on the measurement frequency, required accuracy, and availability of calibration standards. These calibration algorithms compute error terms to form an error model, which is then applied to the VNA for error correction. The number of error terms or error coefficients included in the error models depends on the number of used ports, measurement accuracy, and hardware topology of the VNA [231]. In this work, the LRRM calibration algorithm is used. LRRM calibration algorithm was first developed in 1990 [232], having less sensitivity to the probe placement on calibration standards and better tolerance for the specification of open and short structures compared to SOLT [233].

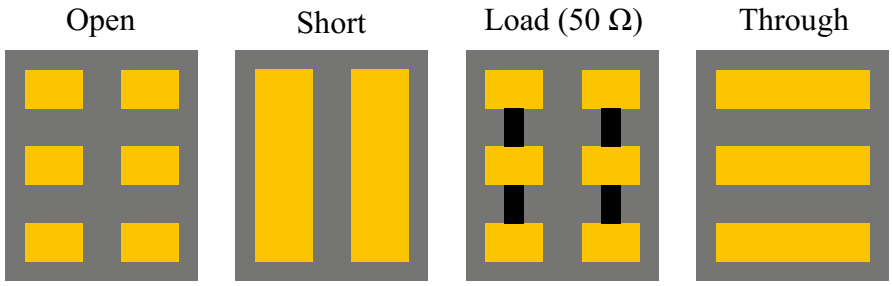


FIGURE 3.3: Example of co-planar calibration standards layout on commercially available calibration substrate. Exact specifications (impedance) of such calibration standards are provided by vendors to be used in the calibration procedure.

### 3.2.2 De-embedding

A successful calibration brings the measurement reference plane to the tips of the RF probes. The goal of the measurement is to obtain the S-parameters of the DUT (i.e., a transistor), which is just a few micrometers in size and cannot be probed directly. To connect the core transistor, there exist many levels of back-end-of-line (BEOL) metallization and vias. The metal lines at different levels separated by the dielectric material exhibit parasitic capacitance while the via and extended metal lines introduce series resistance and inductance. These contact pads and interconnects have a substantial amount of parasitic impedance at high frequencies, which can even be several orders of magnitude larger than that of the device itself. The surrounding parasitic impedance is removed from the total measurement to obtain the device's measurement through a de-embedding process. De-embedding further moves the measurement reference plane to the boundaries of the actual

device of interest. Special structures called de-embedding dummies having identical BEOL stack as the DUT are fabricated. The open and short dummies, along with their equivalent schematic, are shown in Fig. 3.4. S-parameters of both dummies and DUT are measured by a calibrated VNA and converted into respective Y- and Z-parameters. A two-step de-embedding process is then applied in which parallel and series parasitic elements are removed using open and short de-embedding dummies, respectively.

$$1^{st}step: \quad Y_{DUT-O} = Y_{DUT} - Y_{open}; \quad Y_{short-O} = Y_{short} - Y_{open}$$

$$2^{nd}step: \quad Z_{DUT} = Z_{DUT-O} - Z_{short-O}$$

Depending on the measurement application, accuracy, and design of the DUT, more complex de-embedding can also be applied, which requires more dummy elements. However, for the analysis done in this work, the two-step de-embedding is used having sufficient accuracy for the frequency range of interest.

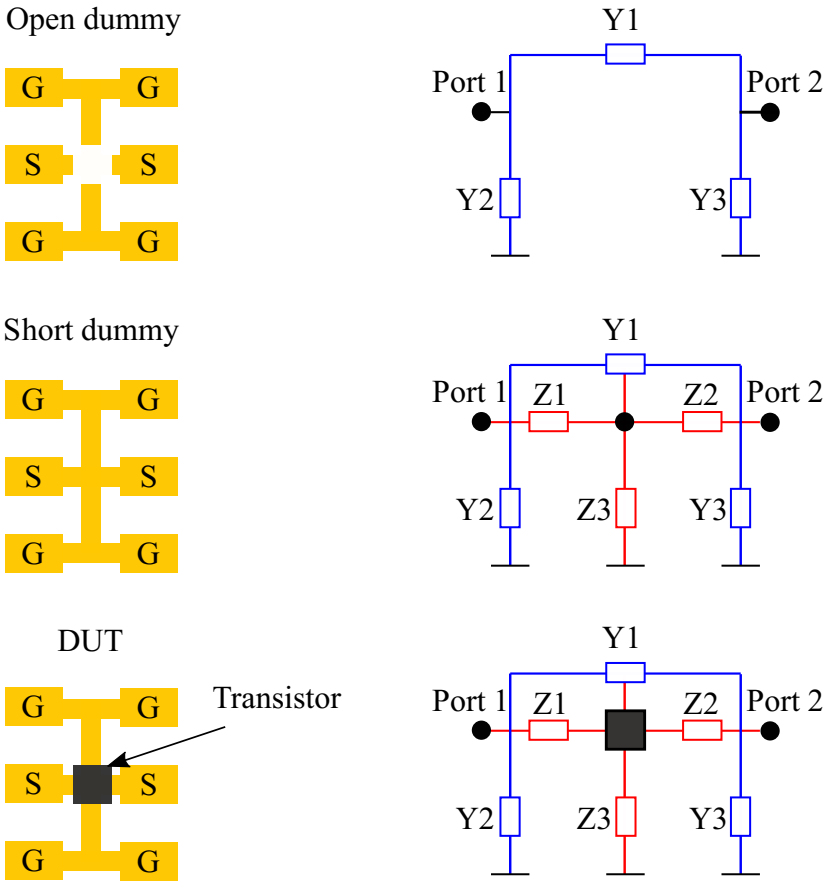


FIGURE 3.4: Representation of BEOL parasitic around the device by open and short dummies with their equivalent schematic (right) for series (Z) and parallel (Y) parasitic elements.

## 3.3 Small-Signal Model

The translation of functioning principle and to extract individual parameters of an FDSOI MOSFET under high-frequency small-signal operation, a small-signal equivalent circuit derived from [234] is shown in Fig. 3.5(a) is used. The equivalent

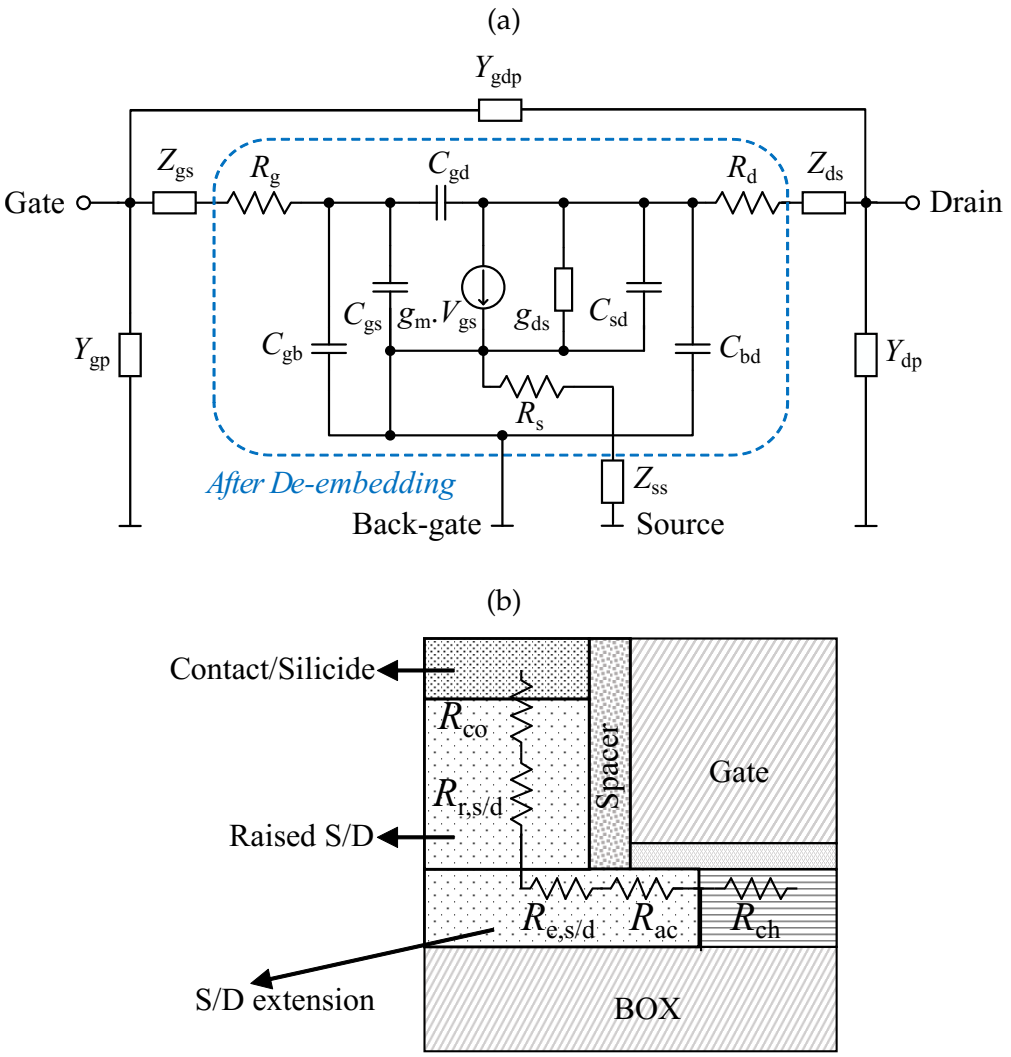


FIGURE 3.5: (a) Small-signal model for an FDSOI MOSFET in common source configuration including pad and interconnect parasitic impedances. Back-gate and substrate connection are tied to the source. (b) Schematic representation of the drain/source series resistance components in a FDSOI MOSFET.

circuit is configured in common source mode with the back gate and source tied together. The de-embedded equivalent circuit can be divided into bias-dependent and bias independent, i.e., intrinsic and extrinsic parts. The series resistances (i.e., source resistance ($R_s$) and drain resistance ($R_d$)) are usually considered extrinsic components; however, the breakdown of these series components reveals the presence of bias-dependent components as well (Fig. 3.5(b)). The series resistance at the drain side, for example, comprised of contact resistance ($R_{co}$), raised source/drain resistance ($R_{r,s/d}$), source/drain extension resistance ($R_{e,s/d}$), and accumulation resistance ($R_{ac}$). The same scheme can also be applied on the source side. $R_{ac}$ is a bias-dependent component as the gate charge can influence the accumulation in the gate to source/drain overlap region [235]–[237]. Another bias-dependent series resistance component due to doping gradient (i.e., spreading resistance) is insignificant in FDSOI devices due to the formation of source/drain regions by a dual in-situ doped epi process [1], [182], [235]. The total gate capacitance ($C_{gg}$) includes mainly gate-source capacitance ($C_{gs}$), and gate-drain capacitance ($C_{gd}$) distributed towards the source and drain regions, respectively,

governed by the inversion layer formed over the channel. $C_{gs}$ and $C_{gd}$ also comprise fringing and source/drain overlap capacitances.

### 3.3.1 Model Parameters Extraction

The small-signal model parameters shown in 3.5(a) are extracted using the S-matrix measured under various bias conditions. The extrinsic elements can be extracted at zero drain bias (cold-FET) condition, thereby reducing the varying effect of bias-dependent intrinsic elements. Table 3.1 lists the expressions used for the extraction of small-signal model parameters from S-parameter measurements.

TABLE 3.1: Summary of expressions used to extract of equivalent small-signal model components from converted Y- and Z-parameters.

| **Small-signal component** | **Expression** |
|---|---|
| transconductance ($g_m$) | $g_m = Re[Y_{21}]$ |
| output-conductance ($g_{ds}$) | $g_{ds} = Re[Y_{22}]$ |
| gate-source capacitance ($C_{gs}$) + gate-back-gate capacitance ($C_{gb}$) | $C_{gs} + C_{gb} = \frac{Im[Y_{11} + Y_{12}]}{w}$ |
| gate-drain capacitance ($C_{gd}$) | $C_{gd} = -\frac{Im[Y_{12}]}{w}$ |
| total gate capacitance ($C_{gg}$) | $C_{gg} = \frac{Im[Y_{11}]}{w}$ |
| drain-source capacitance ($C_{sd}$) + drain-back-gate capacitance ($C_{bd}$) | $C_{sd} + C_{bd} = \frac{Im[Y_{22} + Y_{12}]}{w}$ |
| gate resistance ($R_g$) | $R_g = Re[Z_{11} - Z_{12}]$ |
| source resistance ($R_s$) | $R_s = Re[Z_{12}]$ |
| drain resistance ($R_d$) | $R_d = Re[Z_{22} - Z_{12}]$ |

### 3.3.2 Transistor Figures of Merit

The parameters readily used for benchmarking the RF transistor performance are transit-frequency ($f_t$) and maximum oscillation frequency ($f_{max}$). $f_t$ is defined as the frequency where the short circuit current gain is unity. In real case applications, the output usually has a non-zero impedance which lowers the output current leading to the reduction of $f_t$. $f_t$ serves as the measure of the intrinsic speed of the transistor. $f_t$ can be derived from an equivalent circuit shown in 3.5(a), where the gate to source serves as an input terminal and drain to source serve as an output terminal. The corresponding terminal voltages and currents are $V_{gs}$, $V_{ds}$, $I_d$, and source current ($I_s$)

$$\frac{I_d(w)}{I_g(w)} = \frac{(g_m - jwC_{gd})V_{gs}(w)}{jw(C_{gs} + C_{gd})V_{gs}(w)}. \tag{3.4}$$

For $jwC_{gd} \ll g_m$

$$\frac{I_d(w)}{I_g(w)} \approx \frac{g_m}{jw(C_{gs}+C_{gd})}. \tag{3.5}$$

When the current gain is unity at the transit frequency ($w_t$)

$$1 = \frac{g_m}{w_t(C_{gs}+C_{gd})}, \tag{3.6}$$

$$f_t = \frac{g_m}{2\pi(C_{gs}+C_{gd})} = |H_{21}|. \tag{3.7}$$

In the above equation, $g_m$ is proportional to $I_d$, gate width ($w_g$), and ($1/l_g$), while $C_{gs}$ and $C_{gd}$ are proportional to $w_g$ and $l_g$. Hence, $f_t$ increases for higher supply current, shorter $l_g$, and is independent of $w_g$. With the scaling of technology, short channel effects and the impact of parasitic components cannot be ignored. At such scaled dimensions, the parasitic components become a function of device perimeter and layout. As a result, $f_t$ scaling deviates from ideal trends of $1/{l_g}^2$ and constant $w_g$. Md Arshad, Kilchytska, Emam, *et al.* [238] extracted $f_t$ as a function of capacitance and resistance components of the equivalent circuit shown in 3.5(a)

$$f_t \approx \frac{g_m}{2\pi C_{gs}} \frac{1}{(1+C_{gd}/C_{gs}) + (R_s+R_d)(C_{gd}/C_{gs}(g_m+g_{ds})+g_{ds})}. \tag{3.8}$$

The non-proportional reduction of $g_m$, $C_{gs}$, and $C_{gd}$ with $w_g$ result in $f_t$ being affected for narrower $w_g$ [238]. Although $f_t$ is the most common figure of merit, it does not reflect the voltage gain performance. Therefore, another widely used metric for the assessment of power gain performance is $f_{max}$. $f_{max}$ is defined as the frequency where the maximum unilateral or Mason's gain (U) is unity. U is the device's gain under conjugate matching of input/output impedances and unilaterization through a feedback mechanism. The value of U can be extracted from S-parameters as:

$$U = \frac{|Y_{21}-Y_{12}|^2}{4(Re[Y_{11}]Re[Y_{22}] - Re[Y_{12}]Re[Y_{21}])}. \tag{3.9}$$

$f_{max}$ is highly sensitive to parasitic losses in the device, most importantly $R_g$. Depending on the layout of the device, $f_{max}$ can be higher or lower than $f_t$. Traditionally for larger $l_g$, $f_{max}$ is higher compared to $f_t$ while for the shorter $l_g$, $f_{max}$ decreases due to an increase in $R_g$ [238]. The ratio of $f_{max}/f_t$ serves as a metric to evaluate the degree of layout optimization [239]. To achieve an optimum circuit performance and compensate for the losses, $f_{max}$ should be multiple times higher than the system operating frequency. Depending on an application, for instance, in amplifiers, the required values of $f_{max}$ can be up to 10 times the operation frequency [221, Chapter 5]. $f_{max}$ in terms of small-signal model components is expressed as [238]:

$$f_{max} \approx \frac{g_m}{4\pi C_{gs}} \frac{1}{(1+C_{gd}/C_{gs})\sqrt{g_{ds}(R_g+R_s)+1/2(C_{gd}/C_{gs})(R_s g_m + C_{gd}/C_{gs})}}. \tag{3.10}$$

## 3.4 Characterization Results

The measured S-parameters are generally converted into Y-parameters which are more insightful in terms of understanding device physics (see Appendix A). Several devices are measured on different dies of a wafer to obtain statistically precise measurements, and median data is plotted for analysis. Using expressions listed in Table 3.1, the small-signal model components are analyzed.

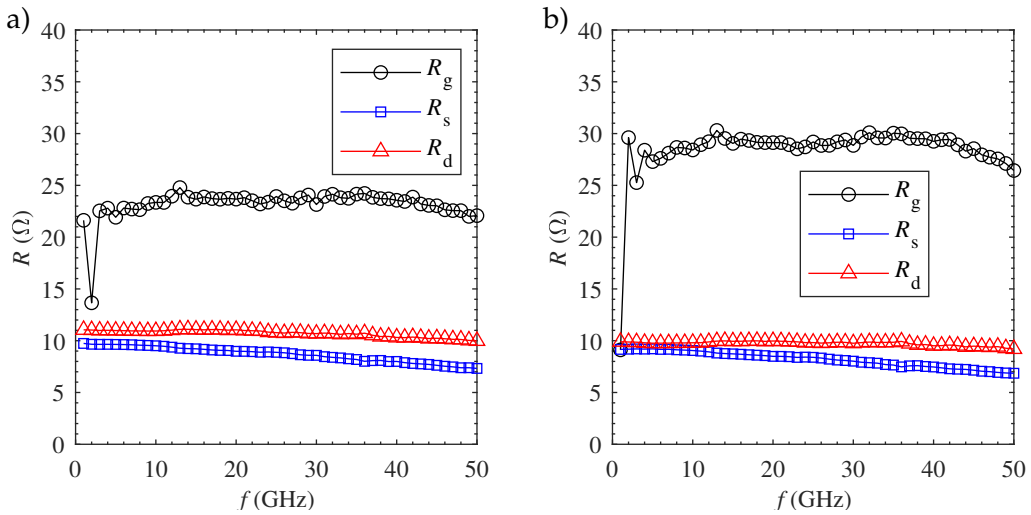


FIGURE 3.6: Frequency dependence of the extracted gate, source, and drain series resistance biased at $|V_{gs}| = 0.8$ V and $V_{ds} = 0$ V for (a) p-MOSFET and (b) n-MOSFET respectively with device dimension of $l_g = 18$ nm, width per finger ($w_f$) = 1 $\mu$m, and number of fingers ($nf$) = 16.

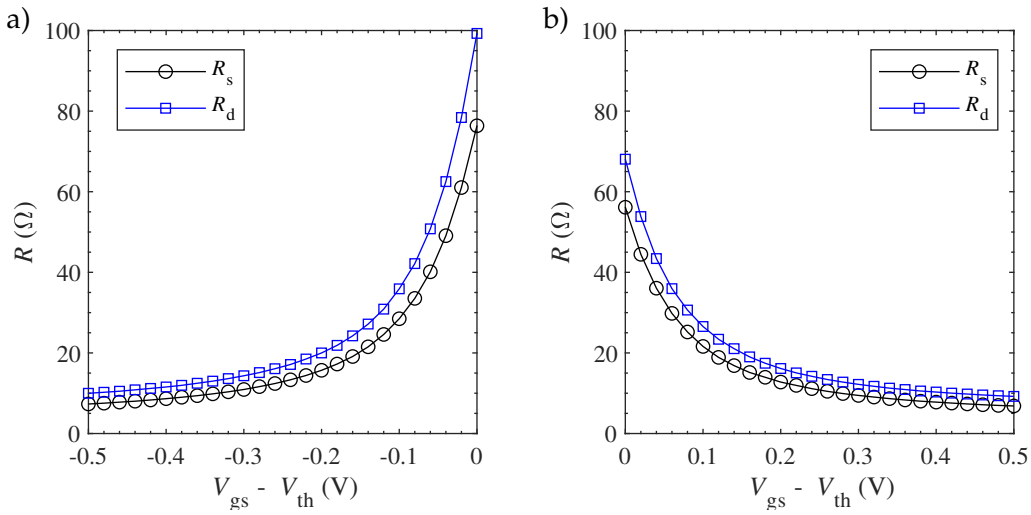


FIGURE 3.7: Bias-dependent source and drain series resistance extracted at $V_{ds} = 0$ V and $f = 50$ GHz for (a) p-MOSFET and (b) n-MOSFET respectively with device dimension of $l_g = 18$ nm, $w_f = 1$ $\mu$m, and $nf = 16$.

Fig. 3.6 shows the extracted values of series resistance components of the small-signal model with respect to frequency in cold-fet condition and strong inversion for both p-MOSFET and n-MOSFET. Under strong inversion, the channel resistance is significantly smaller than the back-gate and substrate-related

impedance [236]. Extracted values of $R_g$, $R_s$, and $R_d$ remain stable over the entire frequency range with a slight decrease in $R_s$ and $R_d$ at high frequencies. This slight decrement is associated with the parallel of intrinsic capacitances and channel resistance ($R_{ch}$) [236], [240]. An average $R_g$ of 22 Ω and 28 Ω is extracted for p-MOSFET and n-MOSFET, respectively. In short channel devices, due to non-ideal effects, the total resistance ($V_{ds}/I_d$) deviates from the conventional linear dependency of drawn $l_g$ [237], [241]. The bias dependency of $R_s$ and $R_d$, as illustrated in Fig. 3.5(b), is depicted in extracted values of $R_s$ and $R_d$ in Fig. 3.7. The series resistances are considerably reduced with the increment of $|V_{gs} - V_{th}|$.

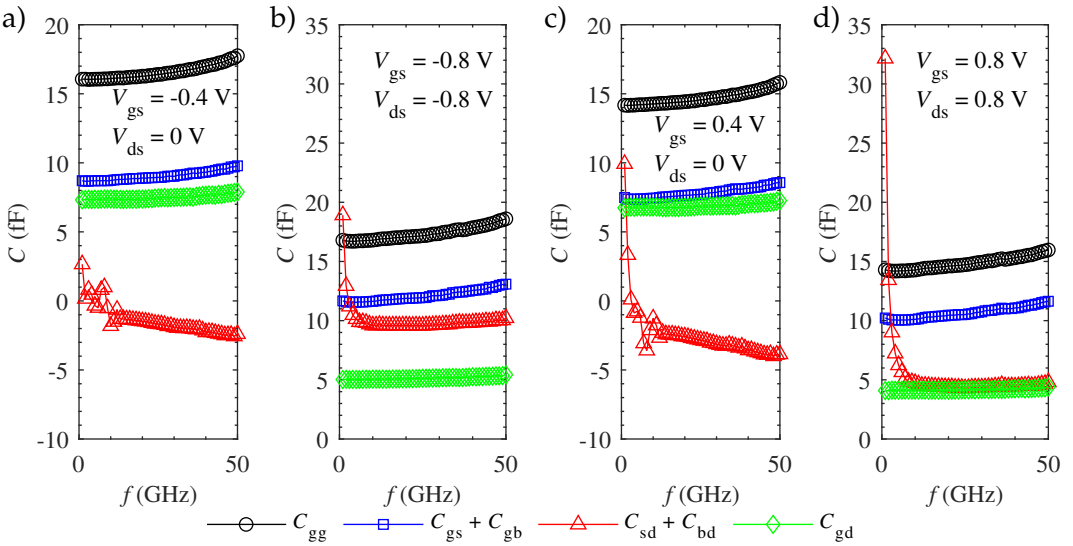


FIGURE 3.8: Small-signal model capacitances as a function of frequency extracted at (a)(c) $|V_{gs}| = 0.4$ V, $V_{ds} = 0$ V and (b)(d) $|V_{gs}| = 0.8$ V, $|V_{ds}| = 0.8$ V for (a)(b) p-MOSFET and (c)(d) n-MOSFET respectively with device dimension of $l_g = 18$ nm, $w_f = 1$ $\mu$m, and $nf = 16$.

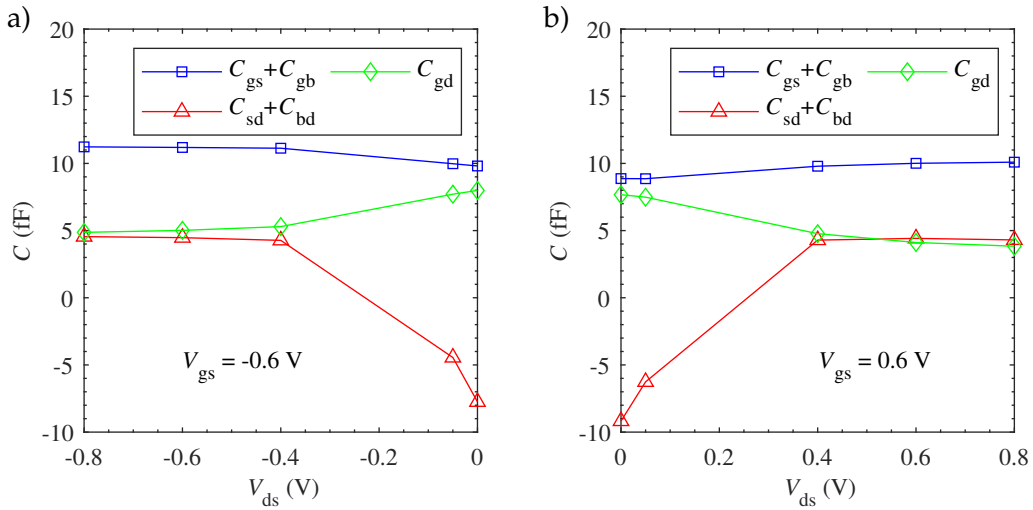


FIGURE 3.9: Drain-source bias dependency of small-signal model capacitances extracted from S-parameters at $f = 30$ GHz and $|V_{gs}| = 0.6$ V (a) p-MOSFET and (b) n-MOSFET respectively with device dimension of $l_g = 18$ nm, $w_f = 1$ $\mu$m, and $nf = 16$.

The capacitance characteristics of a MOSFET are extensively studied and modeled by the well-known Meyer model [242] and other charge-based models [243]. The Meyer model assumes the reciprocity of intrinsic capacitances ($C_{ij} = C_{ji}$), which is invalid in the case of real devices and has been addressed by charge-based models ensuring the charge conservation [244], [245]. The intrinsic capacitance between terminals of a MOSFET is defined as $C_{ij} = -\partial Q_i/\partial V_j$, where $i$ and $j$ can be any terminal of a MOSFET [246, Chapter 8]. In figure 3.8, the frequency dependence of capacitances is plotted for the cold-fet condition ($V_{ds}$ = 0V) in inversion and saturation. At $V_{ds}$ = 0V, $C_{gg} = \frac{1}{2}C_{gs} = \frac{1}{2}C_{gd}$; however, a small contribution of back-gate and substrate capacitance is included (as seen in figure 3.8(a), 3.8(c), 3.9(a), and 3.9(b)) while extracting $C_{gs}$ using 2-port configuration with source tied together with back-gate and substrate. For both n-MOSFET and p-MOSFET, the $C_{gd}$ remains almost constant for all frequencies while $C_{gs}$+$C_{gb}$ shows slight frequency dependency. This minor increment in $C_{gs}$+$C_{gb}$ with the frequency is bias independent (Fig. 3.8) and can be associated with the substrate effect. The drain bias dependence of the extracted capacitances is shown in figure 3.9. $C_{gd}$ is expressed as a change of gate charge ($Q_g$) caused by changing drain voltage ($V_d$) ($\partial Q_g/\partial V_d$) while keeping other terminals at a constant voltage. With the increase of drain bias at a fixed $V_{gs}$, the inversion layer charge will shift towards the source, resulting in a drop of $C_{gd}$ and an increase of $C_{gs}$. In saturation, $C_{gd}$ is almost equal to gate-drain overlap and fringing capacitance due to the inability of $\partial V_d$ to change $Q_g$ caused by pinch-off. In the linear region, $C_{sd}$+$C_{bd}$ becomes negative due to the inverse effect of applied $\partial V_d$ to the magnitude of inversion layer charge. To show the variation with respect to the gate bias, the extracted capacitances are plotted at fixed $V_{ds}$ in Fig. 3.10. With the increase of gate bias as the device shifts from saturation to non-saturation (i.e., $V_{ds} < V_{gs} - V_{th}$), the corresponding increase in intrinsic $C_{gs}$ and $C_{gd}$ is observed. S-parameter enables accurate characterization of such individual capacitances in a short channel device at high frequencies (GHz), which cannot be easily achieved through conventional capacitance-voltage (C-V) measurement schemes that require large C-V test structures.

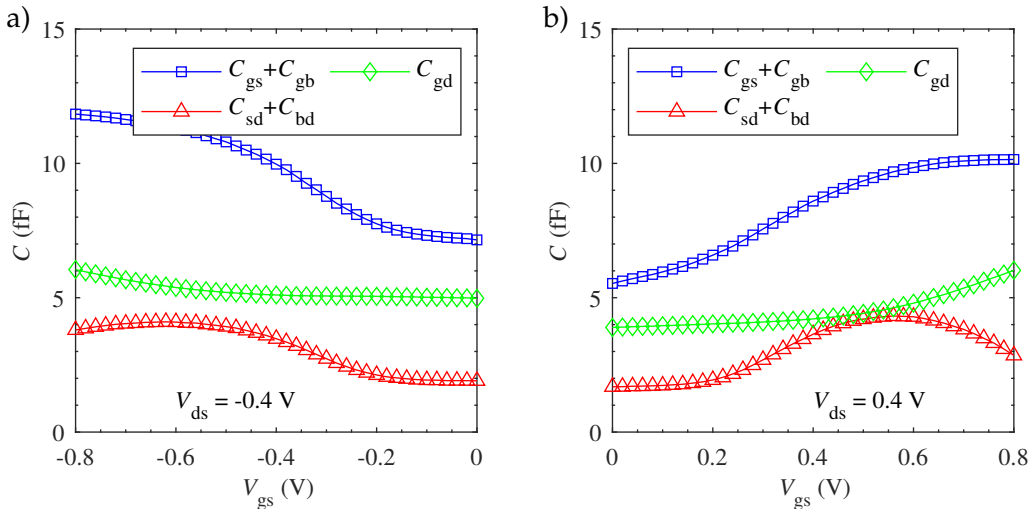


FIGURE 3.10: Extracted capacitances vs. gate-source bias obtained at $f$ = 30 GHz and $|V_{ds}|$ = 0.4 V (a) p-MOSFET and (b) n-MOSFET respectively with device dimension of $l_g$ = 18 nm, $w_f$ = 1 $\mu$m, and $nf$ = 16.

Two of the important gain parameters of a MOSFET, i.e., $g_m$ and $g_{ds}$, derived from the Y-parameters, are plotted in Fig. 3.11. $g_m$ extracted through RF measurement shows comparable values at low $V_{gs}$ and $V_{ds}$ with the one obtained from the slope of the transfer characteristics. At high $V_{gs}$ and $V_{ds}$, self-heating caused the lowering of DC extracted $g_m$. S-parameter measurements performed at high frequency do not suffer from dynamic self-heating.

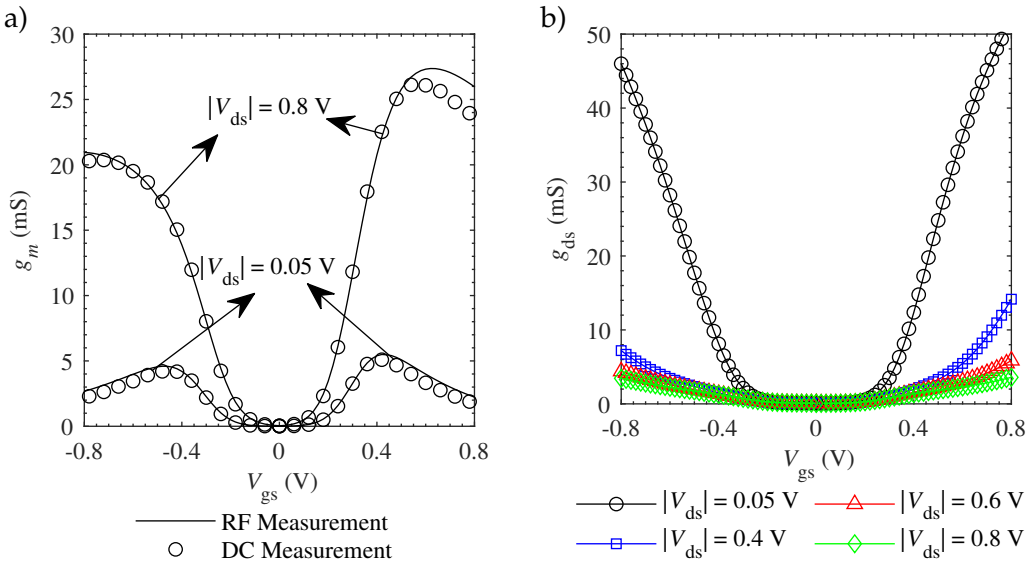


FIGURE 3.11: (a) Comparison of transconductance ($g_m$) vs. $V_{gs}$ extracted from S-parameter at $f$ = 30 GHz and DC measurements in linear ($|V_{ds}|$ = 0.05 V) and saturation ($|V_{ds}|$ = 0.8 V). (b) Output conductance ($g_{ds}$) as a function of $V_{gs}$ for various drain-source biases. The negative and positive $V_{gs}$ plots the corresponding $g_m$ and $g_{ds}$ for p-MOSFET and n-MOSFET, respectively, with device dimension of $l_g$ = 18 nm, $w_f$ = 1 $\mu$m, and $nf$ = 16.

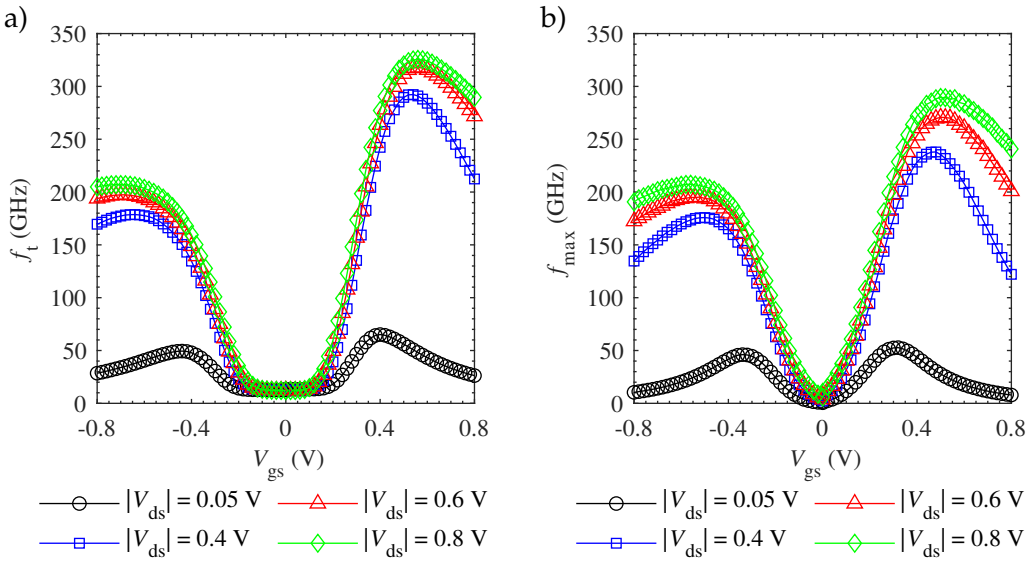


FIGURE 3.12: RF performance parameters: (a) $f_t$ and (b) $f_{max}$ as a function of $V_{gs}$ computed at $f$ = 30 GHz for multiple $V_{ds}$. The negative and positive $V_{gs}$ represents these corresponding figures of merit (FoMs) for p-MOSFET and n-MOSFET, respectively, with device dimension of $l_g$ = 18 nm, $w_f$ = 1 $\mu$m, and $nf$ = 16.

The key FoMs for the performance assessment of a transistor, i.e., $f_t$ and $f_{max}$, are plotted in figure 3.12 at various inversion levels against different $V_{ds}$. The values of $f_t$ and $f_{max}$ according to expressions 3.8 and 3.10 are a strong function of $g_m$. With an increase in $g_m$, $f_t$ and $f_{max}$ also raise to the peak values and then decline due to decreased $g_m$ caused by mobility degradation. Lower transconductance for p-MOSFET as compared to n-MOSFET reasoned in lower mobility of holes inherently affects the RF performance. The performance of n-MOSFET generally exceeds the one of p-MOSFET, and improved p-MOSFET performance is desirable. This allows a balanced n-MOSFET/p-MOSFET performance ratio, having an advantage of symmetrical circuit designs [2], [247]. The p-MOSFET in FDSOI technology features an undoped SiGe channel for improved mobility, which leads to enhanced RF performance [248]. For the experimental devices characterized in this work, the median peak values of $f_t/f_{max}$ at $|V_{ds}| = 0.8$ V are extracted as 326 GHz/290 GHz for n-MOSFET and 207 GHz/207 GHz for p-MOSFET. As the maximum of these FoMs is extracted in strong inversion, it is imperative to consider the trade-off between performance and power consumption, especially for the lower power RF applications. Other FoMs which captures the power consumption for such low power applications are defined as: $f_t(g_m/I_d)$ and $f_{max}(g_m/I_d)$ [247], [249]. The plot of these FoMs over drain current reveals the trade-off between high speed and power consumption, as shown in Fig. 3.13. The maximum values for both n-MOSFET and p-MOSFET are obtained in moderate inversion (between weak and strong inversion [250]), which serves as the optimal region for power efficiency and performance.

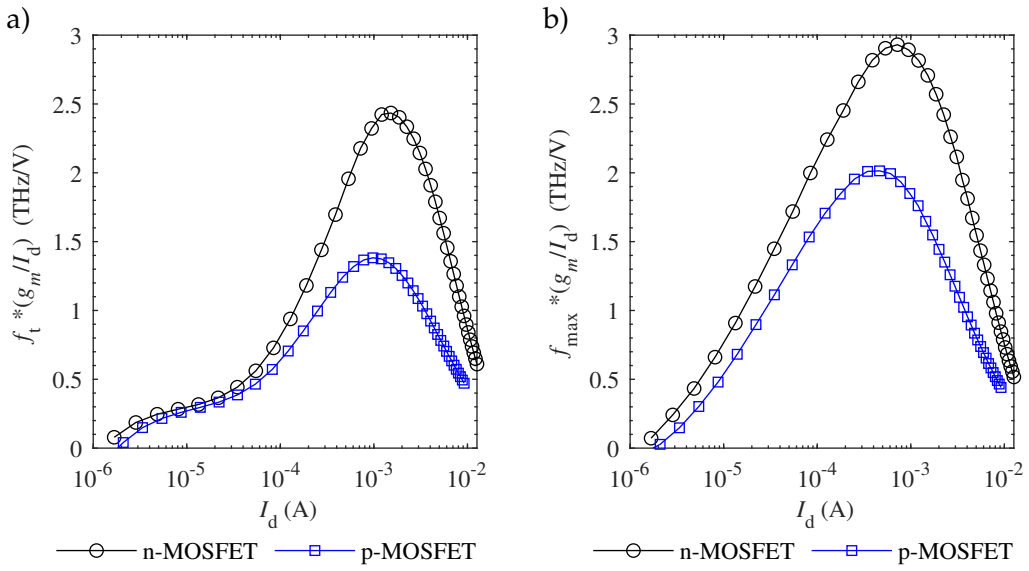


FIGURE 3.13: $g_m/I_d$ normalized RF FoMs (a) $f_t(g_m/I_d)$ and (b) $f_{max}(g_m/I_d)$ plotted vs. drain current $I_d$ extracted at $f = 30$ GHz and $|V_{ds}| = 0.8$ V for n-MOSFET and p-MOSFET with device dimension of $l_g = 18$ nm, $w_f = 1$ $\mu$m, and $nf = 16$.

# Chapter 4

# Self-heating assessment in Multi-finger Devices

As discussed in the fundamentals, self-heating in advanced semiconductor devices is an important aspect. The characterization of self-heating is essential for device design, modeling the device operation, and accurate assessment of device reliability. FDSOI having better electrostatic control of the channel region and low substrate parasitics [1], [2] features more self-heating as compared to bulk technologies [251], [252]. In FDSOI, the channel is isolated from the substrate by underneath BOX and STI from sides which hinders the dissipation of the generated heat. Materials used in BOX and STI possess much lower thermal conductivity than bulk silicon [192]. In addition to the changes caused by self-heating to intrinsic device parameters as explained in Chapter 2, several degradation mechanisms, including HCD and BTI, are a function of device temperature. Characterization of normalized thermal resistance ($R_{th}$) and thermal capacitance ($C_{th}$) enables the incorporation of self-heating effects in reliability evaluations. The temperature within the device is governed by the rate at which the heat is generated and dissipated. Along with the thermal properties of material composition, the structure of a device and its dimensions are the key factors determining the final device temperature. This chapter focuses on the extraction of thermal properties of FDSOI transistors in a multi-finger layout. Starting with a brief overview of the self-heating characterization method, the effect of varied layout parameters and design on thermal resistance is discussed. Finally, based on the extracted correlation of thermal resistance and layout parameters, an empirical model is developed. It is important to note that the aspiration behind is to investigate the self-heating effects of different layouts used in devices deployed for RF applications. As this work aims towards reliability investigation using RF characterization on RF transistors, the findings of this chapter establish the basis for the work done in succeeding chapters.

## 4.1 Self-heating Characterization Methodology

In addition to analytical and numerical models [192], [253]–[256], there exist several characterization methods to determine self-heating in semiconductor devices experimentally. These methods include optical measurements using infrared or Raman spectroscopy [257]–[259], gate thermometry where the gate resistance is serving as a temperature sensor [260]–[263], noise thermometry exploiting thermal noise of dedicated sensing structures for channel temperature extraction [206], [264], pulsed *I-V* [205], [265]–[267], and the conductance method [202], [206], [268]–[270]. In recent years the pulsed IV and conductance-based methods are

widely applied to characterize the modern ultra-scaled devices due to their superior accuracy. Generally, the pulsed *I-V* and conductance-based methods are classified as time domain and frequency domain characterization methods, respectively. In the pulsed *I-V* method, a short voltage pulse is applied to gate/drain terminals, and the respective drain current is measured. As the device needs a specific time (given by the thermal time constant ($\tau_{th}$)) to heat up, the applied voltage pulse duration should be smaller than $\tau_{th}$ to measure the self-heating free drain current. The pulsed *I-V* technique is limited by the minimum pulse width of a few tens of nanoseconds (few MHz) and the amplitude of the voltage pulses. The pulse width limitation leads to an underestimation of thermal characteristics, especially in advanced devices such as FDSOI MOSFET and FinFET, having $\tau_{th}$ below 100 ns [203]. The latter restricts the application of the pulsed *I-V* method for devices drawing a large amount of current as the pulse generator setup generally has a trade-off between pulse width and power compliance.

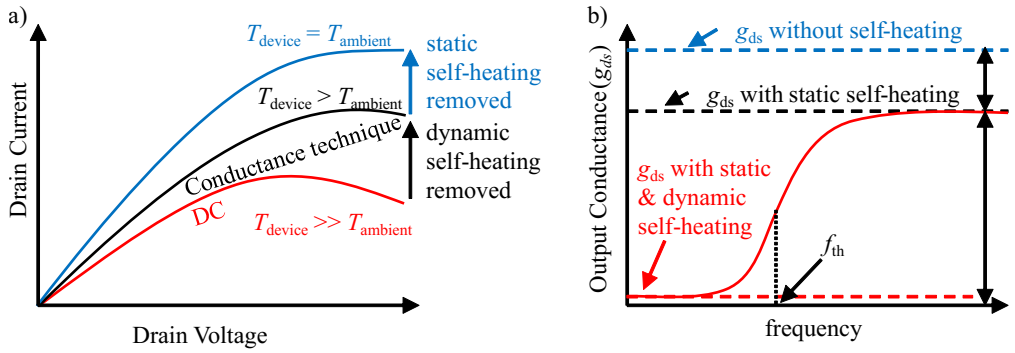


FIGURE 4.1: Graphical illustration of static and dynamic self-heating components in (a) output characteristics and (b) $g_{ds}$ behavior with respect to the frequency corresponding to the device and ambient temperature.

While the pulsed *I-V* technique assumes to achieve isothermal behavior by reducing the pulse width, a similar result is obtained in the frequency domain through the conductance-based method. The conductance-based technique assumes that the temperature within the device does not follow voltage oscillations at higher frequencies due to finite $C_{th}$ [206]. This assumption enables the extraction of thermal-related properties by measuring output conductance $g_{ds}$ at low and high frequencies. Based on the $g_{ds}$ extraction frequency, the conductance-based methods are further classified into AC and RF conductance technique. The AC conductance setup deploys an impedance analyzer for measurements limited to the maximum frequency range of several hundreds of MHz (in our case, precisely 110MHz of Agilent's 4294A). In the AC conductance technique, $g_{ds}$ is acquired by applying a small varying signal of different frequencies over a fixed drain bias. The gate bias is applied via SMU, which shares the common ground (source) with the impedance analyzer. As the frequency of the applied small-signal stimuli increases beyond $f_{th} = 1/2\pi\tau_{th}$, the device temperature ceases to follow the stimuli resulting in the elimination of dynamic self-heating. The static self-heating component would still be present due to the presence of the applied fixed bias. The static and dynamic self-heating components are depicted in fig. 4.1 in the $g_{ds}$ vs. frequency curve and the corresponding output characteristic. According to [268], the remaining static self-heating component can be determined from $\partial I_d/\partial T$, i.e., the dependence of $I_d$ on ambient $T$, obtained from a hot-chuck measurement of the drain current. Knowing the difference of $g_{ds}$ at high-frequency ($g_{ds,HF}$) and $g_{ds}$ at low-frequency

($g_{\mathrm{ds,LF}}$), $R_{th}$ is then expressed as [268]:

$$R_{th} = \frac{g_{\mathrm{ds,HF}} - g_{\mathrm{ds,LF}}}{(V_{\mathrm{ds}} g_{\mathrm{ds,HF}} + I_{\mathrm{d}}) \dfrac{\partial I_{\mathrm{d}}}{\partial T}} \tag{4.1}$$

AC conductance techniques benefit from a simple setup scheme and can be applied to available DC pad layout structures. However, its frequency limitation undermines the device's self-heating effects, where the plateau of $g_{\mathrm{ds}}$ indicates the removal of dynamic self-heating lies in the frequency range of several hundred MHz [203], [204], [269], [271]. This frequency limitation can be overcome by applying the RF technique for the measurement of $g_{\mathrm{ds}}$ at high frequencies (> 100 MHz) in state-of-the-art semiconductor technologies featuring smaller thermal time constants [195]. RF technique deploys a similar approach for the extraction of thermal characteristics utilizing S-parameters to extract the $g_{\mathrm{ds}}$, as explained in Chapter 3. The derivation of thermal impedance for a 2-port network is expressed in Y-parameters as [202]:

$$Y_{ij} = Y_{ijT} + Z_{th} \frac{\partial I_i}{\partial T} (V_1 Y_{1jT} + V_2 Y_{2jT} + I_j). \tag{4.2}$$

Where $i, j = 1, 2$ are port indices (as shown in Fig. 3.1), thermal impedance ($Z_{th}$) is a complex number whose real part represents $R_{th}$, and imaginary part represents $C_{th}$, $Y_{1jT}$, $Y_{2jT}$ are the $Y_{1j}$, $Y_{2j}$ parameters, respectively at high frequency with dynamic self-heating removed. Solving for the real part, the equation 4.2 can be written as:

$$Re(Y_{ij}) = g_{ij} = g_{ijT} + R_{th} \frac{\partial I_i}{\partial T} (V_1 g_{1jT} + V_2 g_{2jT} + I_j). \tag{4.3}$$

In the above equation 4.3, the gain parameter can be $g_m$ and $g_{\mathrm{ds}}$ ($Y_{21}$ and $Y_{22}$, respectively). However, the variation of $g_{\mathrm{ds}}$ with frequency is relatively larger as compared to the variation of $g_m$. Hence, the transition of $g_{\mathrm{ds}}$ will be considered for the extraction of $R_{th}$. Rewriting equation 4.3 for $i = j = 2$ yields

$$g_{\mathrm{ds}} = g_{\mathrm{ds,HF}} + R_{th} \frac{\partial I_{\mathrm{d}}}{\partial T} (V_{\mathrm{gs}} g_{12,HF} + V_{\mathrm{ds}} g_{\mathrm{ds}} + I_{\mathrm{d}}). \tag{4.4}$$

The reverse gain term at high frequency ($g_{12,HF}$) can be neglected as it is much smaller than $g_{\mathrm{ds}}$ which results in a similar equation to 4.1 as derived for the AC conductance technique. Similarly, the imaginary part of equation 4.2 considering $i = j = 2$ for $C_{th}$ is expressed as:

$$Im(Y_{22}) = Im(Y_{22,HF}) + Im(Z_{th}) \frac{\partial I_{\mathrm{d}}}{\partial T} (V_{\mathrm{gs}} Im(Y_{12,HF}) + V_{\mathrm{ds}} Im(Y_{22,HF}) + I_{\mathrm{d}}), \tag{4.5}$$

$$C_{th} = \frac{1}{\omega Im(Z_{th})}. \tag{4.6}$$

Finally, the average temperature rise for the device can be extracted from $R_{th}$ as:

$$\Delta T = R_{th} I_{\mathrm{d}} V_{\mathrm{ds}}. \tag{4.7}$$

### 4.1.1 Output Conductance Frequency dependence

The measurement of $g_{ds}$ is carried out in low and high-frequency bands using respective AC conductance technique and RF technique. In addition to the generic measurement setup shown in Fig. 3.2, an impedance analyzer is deployed to acquire measurement in the 40 Hz to 50 MHz range. A VNA is used for frequencies above 10 MHz, as shown in a simplified setup in Fig. 4.2.

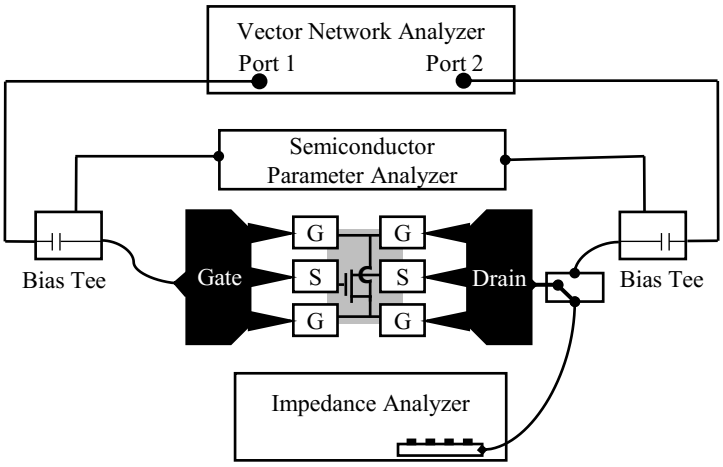


FIGURE 4.2: Experimental setup for the measurement of $g_{ds}$ on the GSG layout structures at low and high frequencies using an impedance analyzer (Agilent 4294A) and a vector network analyzer (Keysight PNA-X N5247A), respectively.

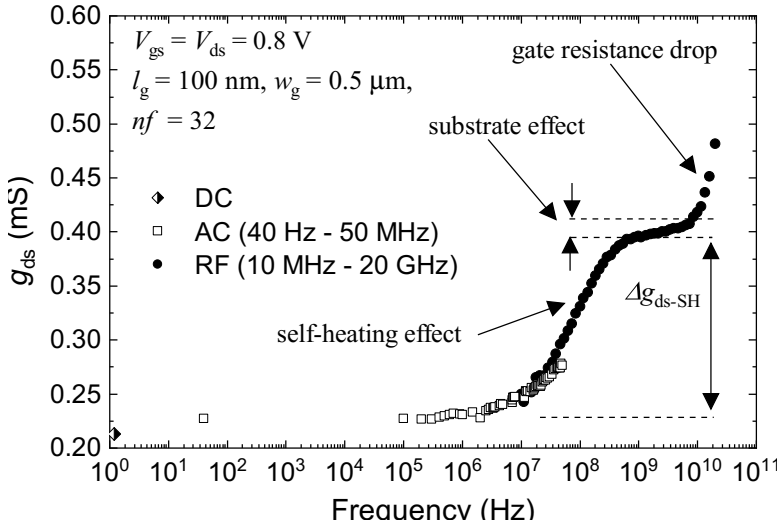


FIGURE 4.3: Plot of $g_{ds}$ vs. frequency extracted using DC IdVd characteristics, AC conductance and Y-parameters at $V_{gs} = V_{ds} = 0.8$ V for an n-MOSFET with $l_g = 100$ nm, $w_f = 0.5$ $\mu$m, and $nf = 32$.

Fig. 4.3 shows the variation of $g_{ds}$ with frequency measured using AC and RF techniques compared to $g_{ds}$ extracted from DC output characteristics. Measured $g_{ds}$ using different techniques show a good match in the overlapping frequency region. The transition of $g_{ds}$ between 1 MHz and 800 MHz resulted from the suppression of dynamic self-heating, whereas the rise between 5 GHz and ≈10 GHz is associated with the substrate effect. As shown in Fig. 4.4(a) the substrate-relate $g_{ds}$ coupling

increase with the $l_g$ reduction. Beyond 10 GHz, the rise in $g_{ds}$ is due to a reduction of the gate resistance [95]. The magnitude of $g_{ds}$ rise because of parasitic gate-resistance does not scale with respect to $l_g$. The effect of substrate coupling and gate-resistance in shorter $l_g$ devices are merged. In comparison, for the longer $l_g$ devices, the gate resistance-related $g_{ds}$ transition is noticeable due to the meager substrate-related effect. The source, back-gate, and substrate are tied together for the devices characterized in this work, minimizing the substrate-related effect in $g_{ds}$. Furthermore, a well-type ground plane under the BOX helps to decimate substrate coupling [199], [268]. Fig. 4.4(b) shows the difference and ratio of $g_{ds}$ to $g_{ds}$ at 10 Mhz. An apparent plateau where dynamic self-heating is removed can be seen around 800 MHz.

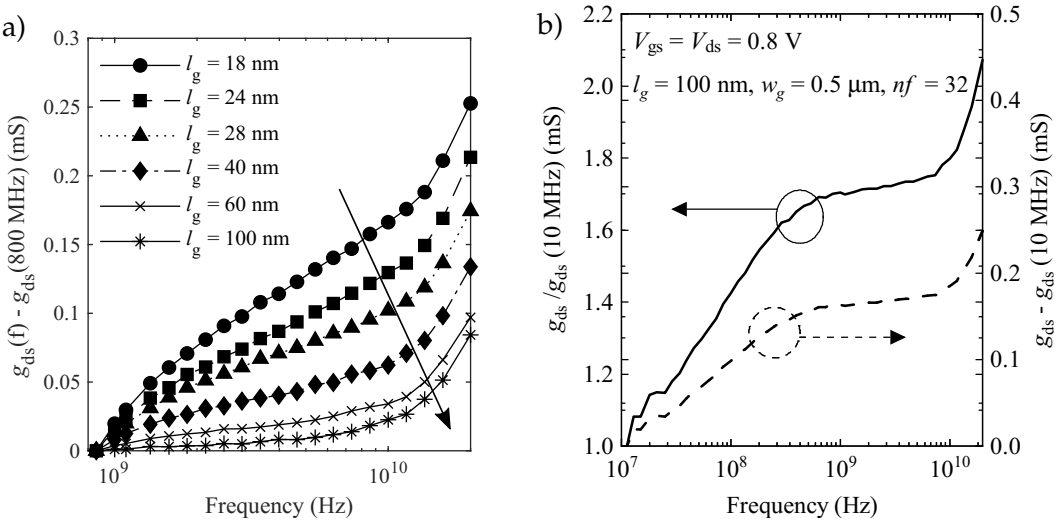


FIGURE 4.4: (a) $\Delta g_{ds}$ calculated as $g_{ds}$(f)-$g_{ds}$(800 MHz) plotted vs. frequency for different gate lengths with fixed $w_f$ = 0.5 $\mu$m, and $nf$ = 32. The arrow serves as the guide to an eye for increasing $l_g$. (b) Frequency behavior of ratio (left y-axis) and difference (right y-axis) of RF extracted $g_{ds}$ to the $g_{ds}$ @ 10 MHz at $V_{gs}$ = $V_{ds}$ = 0.8 V for an n-MOSFET with dimensions $l_g$ = 100 nm, $w_f$ = 0.5 $\mu$m, and $nf$ = 32.

### 4.1.2 Temperature dependence of Drain Current

To determine $R_{th}$ (equation 4.1) $\partial I_d/\partial T$ can be extracted from the measured output characteristics at different temperatures as shown in Fig. 4.5. The inset of Fig. 4.5 shows $\partial I_d/\partial T$ in the saturation regime for $V_{gs}$ = $V_{ds}$ = 0.8 V. $\partial I_d/\partial T$ evaluation can be performed at any biasing condition as shown in Fig. 4.6(a). However, depending on the drain current, the slope changes with the drain bias and has an almost constant value for $V_{ds}$ > 0.6 V, as shown in Fig. 4.6(b). It is important to note that the evaluation of $\partial I_d/\partial T$ should be performed at bias conditions above zero temperature coefficient (ZTC) point. ZTC is the bias point where the effect of mobility reduction and decrement of threshold voltage with increasing temperature counterbalance each other, resulting in a constant value of drain current which is independent of temperature (i.e., $\partial I_d/\partial T \approx 0$) [272], [273]. Below the ZTC point, the threshold voltage reduction effect due to an increase in temperature dominates, which leads to an increase in drain current. In contrast, above the ZTC point, the mobility degradation dominates, resulting in the reduction of drain current [274], [275]. The existence of the ZTC point is well studied in bulk [272], [276] and SOI devices [274], [277], [278].

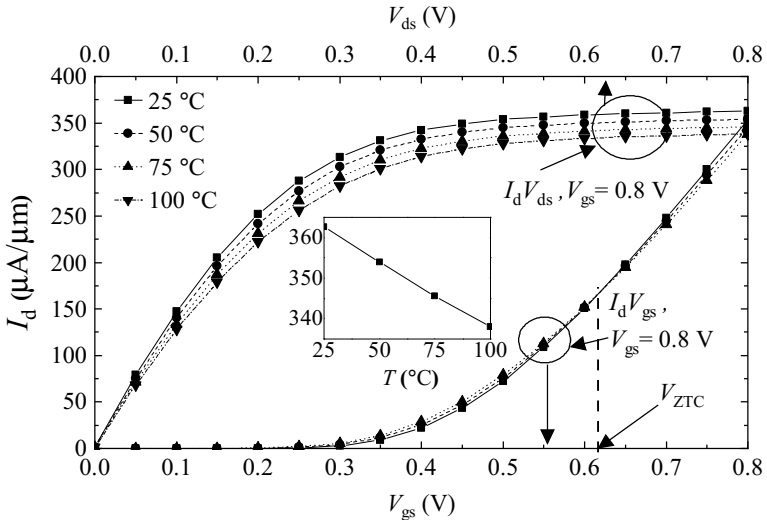


FIGURE 4.5: Transfer ($I_d V_{gs}$) and output ($I_d V_{ds}$) characteristics at different temperatures between 25 °C and 100 °C for an n-MOSFET device having $l_g$ = 100 nm, $w_f$ = 0.5 $\mu$m, and $nf$ = 32. The inset shows $I_d$ at $V_{gs}$ = $V_{ds}$ = 0.8 V as a function of temperature. The voltage where zero temperature coefficient is achieved is extracted as $V_{ZTC}$ = 0.625 V.

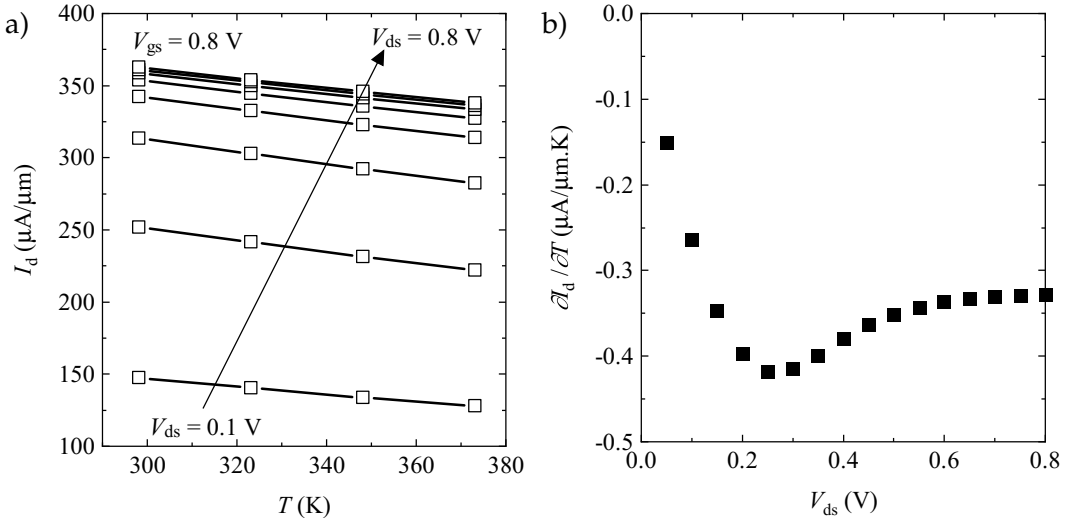


FIGURE 4.6: (a) $I_d$ as a function of temperature shown for fixed $V_{gs}$ and different $V_{ds}$ from 0.1 V to 0.8 V with the step size of 0.1 V. (b) Slope of $I_d$ vs. $T$ as a function of drain-source bias at $V_{gs}$ = 0.8 V. Data is shown for an n-MOSFET device with $l_g$ = 100 nm, $w_f$ = 0.5 µm, and $nf$ = 32.

The dependence of gate-bias at the ZTC point ($V_{ZTC}$) on applied drain bias is evident from Fig. 4.7. $V_{ZTC}$ for the linear and saturation region is determined to be 0.5 V and 0.625 V, respectively. An increase of $V_{ZTC}$ for higher drain biases is reported for the long channel bulk devices [276], while an opposite trend is reported in some PDSOI [275] and FDSOI [277] devices. $V_{ZTC} \propto 1/V_{ds}$ behavior in those devices is associated with a short channel effect, i.e., DIBL causing threshold voltage to drop at higher $V_{ds}$. The reported trend of simulated FDSOI devices in [277] does not agree with the devices [1] studied in this work and can be understood by better control of short channel effects due to the following reasons: (i) thinner $t_{BOX}$ as compared to 0.5 µm improve DIBL [279] (ii) the presence of a well-type ground plane underneath BOX minimizes DIBL [280], [281] (iii) smaller

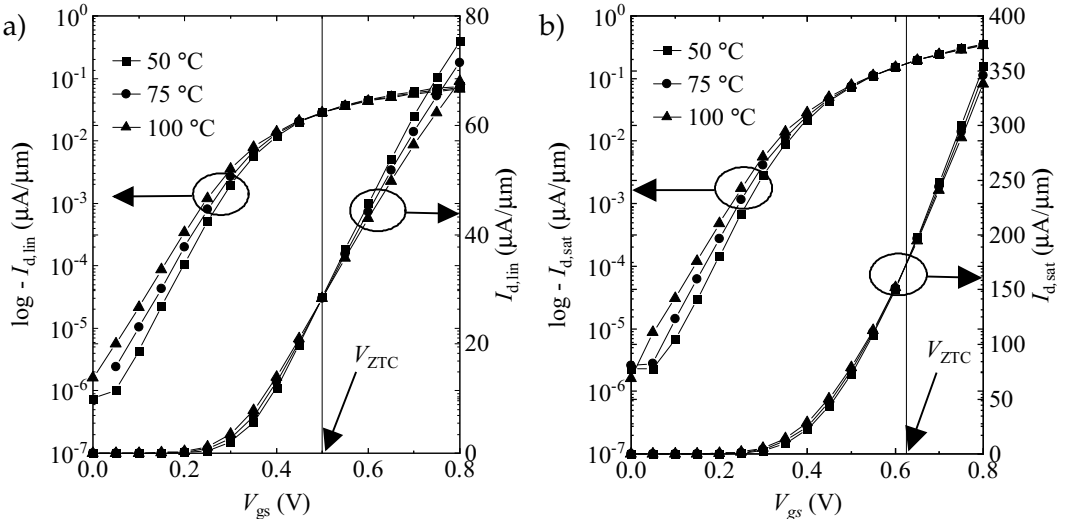


FIGURE 4.7: Transfer characteristics in log (left) and linear (right) scale for an n-MOSFET device with $l_g$ = 100 nm, $w_f$ = 0.5 µm, and $nf$ = 32. (a) $V_{ds}$ = 0.05 V and $V_{ZTC}$ = 0.5 V (b) $V_{ds}$ = 0.8 V and $V_{ZTC}$ = 0.625 V.

$t_{Si}$ of less than 7 nm as compared to 90 µm suppress short channel effects [282]. The evaluation of self-heating is done in the saturation region ($V_{gs}$ = $V_{ds}$ = 0.8 V) above the ZTC point, where mobility degradation dominates as temperatures rise and a major transition of $g_{ds}$ is observed. The self-heating effects are pronounced at such high gate and high drain bias conditions [208].

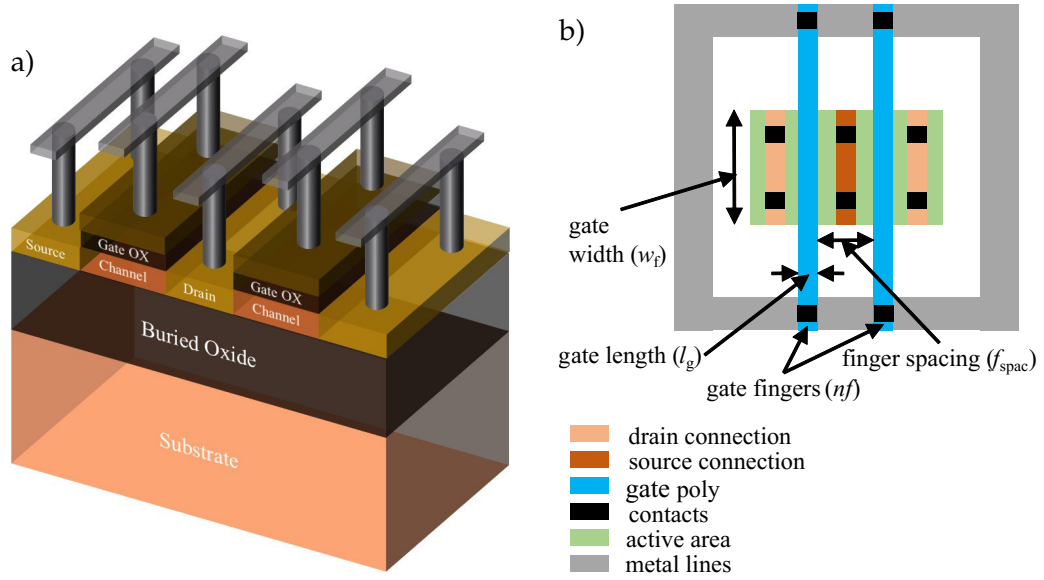


FIGURE 4.8: (a) 3D view of a 2-finger FDSOI MOSFET structure. (b) Simplified layout of a 2-finger device indicating variable dimensions for the analysis of thermal behavior.

## 4.2 Thermal Resistance Behavior

The relevance of geometrical dimensions on thermal effects has increased due to aggressive device scaling and design flexibility required to achieve robust circuit performance. Technology scaling indirectly resulted in the increase of power

density as static power dissipation becomes comparable to the main dynamic power [283], [284]. On the one hand, the thinner SOI thickness helps to reduce short channel effects but, on the other hand, degrades the thermal conductivity by considerably reducing phonon mean free path due to phonon boundary scattering [186], [285], [286]. At such nano-scale dimensions, the thermal transport is defined by the combination [287] of classical Fourier law of heat conduction [288] and Boltzmann transport equation [198], [289], [290]. The phonon mean free path in undoped bulk silicon is approximately 200-300 nm, meaning any dimension comparable or smaller encounters sub-continuum transport effects [291]. Fiegna, Yang, Sangiorgi, *et al.* in [192] reported three implications, i.e., creation of local hot-spot, hot-spot leading to an increased ratio of optical phonons concentration to acoustic phonons concentration, and film boundaries significantly reducing phonon mean free path. Therefore, it is essential to account for the dependence of device geometry and design in self-heating analysis. Fig. 4.8(a) shows a 3D view of a multi-finger device structure, and its corresponding variable layout parameters, i.e., $l_g$, $nf$, $w_f$, and spacing between fingers ($f_{spac}$), are presented in Fig. 4.8(b).

### 4.2.1 Thermal Resistance Scaling with number of fingers

It can be seen in Fig. 4.9 that the width-specific $R_{th}$ increases non-linearly with the number of fingers and then shows a nearly constant value for $nf > 50$. This is reasoned in the thermal coupling between the transistor finger. Each transistor finger behaves as a heat source for the adjacent fingers raising the device's temperature as a whole, a trend that tends to saturate for larger finger numbers. The drain and source contacts are shared among adjacent fingers in the multi-finger devices (shown with a fitted line) except for the first and last finger. Another major difference between the layout of the investigated single-finger and multi-finger device is the presence of dummy gates for single-finger devices. Hence, the presence of relatively large active area for heat dissipation in single-finger devices as shown in Fig. 6.14.

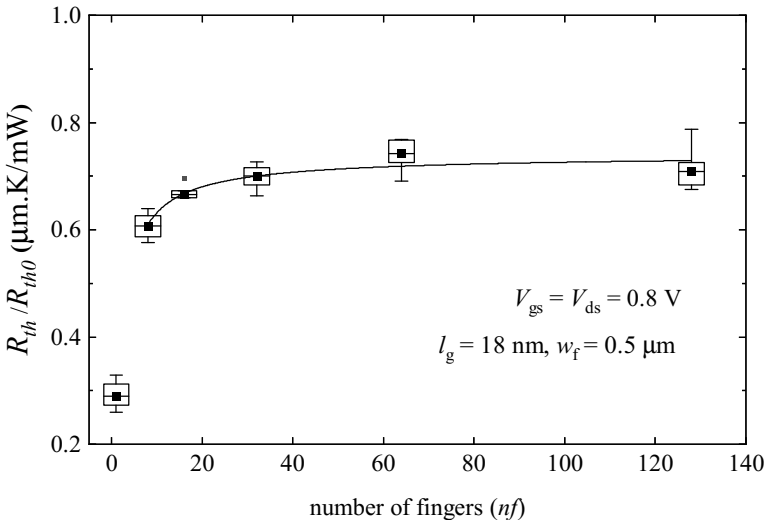


FIGURE 4.9: Box plot of thermal resistance (extracted experimentally from equation 4.1) as a function of number of finger extracted at $V_{gs} = V_{ds} = 0.8$ V for n-MOSFET with $l_g = 18$ nm, $w_f = 0.5$ $\mu$m, and $f_{spac} = 86$ nm. The line shows a non-linear fit for median data points using the expression $y = a(1 - x^{-b})$, where $a$ and $b$ are the fitting parameters. The single-finger device is omitted for the fit because of its incomparable layout with multi-finger devices.

### 4.2.2 Thermal Resistance Scaling with finger spacing

In Fig. 4.10 $R_{th}$ is observed to improve as the spacing between adjacent fingers is increased. Two aspects that play their role in the reduction of $R_{th}$: (i) Increasing $f_{\text{spac}}$ increases the source/drain regions, which contributes as a heat dissipation paths [192] (ii) Larger spacing between the adjacent fingers reduces the thermal crosstalk leading to better thermal isolation for the case of $f_{\text{spac}}$ = 190 nm while further increment does not show a similar significant drop of $R_{th}$. It is important to note that for $f_{\text{spac}}$ > 86 nm, the source and drain contacts are doubled, which aids heat dissipation and consequently improves thermal behavior. As most of the scattering events happen at the peak electric field region, a local hot-spot forms near the drain region; hence, the heat dissipation through the drain region is more effective compared to the source. The experimentally shown trends of $nf$ and $f_{\text{spac}}$ agree well with the simulations carried out in [192].

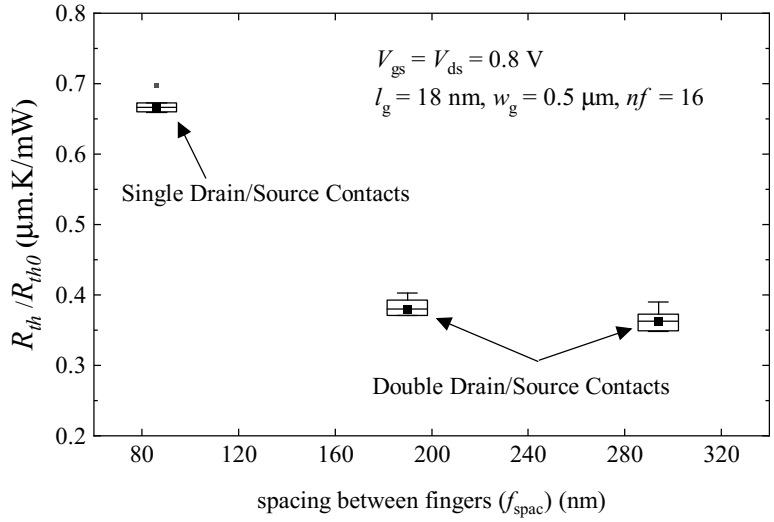


FIGURE 4.10: Plot of thermal resistance behavior with respect to spacing between adjacent fingers ($f_{\text{spac}}$) extracted at $V_{\text{gs}}$ = $V_{\text{ds}}$ = 0.8 V for n-MOSFET with $l_{\text{g}}$ = 18 nm, $nf$ = 16, and $w_{\text{f}}$ = 0.5 $\mu$m. Devices with $f_{\text{spac}}$ = 190 nm and 294 nm have double the amount of source and drain contacts as compared to devices with $f_{\text{spac}}$ = 86 nm

### 4.2.3 Thermal Resistance Scaling with Gate Width

Fig. 4.11 shows the extracted $R_{th}$ as the function of $w_{\text{f}}$. Notably, this result is contrary to the trend observed in [268], which reports linear scaling of $R_{th}$ with $1/w_{\text{g}}$. The difference could be explained by the thicker silicon of 70 nm in the simulation study reported in [268] compared to the devices studied in this work. An extended heat dissipation path can explain the increase of $R_{th}$ to the surrounding material along the width direction for larger $w_{\text{f}}$. This would confine the generated heat more effectively to the center of the channel for wider devices resulting in an overall larger self-heating. The scaling of self-heating with device width was reported in the literature for thin film transistors [292]–[294]. Cai, Chen, Du, *et al.* [295] demonstrated in simulated nano-sheet transistors with $t_{\text{Si}}$ = 5 nm: a scaling of the peak temperature with the width of the nano-sheet but a decrease in $R_{th}$ because of better heat dissipation in their structures.

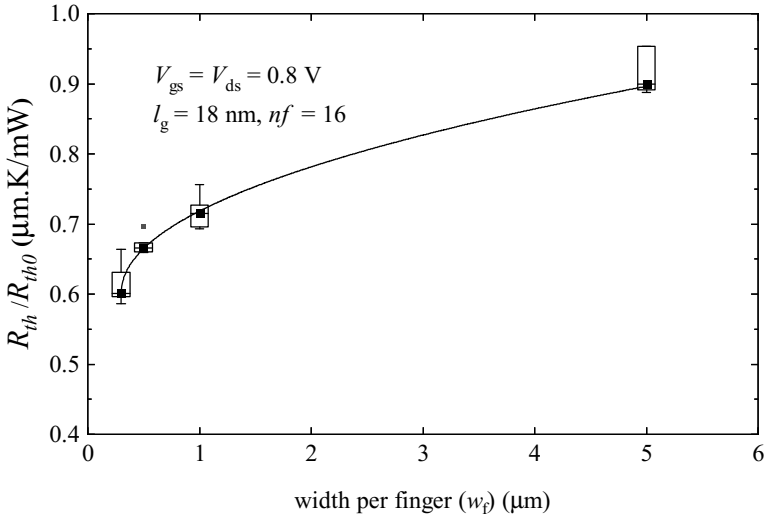


FIGURE 4.11: Thermal resistance vs. $w_f$ extracted at $V_{gs} = V_{ds}$ = 0.8 V for n-MOSFET with $l_g$ = 18 nm, $nf$ = 16, and $f_{spac}$ = 86 nm. The solid line represents the median data fitting with expression $y = A * |x - x_c|^P + y_0$, where $A$,$x_c$, $P$, and $y_0$ are the fitting parameters.

### 4.2.4 Thermal Resistance Scaling with Gate length

Due to design limitations, the gate length could not be varied in the studied structures while keeping the $f_{spac}$ constant. Therefore, Fig. 4.12 shows $R_{th}$ as a linear function of ($l_g$+$f_{spac}$). With the increase of $l_g$, $f_{spac}$ was also increased, and as shown in Fig. 4.10, a coupled effect of larger $l_g$ can be observed. Reducing the gate length translates into a confined boundary leading to a smaller phonon mean free path and generation of localized thermal hot-spots. The effect of sheer larger gate length can be seen in Fig. 4.12 inset where the total ($l_g$+$f_{spac}$) is kept constant while increasing $l_g$. $R_{th}$ remains almost constant with a slight decrease for $l_g$ = 28 nm (approx 7 µm K/mW), essentially indicating a counterbalancing effect of reduced $f_{spac}$.

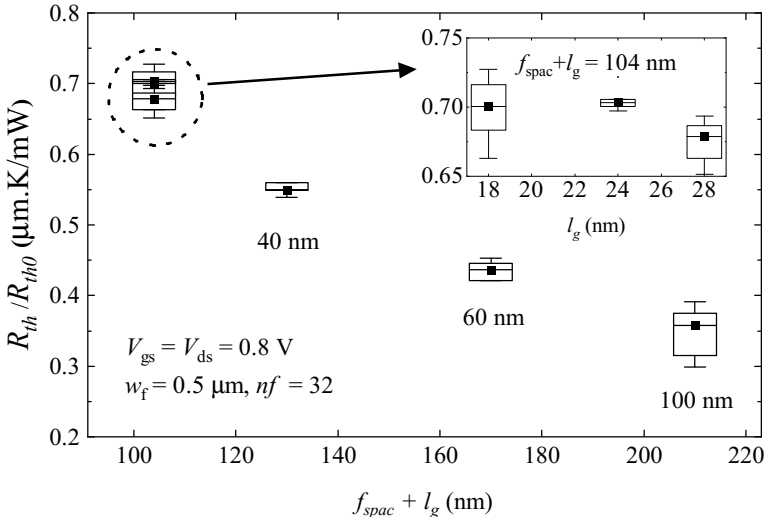


FIGURE 4.12: $R_{th}$ plotted as a function of ($f_{spac}$+$l_g$) extracted at $V_{gs} = V_{ds}$ = 0.8 V for n-MOSFET with $nf$ = 32 and $w_f$ = 0.5 $\mu$m. Data labels below the box indicate the corresponding gate length ($l_g$). The inset in the figure shows $R_{th}$ scaling with $l_g$ for the devices with constant $f_{spac}$+$l_g$ of 104 nm.

## 4.3 Thermal Resistance Model

The heat generated in the channel region is dissipated in all directions. Depending on the materials and construction of the device front-end-of-line (FEOL) and BEOL, there exist different heat conduction rates for different elements. The elements closer to the heat source, such as gate oxide, BOX, spacers, source/drain regions, play a vital role in determining the heat dissipation capability. Heat conduction path can be represented and modeled with series and parallel combination of their corresponding equivalent thermal resistance as illustrated in Fig. 4.13. By further investigating different variations and combinations of several layout parameters (see Appendix B), an empirical-based $R_{th}$ model as a function of key layout geometric dimensions is derived.

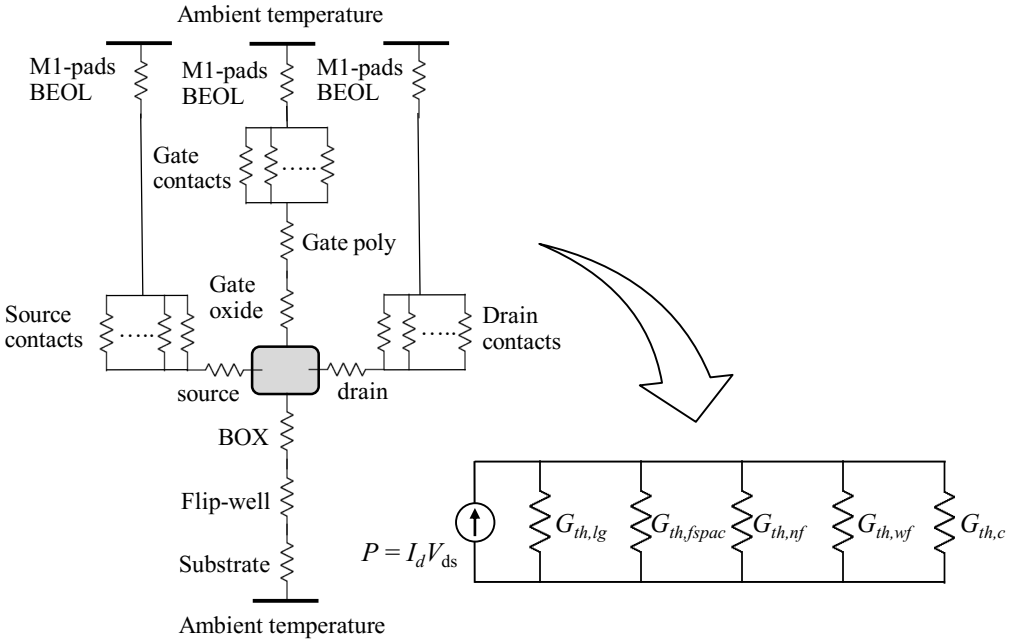


FIGURE 4.13: Thermal network for an FDSOI transistor with several elements involved in heat conduction from a heat source to the ambient temperature. Parallel resistances for gate, source, and drain contacts correspond to multi-finger layout. The equivalent resistance of M1-pads represents BEOL metal lines and vias at different levels. The equivalent electrical circuit on the bottom right represents power as a heat source and layout parameter-dependent conductances as the dissipation paths used for empirical modeling.

Considering the thermal behavior, an equivalent electrical circuit is drawn in Fig. 4.13. The following equation can represent the thermal resistance based on the equivalent circuit:

$$\frac{1}{R_{th}} = G_{th} = G_{th,lg}.l_{\mathrm{g}} + G_{th,nf}.\frac{1}{nf} + G_{th,fspac}.f_{\mathrm{spac}} + G_{th,wf}.\frac{1}{w_{\mathrm{f}}} + G_{th,c}.c \tag{4.8}$$

where $G_{th,lg}$, $G_{th,fspac}$, $G_{th,nf}$, $G_{th,wf}$, and $G_{th,c}$, are the gate length, finger spacing, number of fingers, gate width, drain/source contacts dependent thermal conductance factors, and $c$ is the ratio of source/drain contact area to source and drain region area. In the derived thermal model following considerations are made:

(i) the heat dissipation through the source and drain regions is not segregated and assumed to share an equal contribution, (ii) the factor of finger spacing and source/drain region is coupled in $G_{th,fspac}$. These layout-dependent thermal conductance components are extracted through regression analysis. An optimized fitting is achieved between the model and experimental data using the extracted conductance factors, as shown in Fig. 4.14. The maximum standard deviation of 5.4 % is observed for the variable $f_{\text{spac}}$. The standard deviation of the other modeled variables is less than 3 %. For instance, the device with dimensions $l_{\text{g}}$ = 18 nm, $nf$ = 16, $f_{\text{spac}}$ = 86 nm, and $w_{\text{f}}$ = 0.5 $\mu$m, have individual conductance contributions of 18%, 6%, 48%, 25%, and 3% respectively (according to equation 4.8). The source/drain area is observed to have the most considerable effect on thermal conductance. In the studied structures, the source/drain contacts variation is not systematic, resulting in the erroneous extraction of the contribution ratio of source/drain region and source/drain contacts. However, it can be concluded that the primary thermal conduction contribution lies within the source/drain region area and contact parameters.

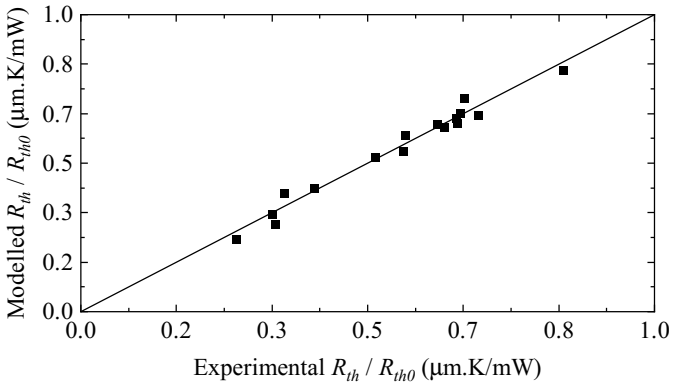


FIGURE 4.14: Rth extracted from model vs. experimentally measured data. The straight line shows the ideal behavior with a slope of 1.

## 4.4 Design for Thermal Resistance Optimization

To improve the thermal performance, two different design variations are considered, as depicted in Fig. 4.15. In the first variation (Fig. 4.15 (a), (b), and (c)), an active area is divided into separate islands of the active area along the direction of device width. Segmentation of total width into smaller width can decrease the thermal resistance due to width effect as seen in Fig. 4.11 and larger device footprint resulting in larger heat dissipation region. The active area islands are represented by number of repetitions along gate poly line (NREP). Having more NREP shown to have better RF performance by reducing the effective gate resistance, [82], [296] at the cost of the size of the layout. In a second design variation (Fig. 4.15 (d), (e), and (f)), the device footprint is kept constant while further slicing the active area into smaller slices of individual active area island width ($w_{\text{rx}}$) and (number of active area slices (NRX)) with reduced total effective width ($w_{\text{eff}}$).

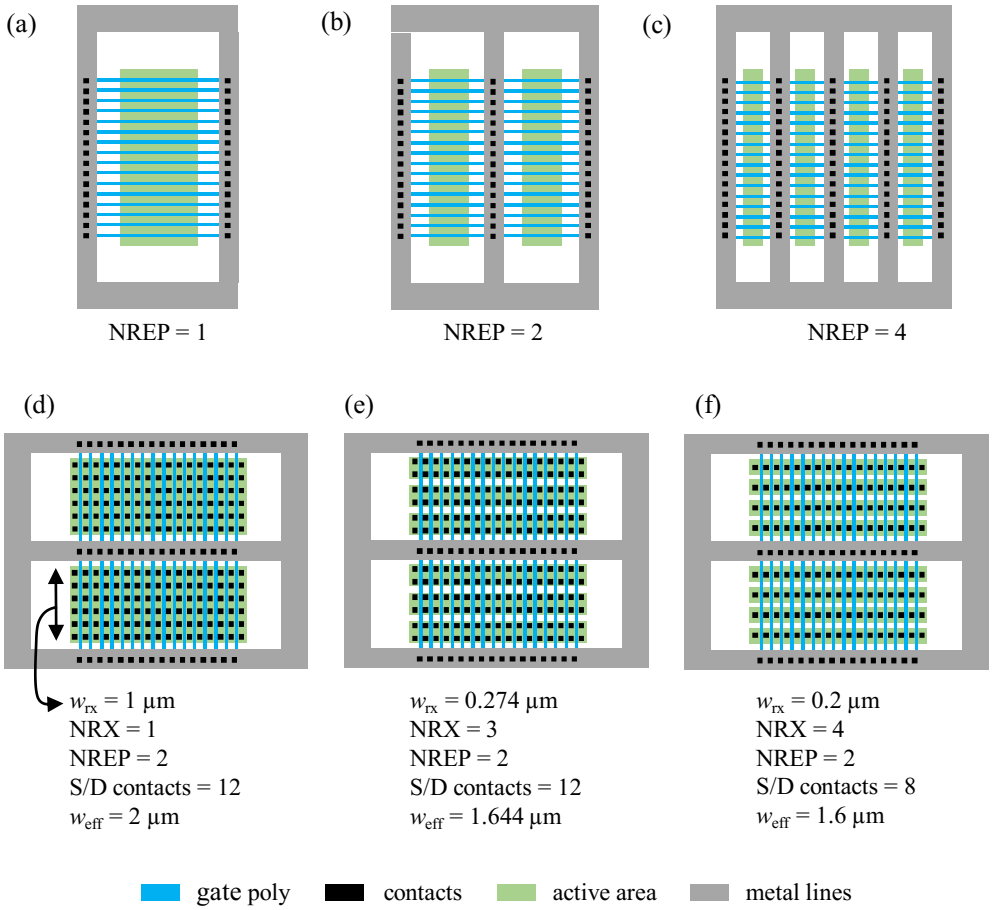


FIGURE 4.15: Layout Design variations for optimization of thermal performance. (a - c) shows NREP structures with multiple active areas having the same total effective width, referred to as folded gate structures. (d - f) shows structures with the sliced active area and same footprint having $w_{\text{eff}} = NRX * NREP * w_{\text{rx}}$

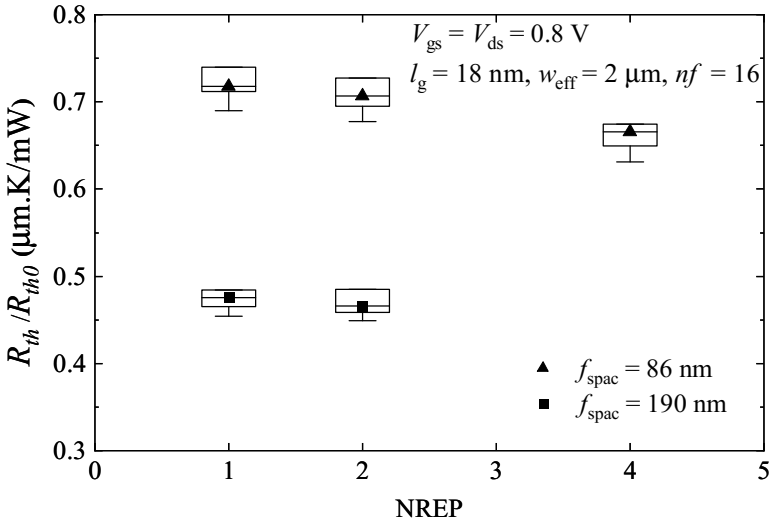


FIGURE 4.16: $R_{th}$ extracted experimentally from equation 4.1 is plotted for different NREP structures (4.15 (a), (b), and (c)) with two different $f_{\text{spac}}$ extracted at $V_{\text{gs}} = V_{\text{ds}} = 0.8$ V for n-MOSFET having dimensions $l_{\text{g}} = 18$ nm, $nf = 16$, and $w_{\text{eff}} = 2$ $\mu$m.

Fig. 4.16 shows the improved and nearly linear scaling of $R_{th}$ for the NREP structures. The structure having NREP = 4 exhibits a 7.8% lower $R_{th}$ compared to the reference structure. Because of the reduction in the effective width of a single active area island, the heat dissipation capability is enhanced along the width. With almost doubling the $f_{\text{spac}}$, $R_{th}$ is reduced significantly to $\approx 2/3$. The improvement of thermal performance in NREP structures can be associated with reducing effective width per active area. The derived model and equivalent $R_{th}$ values are extracted for corresponding widths and summarized in Table 4.1. Examining the change in thermal resistance with reference structure (NREP = 1), the measured values show less reduction of thermal resistance as compared to the reduction predicted by derived $R_{th}$ model (4.8) using equivalent $w_{\text{f}}$ of single active area island. This implies that the improvement of $R_{th}$ in NREP structures is not entirely a width reduction effect but also involves the contribution of the STI region in between the active area islands. However, NREP structures can be deployed to improve thermal performance while keeping the width constant, especially with a combination of larger $f_{\text{spac}}$.

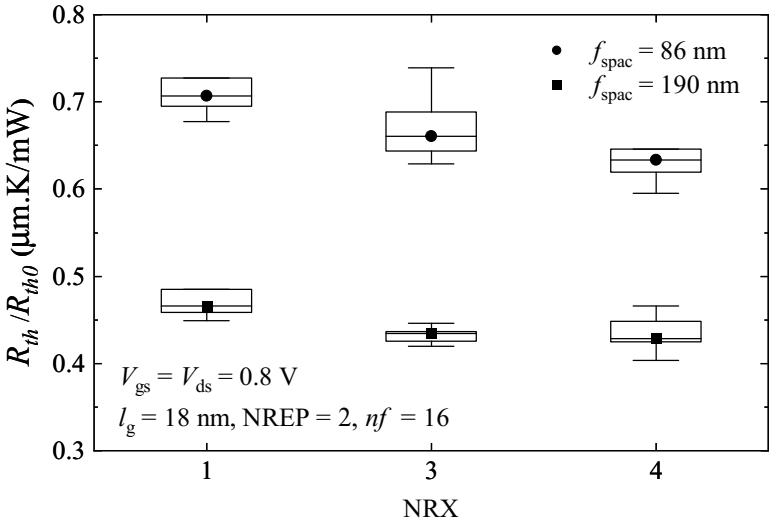


FIGURE 4.17: Thermal resistance variation for NRX structures (4.15 (d), (e), and (f)) with two different $f_{\text{spac}}$ extracted at $V_{\text{gs}} = V_{\text{ds}} = 0.8$ V for n-MOSFET with $l_{\text{g}} = 18$ nm, NREP = 2, and $nf = 16$.

Measured thermal resistance for the NRX structures is shown in Fig. 4.17. Devices with $f_{\text{spac}} = 86$ nm exhibits prominent scaling for more NRX, and the effect seems to be relatively fade for $f_{\text{spac}} = 190$ nm (also summarized in Table 4.1). Model extracted change in $R_{th}$ for the same $w_{\text{eff}}$ is smaller in comparison with the measured $R_{th}$ change for more NRX (see Table 4.1). The findings reveal that the thermal resistance reduction in NRX structures is not merely a reduced effective width effect. A decreased ratio of the active area to the device's total footprint also contributes towards better thermal performance.

TABLE 4.1: Comparison of respective change in $R_{th}$ observed in measured against modeled values using equivalent width for the evaluation of layout design effects.

| $f_{\text{spac}}$ (nm) | **NREP** | $R_{th}/R_{th0}$ (µmK/mW) Measured | Δ(%) | $w_{\text{f}}$ (µm) | $R_{th}/R_{th0}$ (µmK/mW) Modeled | Δ(%) |
|---|---|---|---|---|---|---|
| | 1 | 0.720 | 0 | 2 | 0.735 | 0 |
| 86 | 2 | 0.708 | -1.69 | 1 | 0.674 | -8.31 |
| | 4 | 0.667 | -7.34 | 0.5 | 0.576 | -21.66 |
| | 1 | 0.474 | 0 | 2 | 0.492 | 0 |
| 190 | 2 | 0.467 | -1.51 | 1 | 0.470 | -4.50 |

| $f_{\text{spac}}$ (nm) | **NRX** | $R_{th}/R_{th0}$ (µmK/mW) Measured | Δ(%) | $w_{\text{f}}$ (µm) | $R_{th}/R_{th0}$ (µmK/mW) Modeled | Δ(%) |
|---|---|---|---|---|---|---|
| | 1 | 0.708 | 0 | 2 | 0.735 | 0 |
| 86 | 3 | 0.661 | -6.60 | 1.644 | 0.721 | -1.89 |
| | 4 | 0.634 | -10.45 | 1.6 | 0.719 | -2.19 |
| | 1 | 0.467 | 0 | 2 | 0.492 | 0 |
| 190 | 3 | 0.435 | -6.83 | 1.644 | 0.487 | -1.02 |
| | 4 | 0.429 | -8.15 | 1.6 | 0.486 | -1.16 |

# Chapter 5

# Bias Temperature Instability Investigation

BTI continues to be one of the most crucial degradation mechanisms in modern metal-oxide-semiconductor devices striving for robust performance under stringent biasing and increased operating temperatures [162]. As mentioned in Chapter 2, the phenomenon itself is known since the late 1960s [297] and gained central attention as a result of aggressive scaling of gate oxide thickness. Various factors, including semiconductor processing steps, gate dielectrics, and channel materials, determine the severity and dependence of BTI. The degradation in MOSFET due to BTI stress is commonly described as the shift of $I_{\mathrm{d}}$, $V_{\mathrm{th}}$, SS, and peak transconductance ($g_{m,\mathrm{max}}$) with respect to the stress time [298]. The physical mechanisms involving the degradation effects and their corresponding impact on such DC parameters are well reported in thousands of articles over several decades [165]. However, the BTI effects on the small-signal behavior of RF MOSFET are yet to be explored. The assessment of BTI effects under the transistor's dynamic and high-frequency operation is necessary for the complete understanding and modeling of small-signal behavior subjected to various modes of stress. In this chapter, the impact of BTI stress on small-signal parameters of FDSOI MOSFET is discussed in the first section and followed up with the introduction and implementation of a new BTI characterization technique exploiting S-parameters.

## 5.1 Impact of Bias Temperature Instability stress on Device Metrics

### 5.1.1 Experimental Details

Several multi-finger n-MOSFETs and p-MOSFETs are subjected to the PBTI and NBTI stress sequence as shown in Fig. 5.1. Three different stress voltage ($V_{\mathrm{stress}}$) (see the table in Fig. 5.1) are applied and referred to as stress A, B, and C in the following text. A test setup shown in Fig. 3.2 is utilized for stressing and S-parameter measurement. The measurement of BTI effects requires fast measurement techniques as BTI constitutes a recoverable component (R) and a permanent component (P). According to some reports, P is shown to be healed at high temperatures [299] with a very large timescale [166] and termed as quasi-permanent [165]. However, P can be significantly detrimental to the device performance and lifetime for extended time scales, depending on the operating conditions [166], [179]. Usually, in a BTI measurement setup, the fast DC measurement techniques are employed to ensure a capturing of R. However, S-parameter measurements at multiple frequencies and bias conditions via a VNA

are necessary for complete small-signal analysis requires more than milliseconds [300], while the BTI recovery time for modern devices is in the ranges of just a few microseconds [174]. Thus, R cannot be characterized if S-parameter measurements are performed by interrupting stress. However, this should not obstruct and limit the characterization of P in terms of S-parameters. Hence, the S-parameters were measured before and after stress in combination with fast spot DC measurements during the stress, as illustrated in Fig. 5.1. To characterize P, the post-stress measurement was performed after the recovery of more than 12 hours at room temperature. It is important to note that a recovery time of 12 hours might not reflect a true permanent BTI degradation component as the recovery is not tracked throughout the relaxation time, and a plateau is not ascertained. Nevertheless, an effort to investigate BTI effects on small-signal parameters is not futile and can provide corresponding insights to the mixed degradation components. S-parameters for various bias points and frequencies in the range of 1 GHz to 50 GHz are acquired using the procedure described in section 3.2.

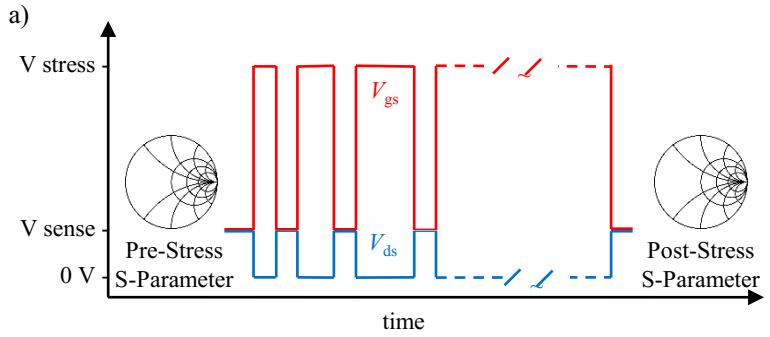


FIGURE 5.1: (a) BTI stress scheme with S-parameter measurements before and after stress. (b) The table lists the stress voltages of PBTI and NBTI for n-MOSFET and p-MOSFET, respectively.

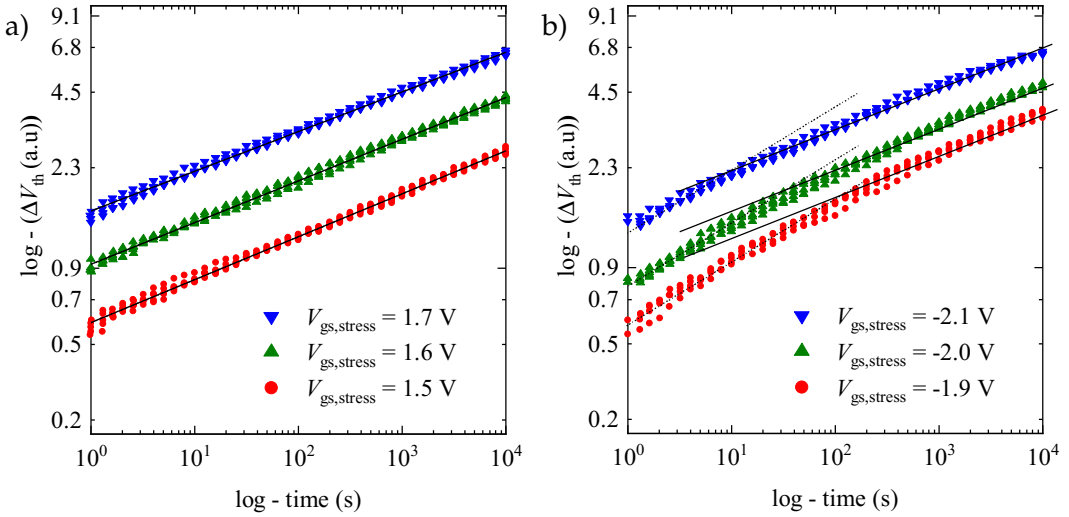


FIGURE 5.2: $V_{th}$ degradation as a function of stress time for (a) n-MOSFET and (b) p-MOSFET. The line shows the fitting of data at different stress voltages. The dotted line in (b) fits the $V_{th}$ degradation for lower stress times. Five devices are measured for each stress condition.

### 5.1.2 DC Parameters Drift

It is well known in the literature that the affected parameters due to BTI stress are linear drain current ($I_{d,lin}$), saturation drain current ($I_{d,sat}$), $V_{th}$, $\mu_{eff}$, and SS [163]. Due to BTI stress, electrons trapping for n-MOSFET and holes trapping for p-MOSFET result in the increase of $V_{th}$, as shown in Fig. 5.2. The time ($t$) resolved degradation can be modeled by the frequently used power law [163]. The $V_{th}$ degradation of the n-MOSFET exhibits a constant slope, while for p-MOSFET saturation effect is observed for longer stress time. The change in slope for NBTI stress in p-MOSFET is due to the nature of defects and their dependence on $V_{stress}$ and time. The interface defects (generated traps at the $Si/SiO_2$ interface) dominate at lower $V_{stress}$ and time, whereas the component of oxide defects (generated border traps) becomes significant for higher $V_{stress}$ and time [165], [167].

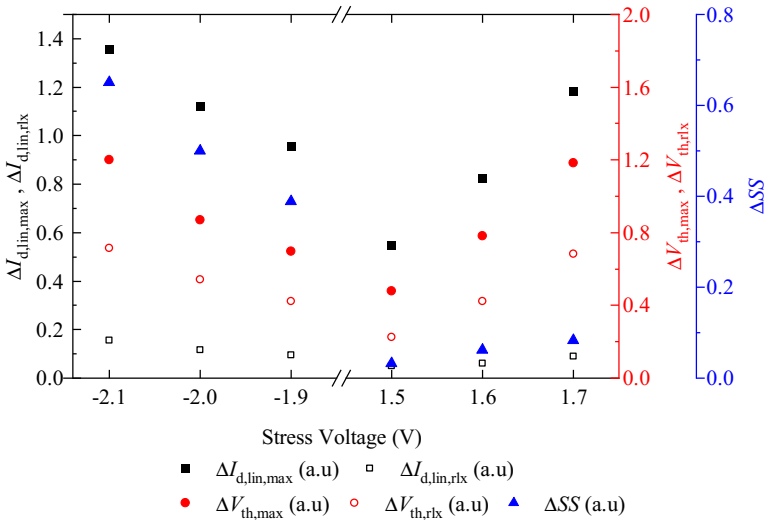


FIGURE 5.3: DC parameters degradation plotted for different stress voltage after 10,000 s of BTI stress. Absolute values are shown in this plot. The black square, red circle, and blue triangle markers represent the $I_{d,lin}$, $V_{th}$, and SS degradation, respectively. The color of markers is linked to the color of the y-axis. The subscript "max" and "rlx" represent R+P (solid markers) and P (hollow markers) components of the degradation, respectively. After stress, $I_{d,lin}$, and SS are decreased while $V_{th}$ is increased.

Fig. 5.3 shows the change in DC parameters as a function of $V_{stress}$ after BTI stress. The higher the applied $V_{stress}$, the larger the number of defects leading to a larger drift in DC parameters. The component P after a significant recovery in DC parameters, is depicted in Fig. 5.3 with hollow markers and subscript "rlx". Compared to PBTI, NBTI stress leads to a stronger increase in SS. This implies that the degradation in p-MOSFET is due to both oxide and interface defects [301], while for n-MOSFET, the defects are dominantly in the oxide [302].

### 5.1.3 RF Small-Signal Parameters Drift

From the measured S-parameters before and after BTI stress, the effect of P on the components of the small-signal equivalent model is analyzed. Fig. 5.4 emphasizes that depending on the bias point, the apparent normalized change in small-signal parameters with respect to $\Delta V_{th}$ projects a different magnitude of drift. It is important to note that the devices' and circuits' operating conditions would determine the sensitivity to BTI degradation.

Fig. 5.5(a) shows the $g_m$ lateral shift due to $\Delta V_{\text{th}}$. If corrected for $\Delta V_{\text{th}}$, i.e., for the same bias point, it becomes evident that a large portion of the $g_m$ drift can be explained only by the $V_{\text{th}}$ shift, as shown in Fig. 5.5(b). However, when enlarging the scale, the $g_{m,\text{max}}$ in the case of NBTI degrades due to interface defects implying $\mu_{\text{eff}}$ degradation as depicted in the inset of Fig. 5.5(b). For PBTI, a scattered and slightly positive $g_{m,\text{max}}$ increment is observed. Similarly, the other gain parameter $g_{\text{ds}}$ also exhibit a bias dependent parallel shift and slight peak $g_{\text{ds}}$ degradation for the case of NBTI (Fig. 5.6). $C_{\text{gg}}$ equates to the sum of $C_{\text{gs}}$, $C_{\text{gd}}$, and $C_{\text{gb}}$. Each of these gate capacitance components (except $C_{\text{gb}}$) suffers from a bias-dependent lateral shift of $\Delta V_{\text{th}}$ (Fig. 5.7 and Fig. 5.8) and can be compensated by bias point correction. $C_{\text{gd}}$ at higher drain bias shows weaker gate bias dependence due to channel pinch-off (miller capacitance component); thus, the apparent lateral change resulting from BTI in such operating conditions becomes insignificant. Hence the capacitance changes are shown at $V_{\text{ds}} = 0.05$ V, where the channel is almost uniform at all gate bias conditions, and the corresponding contribution of both gate capacitance elements are visible. $\Delta V_{\text{th}}$ also affected the dominant bias-dependent component $R_{\text{ac}}$ of series $R_{\text{s}}$ and $R_{\text{d}}$ extracted in cold FET condition with a fully open gate. The apparent shift in series resistances is symmetric between source and drain; however, larger due to NBTI stress, as shown in Fig. 5.9. The difference of resultant bias-dependent series resistance change between NBTI and PBTI is associated with the respective sensitivity of series resistance to biasing, as shown in Fig. 3.7. In Fig. 5.10 and 5.11, the as measured and $\Delta V_{\text{th}}$ corrected key FoMs $f_{\text{t}}$ and $f_{\text{max}}$ after the BTI stress are shown. The changes in both FoMs are mainly associated with $\Delta g_m$. $\Delta g_{m,\text{max}}$, and $\Delta V_{\text{th}}$. The parameter $\Delta V_{\text{th}}$ is widely used for modeling BTI degradation and can be used to predict the change in small-signal RF parameters. The scaling of drift with the stress voltage in most of the RF small-signal extracted parameters for PBTI and NBTI is not comparable and reasoned in the voltage acceleration factor of p-MOSFET and n-MOSFET. BTI stress does not affect the frequency-dependent behavior of small-signal parameters, as evident from the $V_{\text{th}}$ compensated plots. Thus, the degradation in S-parameters caused by BTI stress can be directly linked to the degradation of purely DC parameters.

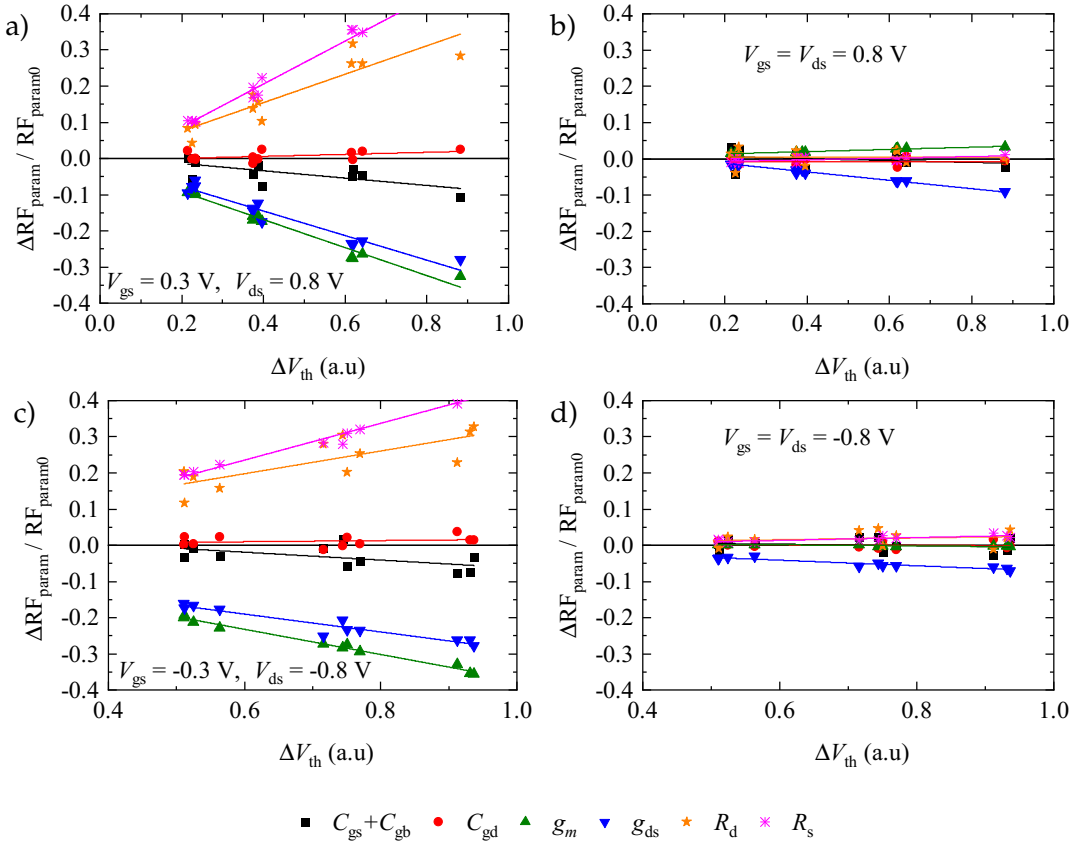


FIGURE 5.4: Apparent drift in small-signal parameters after BTI stress extracted at $f$ = 30 GHz for bias condition of (a)(c) $|V_{gs}|$ = 0.3 V, $|V_{ds}|$ = 0.3 V (b)(d) $|V_{gs}|$ = $|V_{ds}|$ = 0.8 V for (a)(b) n-MOSFET and (c)(d) p-MOSFET with device dimensions $l_g$ = 18 nm, $w_f$ = 1 µm, and $nf$ = 16.

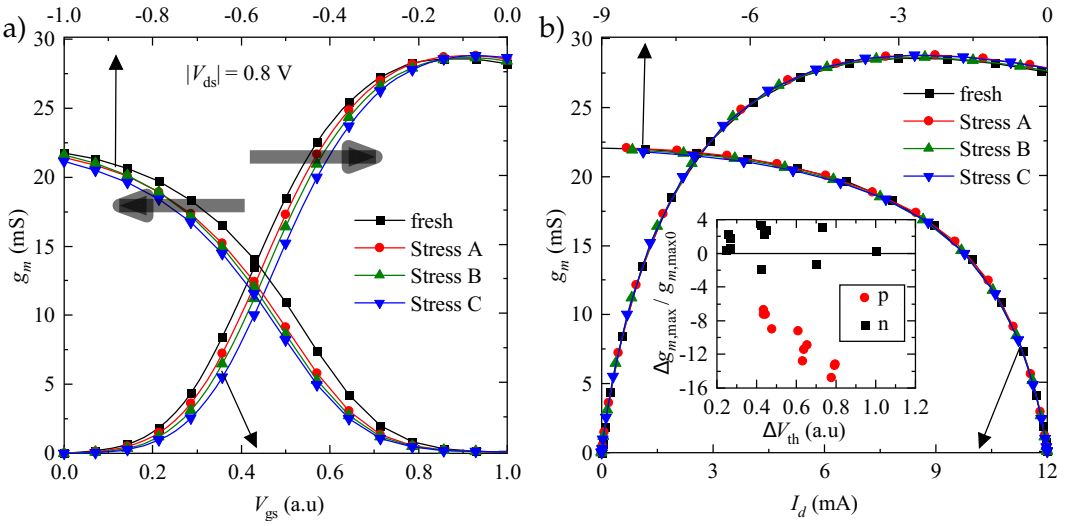


FIGURE 5.5: (a) $g_m$ vs. $V_{gs}$ extracted at $f$ = 30 GHz at $|V_{ds}|$ = 0.8 V for the fresh and stressed devices subjected to stress A, B, and C as defined in the table of Fig. 5.1(b). (b) $g_m$ vs. $I_d$ plot showing $V_{th}$ correction validity. Inset in (b) shows $g_{m,max}$ degradation. The bottom and top x-axis represents values for (a) $V_{gs}$ (b) $I_d$ for an n-MOSFET and p-MOSFET, respectively.

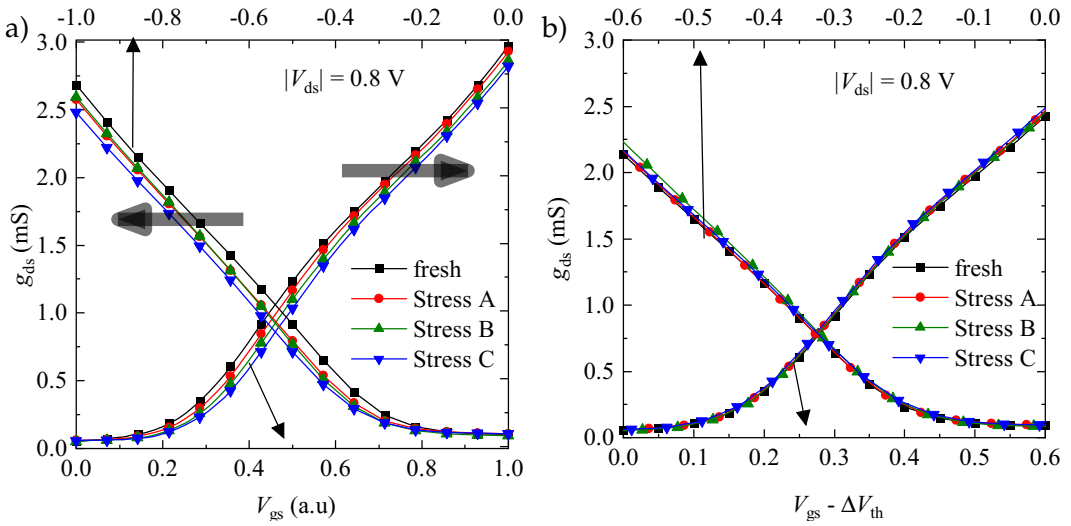


FIGURE 5.6: (a) $g_{ds}$ vs. $V_{gs}$ extracted at $f$ = 30 GHz at $|V_{ds}|$ = 0.8 V for fresh and stressed devices subjected to stress A, B, and C as defined in the table of Fig. 5.1(b). (b) The plot of $g_{ds}$ vs.$V_{gs}$ corrected for $V_{th}$ shift (due to BTI stress) showing compensation of $\Delta g_{ds}$ under all stress conditions. The bottom and top x-axis represents values for (a) $V_{gs}$ (b) $V_{gs} - \Delta V_{th}$ for an n-MOSFET and p-MOSFET, respectively.

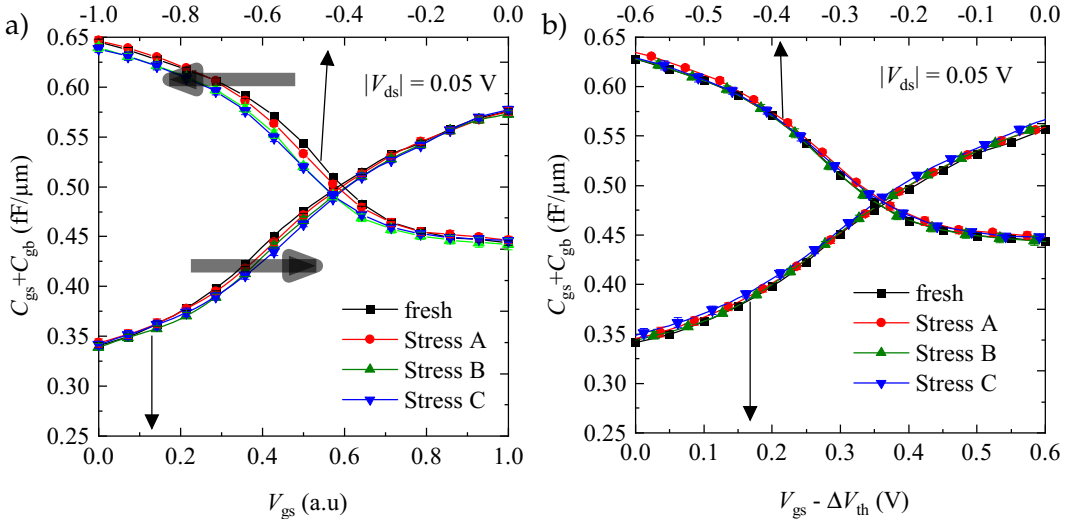


FIGURE 5.7: Changes in gate-source capacitance with respect to gate bias at $f$ = 30 GHz and $|V_{ds}|$ = 0.05 V for fresh and stressed devices. (a) Plotted as a function of $V_{gs}$ and (b) $V_{gs}$ corrected for $V_{th}$ shift due to BTI stress. The substrate (back-gate) capacitance component $C_{gb}$ is not affected by the stress. The bottom and top x-axis represents values for (a) $V_{gs}$ (b) $V_{gs} - \Delta V_{th}$ for an n-MOSFET and p-MOSFET, respectively.

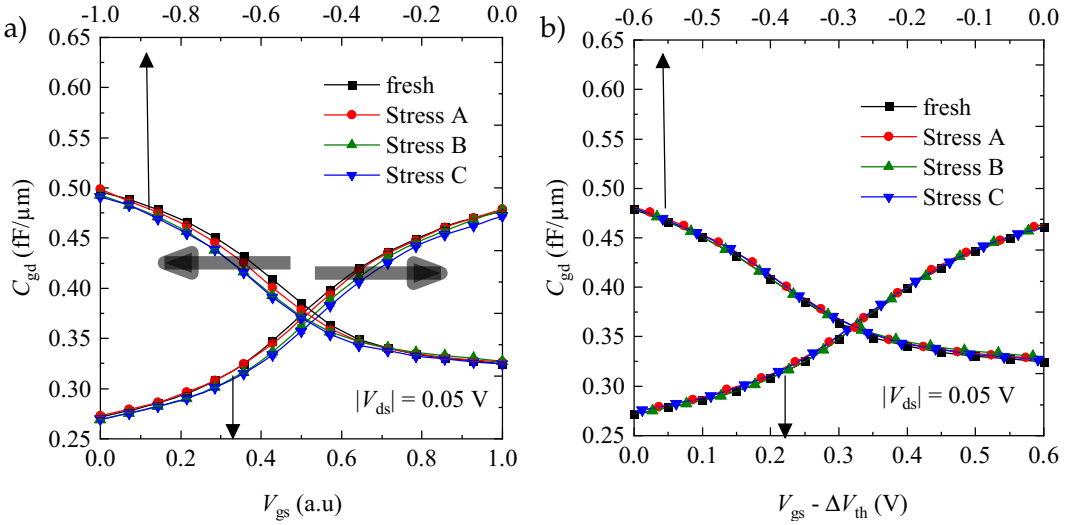


FIGURE 5.8: Plot of $C_{gd}$ as a function of gate-bias extracted at $f$ = 30 GHz and $|V_{ds}|$ = 0.05 V for fresh and stressed devices under different stress conditions as defined in the table of Fig. 5.1(b). $C_{gd}$ plotted (a) as a function of $V_{gs}$ and (b) $V_{gs}$ corrected for $V_{th}$ shift due to BTI stress. The bottom and top x-axis represents values for (a) $V_{gs}$ (b) $V_{gs} - \Delta V_{th}$ for an n-MOSFET and p-MOSFET, respectively.

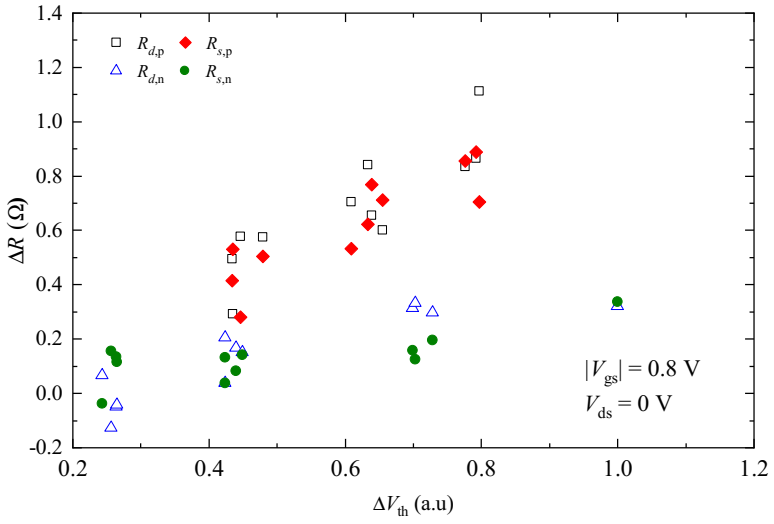


FIGURE 5.9: Apparent shift in source and drain series resistances after BTI stress for n-MOSFET, and p-MOSFET plotted as a function of resultant $V_{th}$ shift. Extraction of series resistance is performed at $f$ = 30 GHz, $|V_{gs}|$ = 0.8 V, and $V_{ds}$ = 0 V.

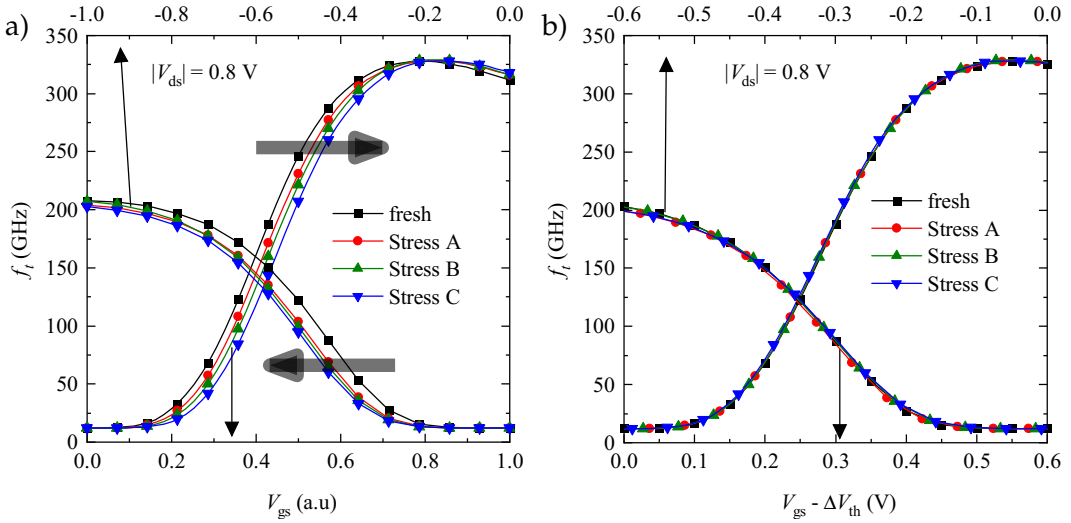


FIGURE 5.10: Effect of BTI stress on transit frequency ($f_t$) plotted over (a) $V_{gs}$ and (b) $V_{gs}$ corrected for $V_{th}$ shift due to BTI stress. Extraction of $f_t$ from $H_{21}$ parameter is performed at $f$ = 30 GHz and $|V_{ds}|$ = 0.8 V. For higher gate biases in (a) for n-MOSFET, the trend in the shift of $f_t$, reversed after reaching the peak $f_t$ value due to decrement of $f_t$ because of mobility degradation and apparent bias shift caused by stress (also observed in Fig. 5.5(a)). The bottom and top x-axis represents values for (a) $V_{gs}$ (b) $V_{gs} - \Delta V_{th}$ for an n-MOSFET and p-MOSFET, respectively.

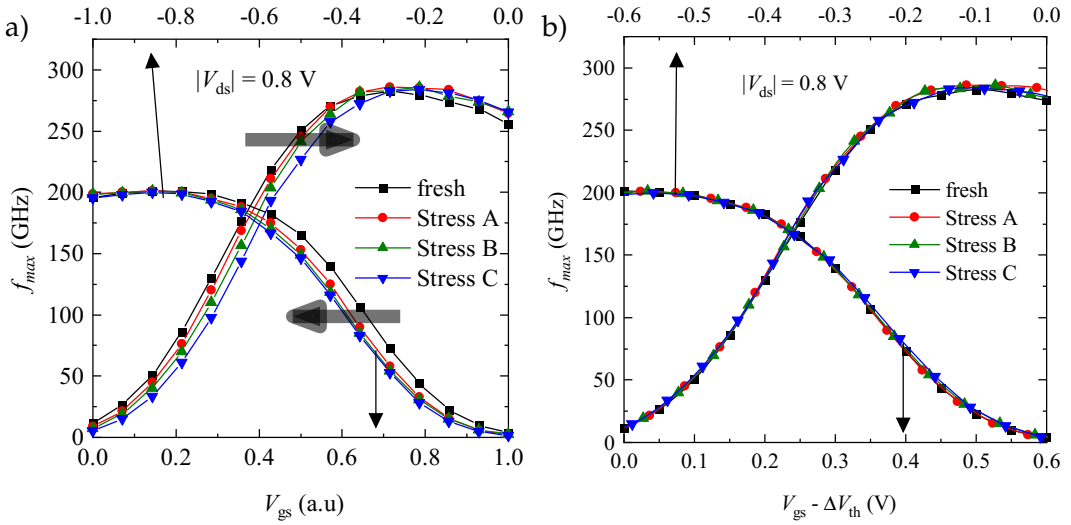


FIGURE 5.11: Maximum oscillation frequency behavior before and after stress plotted vs. (a) $V_{gs}$ and (b) $V_{gs}$ corrected for $V_{th}$ shift due to BTI stress. $f_{max}$ is extracted at $f$ = 30 GHz and $|V_{ds}|$ = 0.8 V. The bottom and top x-axis represents values for (a) $V_{gs}$ (b) $V_{gs} - \Delta V_{th}$ for an n-MOSFET and p-MOSFET, respectively.

## 5.2 S-parameter based on-the-fly Bias Temperature Instability Characterization Method

Since the exploration of the BTI degradation mechanism, the accurate characterization of degraded parameters is a tough challenge due to an inherent recovery as soon as the stress is removed. In some cases, up to 50% of the degradation is reported to recover within 1 s after removal of the stress [174]. The recovery effect is typically associated with de-trapping of the oxide traps, while the quasi-permanent component is generally attributed to the newly generated interface traps [165]. Some reports also claim the switching oxide traps (having charge state depending on the energetic level in the band gap [168]) as a contributor to the recovery [166]. The detailed discussion regarding the nature of traps is significant for the qualitative analysis and understanding of BTI degradation mechanism, albeit the characterization of recovery component accurately is a key to account for the quantitative analysis and identification of trap nature. It is imperative to consider and account for this recovery effect because the significant delay between stress and monitor conditions leads to underestimating the degradation. To measure the true bias temperature degradation as accurately as possible several measurement techniques and setups have been developed to reduce or eliminate the recovery effect. The "fast Vt" method is reported to have achieved a 0.5 $\mu$s measurement delay with special hardware [184]. Using the customary hardware "fast Id" method, which measures the drain current at specified gate voltage near the threshold voltage and then uses the pre-stress IdVg slope for $V_{\text{th}}$ extraction, typically achieve as low as 1 ms of measurement delay [184]. Another measurement technique that gained much attraction in terms of eliminating recovery is the on-the-fly (OTF) method [163], [185], which monitors the degradation without interrupting the stress by applying a small drain voltage or combining it with slight modulations of the stress voltage applied to the gate. Reisinger, Brunner, Heinrigs, *et al.* in [303] showed that even a slight modulation of the stress voltage can induce recovery and lead to a significant error. It was also reported that the error scales with the magnitude of the modulation voltage. S-parameters are the fundamental means of network characterization at a high frequency where a network is described in terms of waves rather than current and voltages. S-parameter measurements are usually required to analyze the high-frequency response of devices and circuits; however, the concept is valid for any frequency. Beyond mere high frequency response characterization, the S-parameter measurements can also be utilized to investigate the changes induced by stress [119], [120], [122], [153], [182], [304]. To extend the full potential of the S-parameter in reliability assessment, the S-parameter based OTF BTI characterization technique (**S**OTF-BTI) is developed to track $V_{\text{th}}$ degradation during BTI stress. Herfst, Schmitz, and Scholten [305] demonstrated the similar S-parameter based methodology featuring small drain bias during monitoring. This characterization discussed in this work aims to eliminate the unwanted recovery during monitoring the BTI degradation and evaluate S-parameters as the potential degradation indicator. The technique is demonstrated for BTI degradation in n-MOSFET and p-MOSFET. The resultant $V_{\text{th}}$ degradation is compared to the "fast Id" method.

### 5.2.1 Measurement Methodology

In order to avoid recovery effects during BTI degradation characterization, it is necessary to maintain the gate stress voltage throughout the entire duration of the stress. This can be achieved by S-parameter measurements performed at the stress condition without interrupting the stress itself. $g_{ds}$ extracted from S-parameter is monitored during the stress and can serve as a parameter to track changes in $V_{th}$. The degradation of $g_{ds}$ due to NBTI in p-MOSFET and PBTI in n-MOSFET has been shown in Fig. 5.6 scales with the stress voltage. A similar apparent shift of $g_{ds}$ can also be observed at $V_{ds}$ = 0 V, as depicted in Fig. 5.12(a). The degradation in $g_{ds}$ is mainly caused by the increase of $V_{th}$ as evident from $V_{th}$ corrected $g_{ds}$ presented in Fig. 5.12(b). Fig. 5.13 shows the apparent and $V_{th}$ corrected $\Delta g_{ds}$ in percentage due to BTI stress plotted over the gate bias. It is observed that $\Delta V_{th}$ correction completely explains the degradation in $g_{ds}$ for the case of PBTI, while for the NBTI, approximately 1% to 2% uncompensated $\Delta g_{ds}$ component remains [182]. This remaining component is associated with the reduction in $g_{m,max}$ caused by mobility degradation.

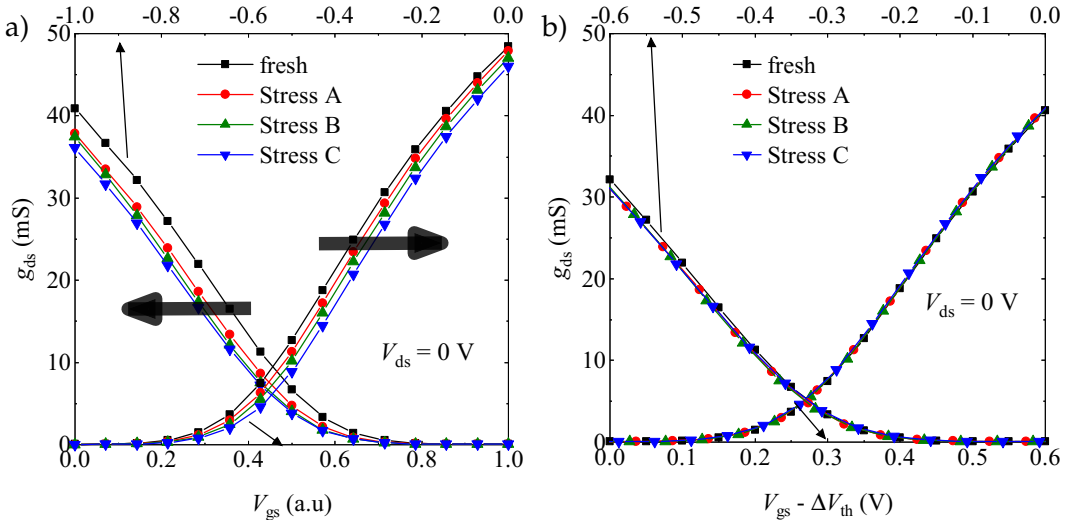


FIGURE 5.12: Behavior of $g_{ds}$ vs. $V_{gs}$ at $V_{ds}$ = 0 V extracted at $f$ = 20 GHz for three different NBTI and PBTI $V_{stress}$ for p-MOSFET and n-MOSFET, respectively as defined in the table of Fig. 5.1(b). (a) Raw $g_{ds}$ degradation before and after stress. The bold arrows direct toward increasing BTI stress volatge. (b) $g_{ds}$ corrected for $\Delta V_{th}$ caused by BTI stress.

This data proves that it is possible to deduce the actual $\Delta V_{th}$ from the measured $\Delta g_{ds}$ with only minor errors due to mobility degradation. The $V_{th}$ shift from the change of $g_{ds}$ is expressed as:

$$\Delta V_{th} = \Big(g_{ds}(t) - g_{ds}(t_0)\Big) \frac{\partial V_{gs}}{\partial g_{ds}}\bigg|_{V_{gs}=V_{stress}} \tag{5.1}$$

where $\partial V_{gs}/\partial g_{ds}$ is measured at $V_{ds}$ = 0 V and $V_{gs}$ around the stress voltage. During BTI stress, the drain is at zero bias. The gate is at fairly high bias above normal operating conditions; a small overlapping signal at zero fixed bias applied at the drain would be sufficient to measure the $g_{ds}$ reliably. Under such bias conditions, the $g_{ds}$ exhibit a comparatively stronger sensitivity to the expected $V_{th}$ shift. In contrast, other bias-dependent small-signal model components such as $g_m$ are relatively insensitive. Thus $g_{ds}$ extracted from S-parameter serve as the critical parameter, which is a function of gate bias.

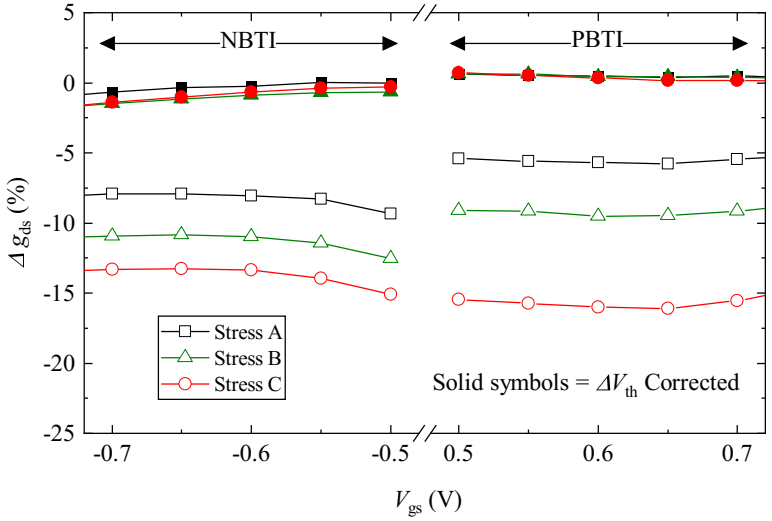


FIGURE 5.13: $\Delta g_{ds}$ in percentage vs. $V_{gs}$ for p-MOSFET and n-MOSFET. The open symbol represents the apparent $\Delta g_{ds}$ after BTI stress, while the solid symbols show the $\Delta V_{th}$ corrected $\Delta g_{ds}$. The x-axis omit the values lower than |0.5 V|. The stress conditions are defined in the table of Fig. 5.1(b).

The setup as shown in Fig. 3.2 is used. As BTI experiments are performed at high temperatures, the VNA is calibrated using the LRRM algorithm at the system temperature of 125 °C. The S-parameters are measured during the stress over logarithmic intervals of time. Extraction of $\partial V_{gs}/\partial g_{ds}$ is performed on separate fresh devices to eliminate the possibility of premature stressing the DUTs on which the degradation has to be observed. The DUTs are then stressed for $10^4$ s in BTI mode, and S-parameters are measured simultaneously for the single frequency point of 20 GHz and power level of -25 dBm during the stress. The power level of -25 dBm in a 50 Ω system corresponds to 35.56 mV peak-to-peak, sufficient to measure $S_{22}$ at $V_{stress}$ reliably. It is imperative to point out that no voltage bias is applied to the drain in this setup except the small RF signal during S-parameter measurement. This eliminates any probability of unwanted parasitic contribution of any other stress mechanism such as HCD due to carriers' flow under the drain bias. The entire measurement flow is summarized in Fig. 5.14.

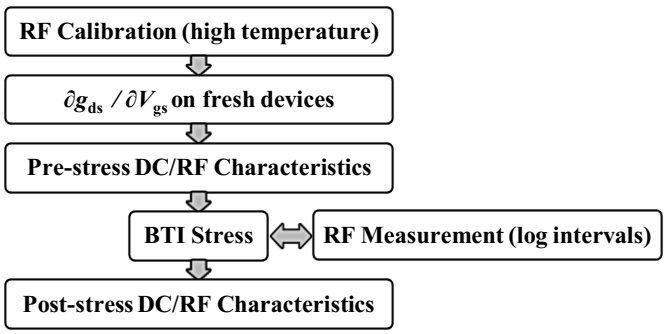


FIGURE 5.14: Characterization flow for the S-parameter based OTF BTI characterization technique.

### 5.2.2 Results and Discussion

Fig. 5.15 shows the time evolution of $g_{ds}$ under NBTI and PBTI stress. It is important to note that the very first $g_{ds}$ reading at time $t_1$ is measured under $V_{gs} = V_{stress}$, which already incorporates some stress. In conventional OTF techniques, the $t_1$ values are assumed to be not critically stressed [163] and regarded as a reference for the subsequent measured values; thus, the degradation would depend on the delay between the application of stress and first measurement. In some OTF setups, the measurement delay is 1 ms [306], whereas, in the ultra-fast OTF, it is reduced to 1 $\mu$s [256], [307]. In this work, the $t_0$ or unstressed value is extracted by assuming the linear fit of $g_{ds}$ for shorter stress times. The $g_{ds}$ at $t_0$ can then be computed from the measured data by the regression, as shown in Fig. 5.16.

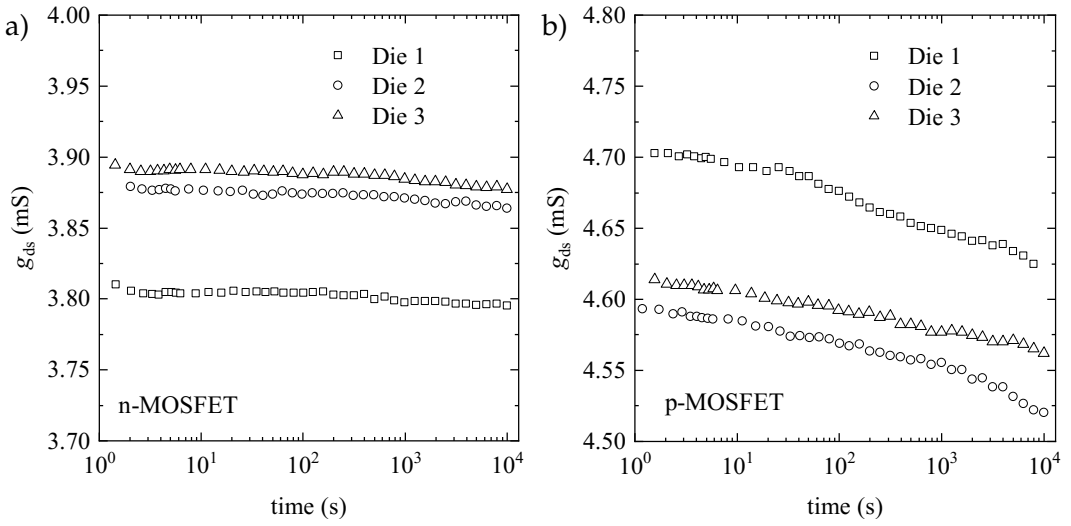


FIGURE 5.15: Measured $g_{ds}$ (at $f$ = 20 GHz) as a function of stress time for $V_{gs} = V_{stress}$ of 1.6 V and -2.0 V for (a) n-MOSFET and (b) p-MOSFET respectively on three different dies on the same wafer.

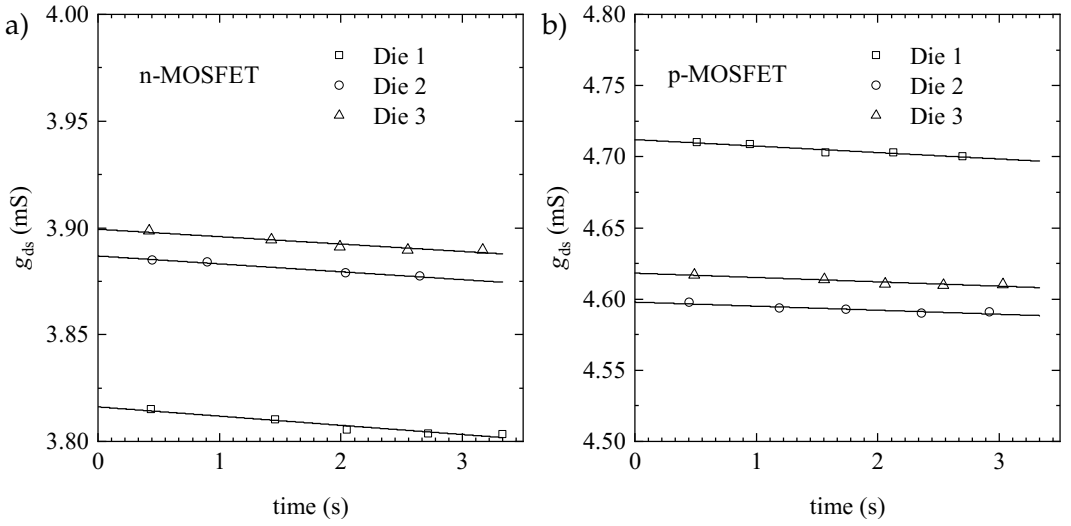


FIGURE 5.16: Extraction of the initial value of undegraded $g_{ds}$ at $t_0$ by linear fit for (a) n-MOSFET and (b) p-MOSFET.

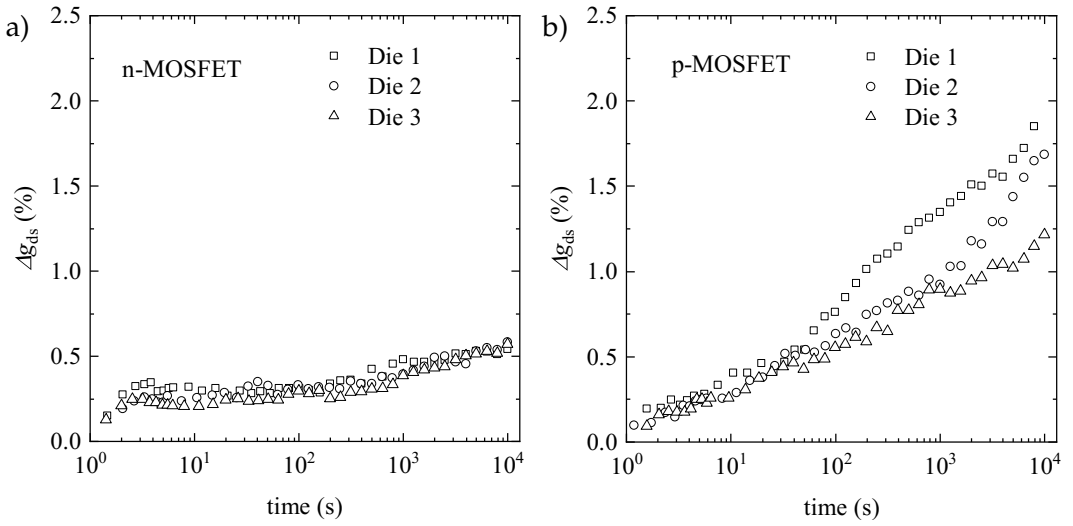


FIGURE 5.17: $\Delta g_{ds}$ in percentage plotted vs. $t$ using the $g_{ds}$ at $t_0$ as the unstressed reference for (a) n-MOSFET and (b) p-MOSFET.

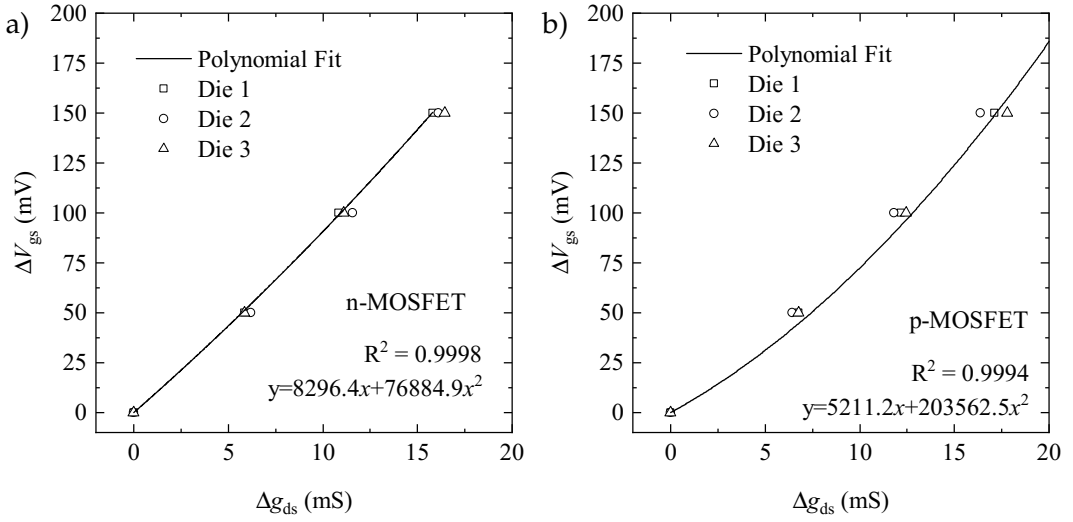


FIGURE 5.18: Polynomial fit of change of $V_{gs}$ as a function of change in $g_{ds}$ for an (a) n-MOSFET and (b) p-MOSFET measured in the vicinity of the applied BTI stress voltages.

Fig. 5.17 shows the percentage shift of $g_{ds}$ for n-MOSFET and p-MOSFET during BTI stress. NBTI in p-MOSFET exhibits prominently larger delta $g_{ds}$ as compared to the PBTI in n-MOSFET. Die-to-die variation in $\Delta g_{ds}$ for n-MOSFET is relatively smaller than p-MOSFET. In order to translate the $\Delta g_{ds}$ into $V_{th}$ shifts using equation 5.1, the $\partial V_{gs}/\partial g_{ds}$ is a crucial parameter which can be either extracted by experimental data around stress conditions or using a calibrated spice model. Using experimental data might lead to underestimating degradation due to the degradation of the devices itself used for such measurements. On the other hand, the spice models are usually calibrated and verified up to the normal operating conditions, and the stress level required to observe the BTI degradation for the devices used in this study is about twice the maximum allowed $V_{gs}$ under operating conditions. In order to eliminate the uncertainty and mismatch of the spice model, the experimental data is used in this study, as shown in Fig. 5.18. The extracted $\Delta V_{th}$ using the methodology demonstrated here is compared in Fig. 5.19 with the BTI degradation measured using the "fast Id" method featuring a

measurement delay of less than 2 ms. The BTI degradation measured by the S-parameter method shows a comparatively larger $\Delta V_{\text{th}}$ for both NBTI and PBTI as it does not constitute the recovery component. Note that the increase of the measured BTI degradation depends on the strength of the recovery effects, which is more pronounced in the p-MOSFET devices as indicated by the larger drop of delta $V_{\text{th}}$ after recovery as indicated by the arrows in Fig. 5.19. BTI degradation assessment with a shorter measurement delay tends to result in smaller time slopes [308]. If measured long enough with larger measurement delays, the time slope approaches towards the one of shorter measurement delay [309]. As illustrated in Fig. 5.19, the $\Delta V_{\text{th}}$ for the PBTI shows a slightly lower time slope than the one of "fast Id". However, for NBTI, the time slope of the **S**OTF-BTI method does not follow the reduced relaxation kinetics. Although, the **S**OTF-BTI measurement setup inherently present the opportunity to avoid the recovery entirely, the $\partial V_{\text{gs}}/\partial g_{\text{ds}}$ present to be the challenge which can be a source of error.

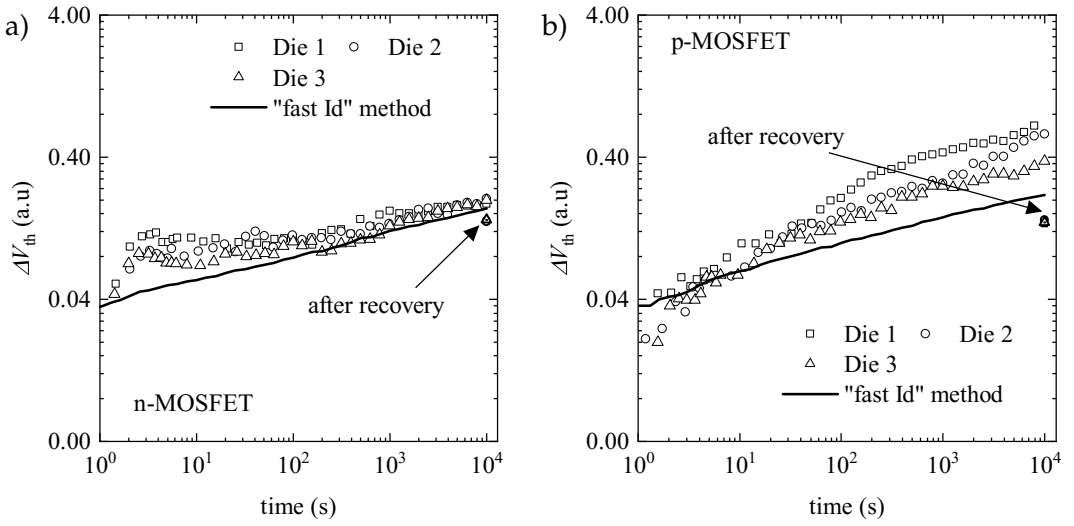


FIGURE 5.19: Comparison of extracted $\Delta V_{\text{th}}$ using **S**OTF-BTI and "fast Id" method plotted over stress time for (a) n-MOSFET and (b) p-MOSFET. The dotted symbols depict $\Delta V_{\text{th}}$ after recovery of a few minutes.

The measurement accuracy is relatively coarse, and for the case of NBTI, the extracted $\Delta V_{\text{th}}$ on three dies does not match very well for longer stress times. The disparity inherently arises from the VNA sensitivity in measuring $g_{\text{ds}}$ with no drain bias and might also be reasoned in the small width of devices used in this study. Fig. 5.20 evaluates the maximum possible systematic error in the extraction of $\Delta V_{\text{th}}$ arising from the deviation of the fit line from the measured data and the die-to-die variation. The systematic error is computed using worst case fit error of $\partial V_{\text{gs}}/\partial g_{\text{ds}}$. The error is comparatively higher in p-MOSFET as the $g_{\text{ds}}$ is relatively insensitive to the $V_{\text{gs}}$ and tends to saturate around the stress level. The systematic error in $\Delta V_{\text{th}}$ is reduced to 3.8% in n-MOSFET due to the better fit and larger dependence of $g_{\text{ds}}$ on $V_{\text{gs}}$.

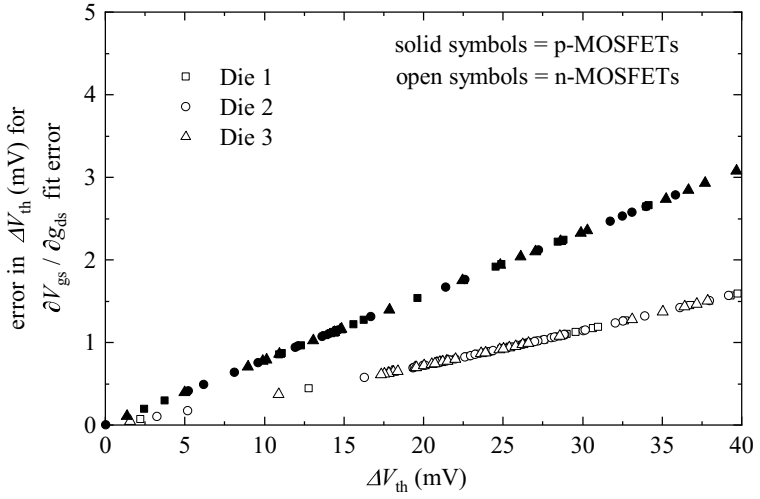


FIGURE 5.20: Systematic error in $\Delta V_{\mathrm{th}}$ extraction due to polynomial fitting error of $\partial V_{\mathrm{gs}} / \partial g_{\mathrm{ds}}$ for n-MOSFET and p-MOSFET.

# Chapter 6

# Investigation of Hot-carrier Degradation

HCD as one of the key reliability concerns for a transistor, is becoming highly relevant in advanced semiconductor devices with ultra-scaled dimensions and enhanced electric fields. Very few studies were devoted to the investigation of hot carrier degradation impact on small-signal parameters in general and are specific to certain technologies [112], [117], [310]. However, no investigations were done in the past for FDSOI transistors. With the wide recognition and applications (especially in high frequency) of the FDSOI devices, the reliability study of these devices plays a vital role in gaining a deeper understanding and develop future technology nodes. Previous studies which covered the impact of hot carrier stress in DC to millimeter-wave domain did not account for the detailed small-signal parameter analysis (inherent to the complex nature of analysis and available information from multiple perspectives) [111], [113], [115], [116], [310]. When considering the implications of HCD in high-frequency applications, different variables such as applied voltage swings, signal frequency, power of the applied signal, and role of harmonics exist. All of these variables can influence the resultant degradation, and with such operation conditions, several degradation mechanisms can interplay. Depending on the prevalent operation condition, a dominant degradation mechanism yields a significant contribution of degradation. The approach of the HCD analysis done in this study is to investigate merely the impact of hot carrier stress and prevent the intermixing of other degradation mechanisms as much as possible. This can be achieved using traditional DC stress conditions, which ensure the applicability of a specific degradation mechanism. To cater for the variable mentioned earlier in the real usage case, a quasi-static approximation is assumed in this study which can be employed by developing scaleable HCD models. The model formation can be based on basic parameters such as stress voltages and temperature while incorporating other factors which could influence the basic parameters. The development and verification of such a model are not in the scope of this dissertation. However, the basis and investigation of those factors are performed in this chapter.

This chapter discusses the impact of HCD on DC and small-signal parameters in the first section. The later part of this chapter is devoted to investigating the dependence of hot carrier-induced degradation on transistor physical dimensions and the design of the devices. The findings of Chapter 4 and Chapter 5 forms the basis for the explanation and origin of this dependence.

## 6.1 Impact of Hot-carrier stress on Device performance

HCD is characterized during the turn-on condition under relatively high drain and gate stress voltages. Used stress condition ($V_{gs}$ = $V_{ds}$) is regarded as the worst-case condition in advanced technology nodes [131], [301], [311], [312]. A stress voltage larger than 1.4 times the maximum operating voltage is applied at a high temperature to accelerate the degradation. Three different stress voltages applied for HCD characterization in p-MOSFET and n-MOSFET are denoted in absolute ascending order as Stress A, Stress B, and Stress C in the following text. The stress voltages are defined in the table 6.1. DC characteristics are intermediately monitored during the stress while S-parameters are measured before and after stress. A minimum of five devices for a given stress condition were stressed and measured to ensure accurate analysis, and median data is plotted in subsequent figures. HCD characterization is performed on the generic measurement setup shown in Fig. 3.2.

TABLE 6.1: Stress voltages applied for HCD characterization to an n-MOSFET and p-MOSFET.

| Stress | n-MOSFET | p-MOSFET |
|---|---|---|
| A | 1.20 V | -1.15 V |
| B | 1.25 V | -1.20 V |
| C | 1.30 V | -1.25 V |

### 6.1.1 DC Metrics Degradation

The carriers ensemble under applied stress condition, govern by MP process result in the generation of localized interface [127], [128] and bulk oxide defects [128], [129] causing the degradation of transistor parameters. Fig. 6.1 shows the degradation of $I_{d,sat}$ plotted vs. stress time for n-MOSFET and p-MOSFET at different stress voltages. For both n-MOSFET and p-MOSFET, $\Delta I_{d,sat}$ scales with the applied $V_{stress}$, and the trend with respect to stress time tends to saturate for longer stress time. For the case of p-MOSFET, this saturation effect is more pronounced and observed to be scaled with the stress voltage. This observed saturation effect in the p-MOSFET will be discussed in detail in section 6.3.

Other DC parameters affected by HC stress are shown in Fig. 6.2. The DC parameters shift originates from the impairment in the channel and interface region caused by the hot (high energy) carriers, which transit through the high electric field between source and drain. The observed degradation in these nano-scaled devices is explained by the single-particle and multi-particle process as discussed in section 2.4.1. These hot carriers lead to the creation of localized interface traps and trapping of hot electrons in the gate oxide, which is evident from the changes in threshold voltage and subthreshold swing (Fig. 6.2). For n-MOSFET, linear $V_{th}$ ($V_{th,lin}$) and saturation $V_{th}$ ($V_{th,sat}$) increase after stress and linearly scale with the applied stress voltage as shown in Fig. 6.2. The difference between $V_{th,sat}$ and $V_{th,lin}$ is defined as drain induced barrier lowering (drain induced barrier lowering). In nano-scaled devices DIBL is one of the main short-channel effect indicating the impairment of the effective gate control for shorter $l_g$. As shown in Fig. 6.2, the DIBL degradation is stronger for the p-MOSFET compared to n-MOSFET.

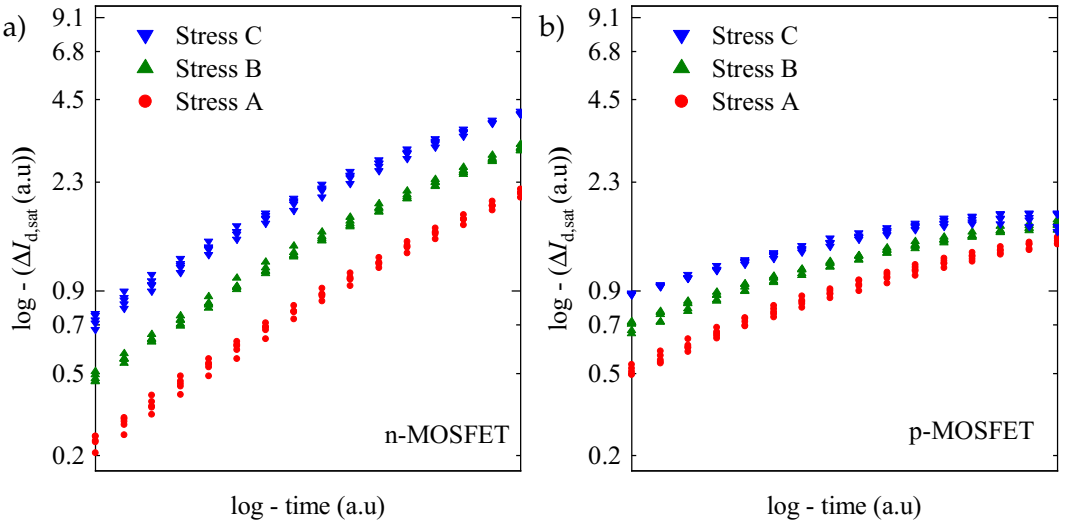


FIGURE 6.1: Absolute degradation of $I_{d,sat}$ plotted as a function of HC stress time for (a) n-MOSFET and (b) p-MOSFET with device dimensions $l_g$ = 18 nm, $w_f$ = 1 µm, $nf$ = 16, and $f_{spac}$ = 86 nm. The magnitude of stress voltage is defined in the table 6.1.

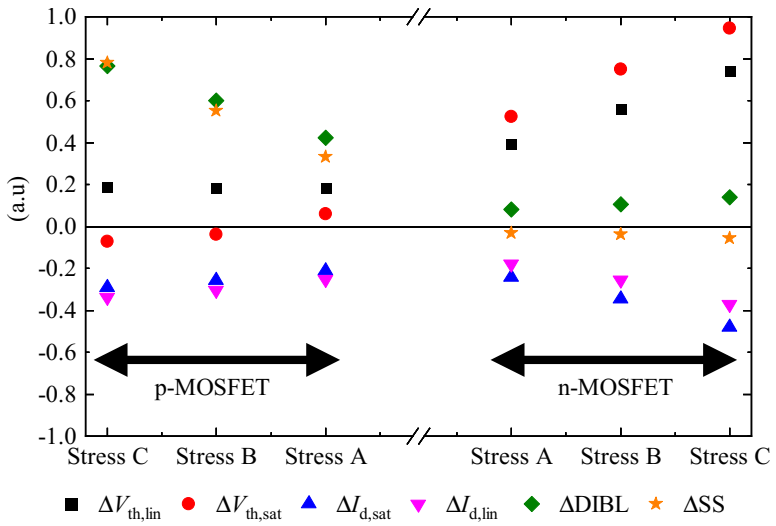


FIGURE 6.2: Apparent shift in DC parameters after stress plotted vs. HC stress voltage. On the left of the x-axis, p-MOSFET characteristics are plotted, while on the right side, parameter drift of n-MOSFET is shown. The negative and positive values correspond to a decrease and increase in respective parameters. The stress voltages are defined in the table 6.1.

In Fig. 6.2, the degradation and linear scaling of SS with stress voltage magnitude can be seen for the p-MOSFET, implying the generation of interface traps. On the other hand, for an n-MOSFET the SS remains almost unchanged but slightly lower for different stress voltages. In p-MOSFET, $V_{th,lin}$ increases after stress but does not scale with the $V_{stress}$. $\Delta V_{th,sat}$, on the other hand for the p-MOSFET, shifts from positive to negative values with the increment of stress voltage. It is interesting to note that though the p-MOSFET $V_{th,sat}$ tends to decrease after the Stress B and Stress C, the $I_{d,sat}$ still shows degradation in Fig 6.1. This peculiar behavior of $\Delta V_{th}$ in p-MOSFET is discussed in section 6.3. Conventionally, the degradation of $I_{d,lin}$ is more severe than $I_{d,sat}$ reasoned in the drain-side degraded region's masking effect in the saturation regime. However, in short, channel devices, the degradation of $I_{d,lin}$ and $I_{d,sat}$ are comparable due to the

increased channel length ratio to the localized damaged drain region. In the studied devices, $\Delta I_{d,lin}$ and $\Delta I_{d,sat}$ degrade almost similar in quantity; however, $I_{d,lin}$ degradation is slightly higher than $I_{d,sat}$ in p-MOSFET and vice versa in n-MOSFET.

### 6.1.2 Impact on small-signal Parameters

As discussed in Chapter 5, for the case of BTI-induced degradation, the frequency dependence of small-signal parameters is not impaired, evident from the validity of bias point correction. In the case of HCD, various DC metrics are affected simultaneously, and a simple bias point correction will not be enough to explain the changes in small-signal parameters. First, the effect of hot carrier stress on the frequency behavior of raw Y-parameters is evaluated. For most of the Y-parameters, the frequency behavior is mainly intact, and only an offset is observed for the measured Y-parameter after stress (see Appendix C). Some Y-parameters such as $Re(Y_{12})$, $Im(Y_{12})$, and $Im(Y_{21})$ in n-MOSFET (Fig. C.1) while $Re(Y_{21})$ and $Im(Y_{12})$ in p-MOSFET (Fig. C.2) show slight variations at higher frequencies. This variation can be associated to the shift of effective bias after the hot carrier stress as Y-parameters are a function of both frequency and bias. Hence, the computed small-signal model components as a function of biasing must be analyzed for further understanding.

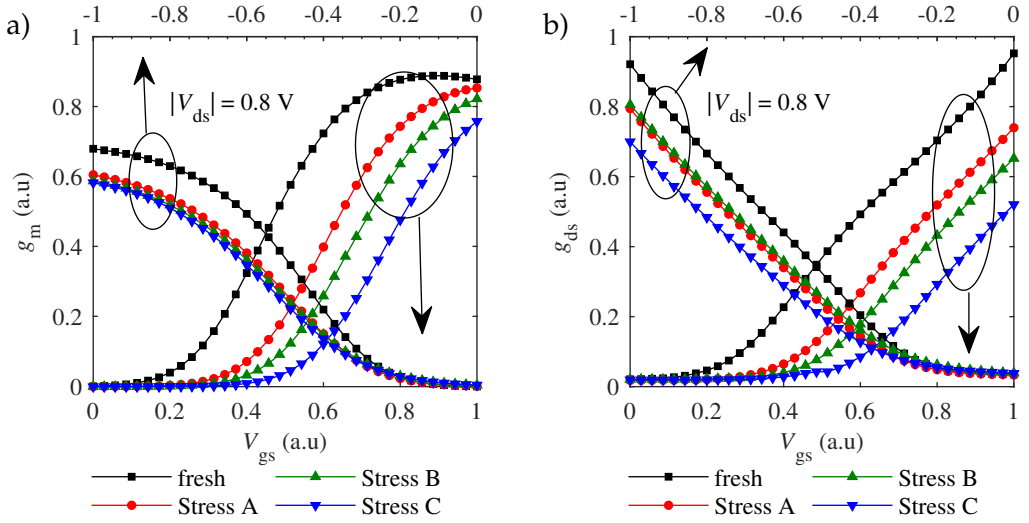


FIGURE 6.3: (a) $g_m$ vs. $V_{gs}$ and (b) $g_{ds}$ vs. $V_{gs}$ for fresh (unstressed) and HC stressed devices extracted at $f$ = 30 GHz at $|V_{ds}|$ = 0.8 V. The negative and positive $V_{gs}$ on top and bottom shows the characteristics of p-MOSFET and n-MOSFET respectively. Device dimensions and stress voltages are identical, as mentioned in the caption of Fig. 6.1.

The degradation of drain current and effective mobility due to HC stress directly translates into the degradation of gain parameters (i.e., $g_m$ and $g_{ds}$), shown in Fig. 6.3. It can be observed that the lateral scaling of $\Delta g_m$ and $\Delta g_{ds}$ with respect to the stress voltage in n-MOSFET and p-MOSFET correlates with the observed $V_{th}$ shift. However, the degradation of the absolute value of peak $g_m$ and $g_{ds}$ can be seen due to the degradation of $\mu_{eff}$. From Fig. 6.3(a), it can be observed that n-MOSFET dominantly suffers from $V_{th}$ degradation while p-MOSFET is mainly affected by $\mu_{eff}$ degradation. It is well known that the HCD predominantly affects the drain region due to high electric fields at the drain side. This effect is visible in the extracted drain and series resistances, as shown in Fig. 6.4. $R_d$ degrades more than $R_s$ in both n-MOSFET and p-MOSFET. It is important to note that the change

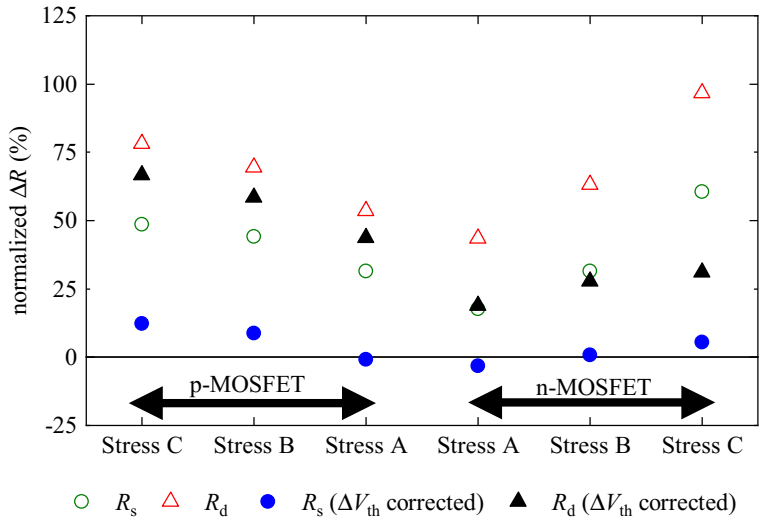


FIGURE 6.4: Extracted change in source and drain series resistances after HC stress of different $V_{stress}$ for p-MOSFET and n-MOSFET. Hollow markers represent the as measured apparent shift in series resistances while solid symbol plots the $\Delta V_{th}$ compensated $\Delta R$. The series resistances are extracted from S-parameters at $f$ = 30 GHz and cold-fet bias condition ($|V_{gs}|$ = 0.8 V, $V_{ds}$ = 0 V).

in series resistance can be reflected from the bias point shift and increase of its absolute value because of localized damage. It can be seen in the plot that after the correction of $\Delta V_{th}$, the apparent bias-dependent resistance shift is removed, and an absolute increase of series resistance is observed. After $V_{th}$ correction, $R_s$ in n-MOSFET remains almost unchanged while a slight increase at higher stress voltage is seen for p-MOSFET.

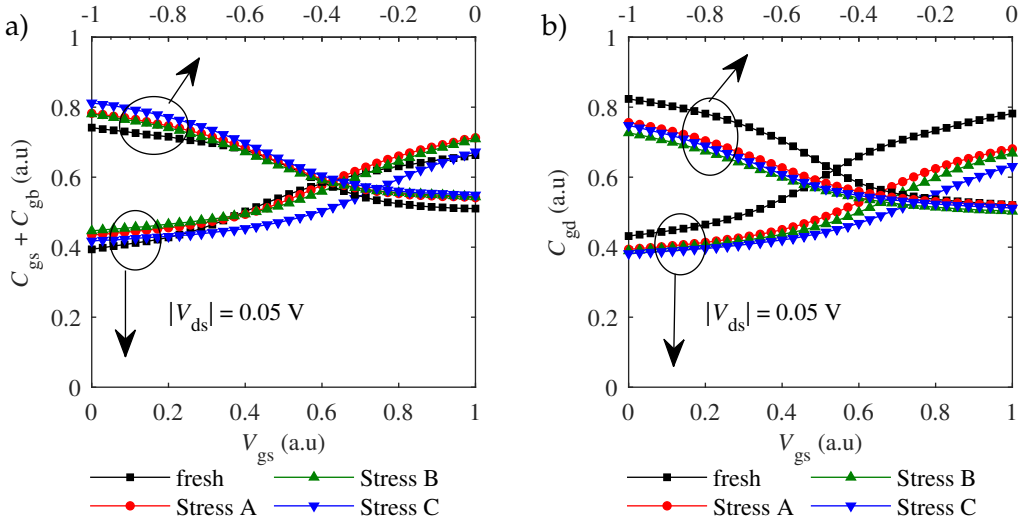


FIGURE 6.5: Behavior of (a) $C_{gs}$ and (b) $C_{gd}$ vs. $V_{gs}$ for fresh (unstressed) and HC stressed devices extracted at $f$ = 30 GHz at $|V_{ds}|$ = 0.05 V. The negative and positive $V_{gs}$ on top and bottom shows the characteristics of p-MOSFET and n-MOSFET respectively. Device dimensions and stress voltages are identical, as mentioned in the caption of Fig. 6.1.

The change in gate-related capacitances before and after stress over different gate biases at $V_{ds}$ = 50 mV is depicted in Fig. 6.5. The behavior of $C_{gs}$ and $C_{gd}$ after stress is similar between n-MOSFET and p-MOSFET. An overall increase of $C_{gs}$ and

a decrease in $C_{gd}$ is observed after stress. For meaningful analysis, the effect of bias point shift from capacitances must be separated. Nevertheless, for RF applications where input and output matching is needed, it is equally important to note the parameter changes at fixed operating conditions. The gate-related intrinsic capacitances $C_{gs}$ and $C_{gd}$ can be represented by the surface channel resistance model [313], [314] according to

$$C_{gs} = -\frac{\partial Q_g}{\partial V_s} = \frac{w_g C_{ox}}{V_{ms}} \int_{x=0}^{x=l_{eff}} v_{ac}(x)dx, \tag{6.1}$$

$$C_{gd} = -\frac{\partial Q_g}{\partial V_d} = \frac{w_g C_{ox}}{V_{md}} \int_{x=0}^{x=l_{eff}} v_{ac}(x)dx \tag{6.2}$$

where $C_{ox}$ is the oxide capacitance and $l_{eff} = l_g - \Delta l_g$ represents the effective channel length. $V_{ms}$ and $V_{md}$ is the amplitude of small-signal AC voltage applied to the source and drain, respectively, to measure the capacitances; $v_{ac}(x)$ is the small-signal potential across the channel. The surface channel resistance model can be used to understand the bias dependence of the small-signal capacitances. For low $V_{ds}$ resulting in a flat channel potential, the contribution of the gate to channel capacitance is equally distributed among $C_{gs}$ and $C_{gd}$. In saturation, $C_{gd}$ is considerably reduced while $C_{gs}$ increases due to pinch-off of the channel at the drain side. In other words, the paramount gate-to-channel capacitance is attributed to $C_{gs}$, as can be seen from the measurement data shown in Fig. 6.6 for the unstressed device. Thus, $C_{gd}$ becomes independent on $V_{gs}$ (Fig. 6.6(c),(f)), and any changes in the gate to channel capacitance have only a minor effect on the remaining $C_{gd}$. However, comparing the $\Delta V_{th}$ corrected capacitances before and after stressing the device, an increase in $C_{gs}$ (Fig. 6.6(b)) and a decrease in $C_{gd}$ (Fig. 6.6(c)) is evident.

Using charge pumping, the decrement of $C_{gd}$ after stress is reported in [313]. Naseh, Deen, and Marinov in [114] reported an increase in $C_{gs}$ only after HC stress and no change in $C_{gd}$. However, it is important to mention that in this study, the total gate-related capacitance $C_{gg}$ remains almost the same after stress (Fig. 6.6(a)). Further, the impact on $C_{gs}$ is more prominent at $V_{ds}$ = 0.05 V compared to $V_{ds}$ = 0.8 V, as shown in Fig. 6.6(b)(c). The observations can be explained as follows. During HC stress, electrons are trapped mainly in the region close to the drain side, resulting in a local change of flatband voltage. For low $V_{gs}$, that effect results in a local pinch-off of the channel, leading to the observed change in the capacitance contributions. However, in the case of saturation at higher $V_{ds}$ the degraded region is masked and $C_{gs}$,$C_{gd}$ exhibit very low sensitivity to the degradation. Fig. 6.6 also demonstrates and compares the changes in capacitance arising from HC and BTI stress. Changes in $C_{gs}$ and $C_{gd}$ reflect the nature of perturbations caused by different stress types. As it can be seen in Fig. 6.6(e),(f), the $\Delta V_{th}$ corrected $C_{gs}$ and $C_{gd}$ is composed dominantly by the bias-dependent transference due to BTI stress. This is contrary to the change in gate capacitances seen after the HC stress. The mere threshold voltage-dependent shift for both $C_{gs}$ and $C_{gd}$ after BTI stress is in accordance with the assumed uniform distribution of defects and trapped charges in the gate oxide and interface. The magnitude of $\Delta V_{th}$ corrected $C_{gg}$ remains the same after both types of stresses.

The key FoMs $f_t$ and $f_{max}$, which depend on the parameter discussed earlier, also exhibit a resultant degradation effect, as shown in Fig. 6.7. The changes in FoMs are predominantly due to the degradation of $g_m$ and exhibit similar bias-dependent behavior for different stress voltages. At higher gate bias in n-MOSFET(Fig. 6.7(b)), the $f_{max}$ tends to have a higher value than the unstressed device. This is due to the

fact that for the stressed devices, the peak of $f_{max}$ is shifted to higher gate bias due to $V_{th}$ degradation. This implies that depending on the amount of induced stress in a real use case, the apparent shift in parameters can be negative and positive.

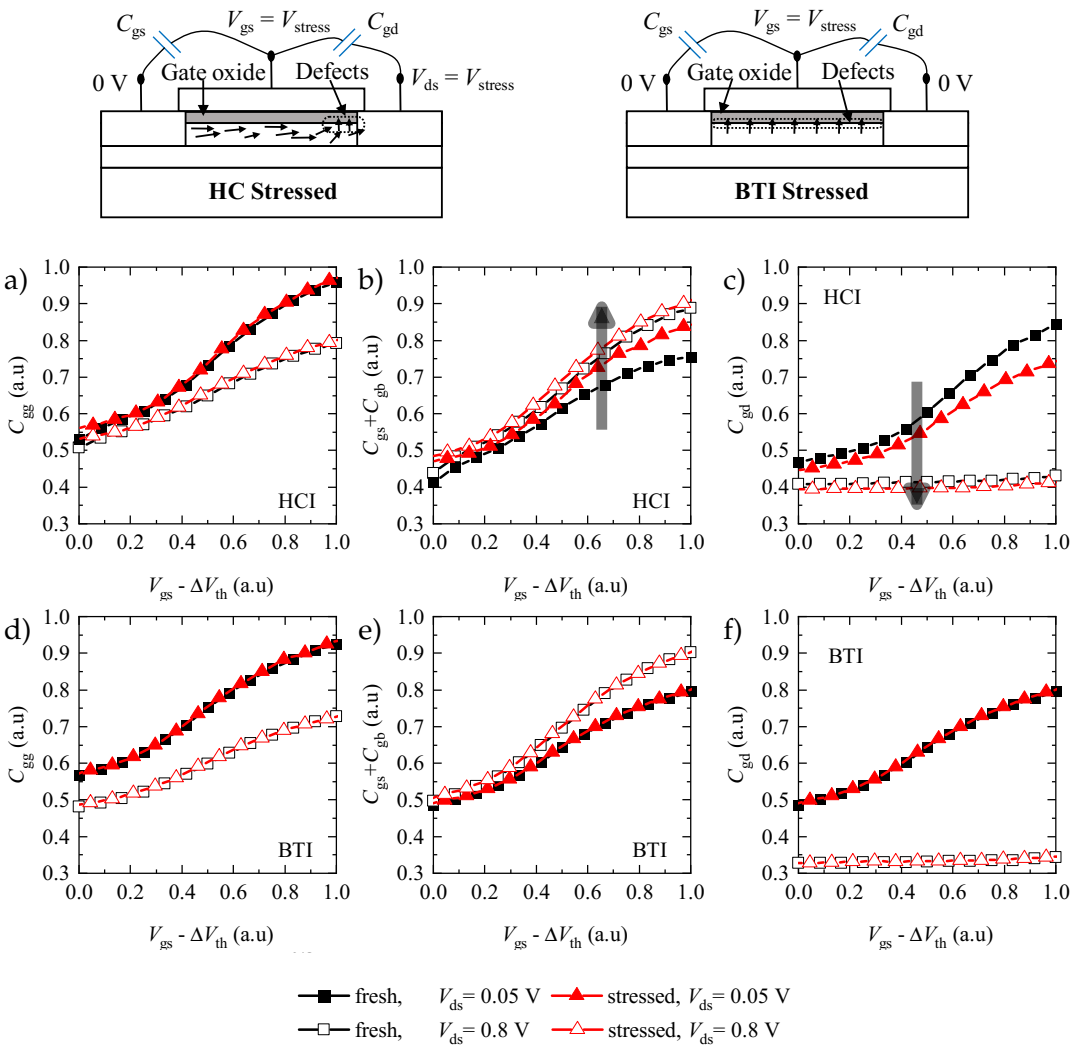


FIGURE 6.6: Comparison of changes in small-signal capacitances after $\Delta V_{th}$ correction in linear ($|V_{ds}|$ = 0.05 V) and saturation ($|V_{ds}|$ = 0.8 V) in n-MOSFET subjected to a specific stress condition of BTI and HC stress. The schematics on top illustrate the assumed macroscopic mechanism of defect creation by different stress modes. (a), (b), and (c) plots the $C_{gg}$, $C_{gs}$, and $C_{gd}$ for HC stressed devices. Similarly, (d), (e), and (f) plots the $C_{gg}$, $C_{gs}$, and $C_{gd}$ for BTI stressed devices. All capacitances are extracted at $f$ = 30 GHz.

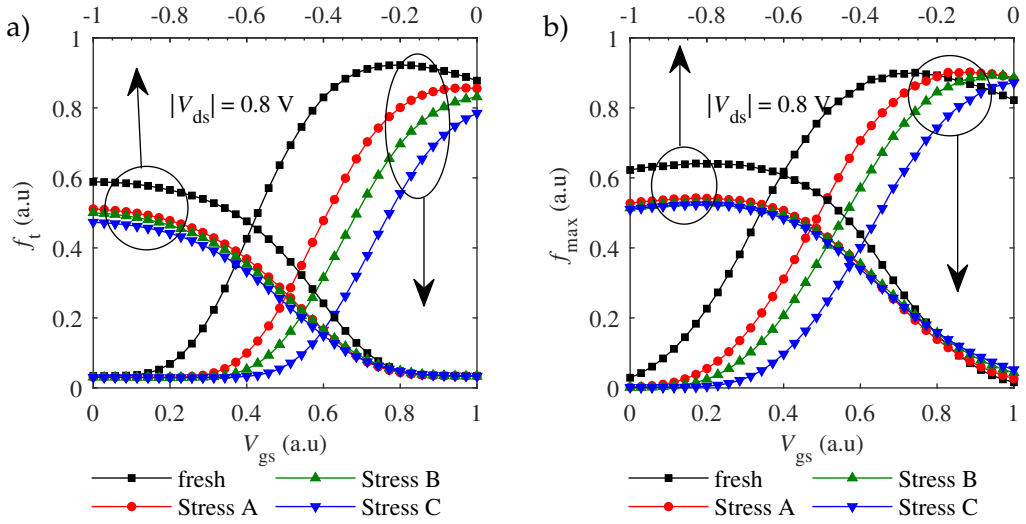


FIGURE 6.7: As measured changes in key FoMs, i.e. (a) $f_t$ and (b) $f_{max}$ plotted vs. $V_{gs}$ for fresh and HC stressed devices. Extraction of FoMs is performed at $f$ = 30 GHz and $|V_{ds}|$ = 0.8 V.

## 6.2 Implications of Self-heating on Hot-carrier Degradation in n-MOSFETs

Several studies in the literature discuss the specific reliability of FDSOI in detail [149], [152], [311]; only a few studies are done to evaluate the impact of self-heating on HCD [315]. However, until now, the convolution of self-heating effects in HCD for multi-finger transistors coupled with layout variations was not investigated for FDSOI devices. Multi-finger and multi-cell devices are widely used in RF and analog applications to achieve high power, reduce the physical size, lower gate resistance, and improve device matching. A simple logic device's self-heating characteristics lack the information about the effects that could arise from multi-finger structures having different layout variations due to application requirements. With the increasing interest in RF reliability, multi-finger devices are readily used for reliability characterization [118], [316]–[319] and subjected to varied stress patterns. Usually, in these reliability assessments, the focus is mainly on the analysis of the performance impact. However, to attain generic applicability and take care of a range of operating conditions, scalable RF reliability models are needed. Therefore, the inclusion and understanding of self-heating is an essential prerequisite for building a scalable reliability model.

The temperature dependence of HCD is an attribute that associates it with self-heating. Traditionally, HCD caused by the impact ionization of hot electrons is more pronounced as the temperature decreases (negative activation energy ($E_a$)) [150]. However, in ultra-scaled devices with the reduction of channel length, the HCD increases with increasing temperature (positive $E_a$) [137], [138], [320]. As the device dimension shrinks, the bond dissociation mechanism is dominated by a multiple particle process in which several cold (having not enough energy for bond dissociation) particle collisions result in rupturing the Si-H bond [131], [139], [145]. Thus, self-heating is an important consideration and should be accounted for in the HC reliability. The impact of self-heating on HCD and its characterization and the analysis of device layout parameters is critical for improved reliability.

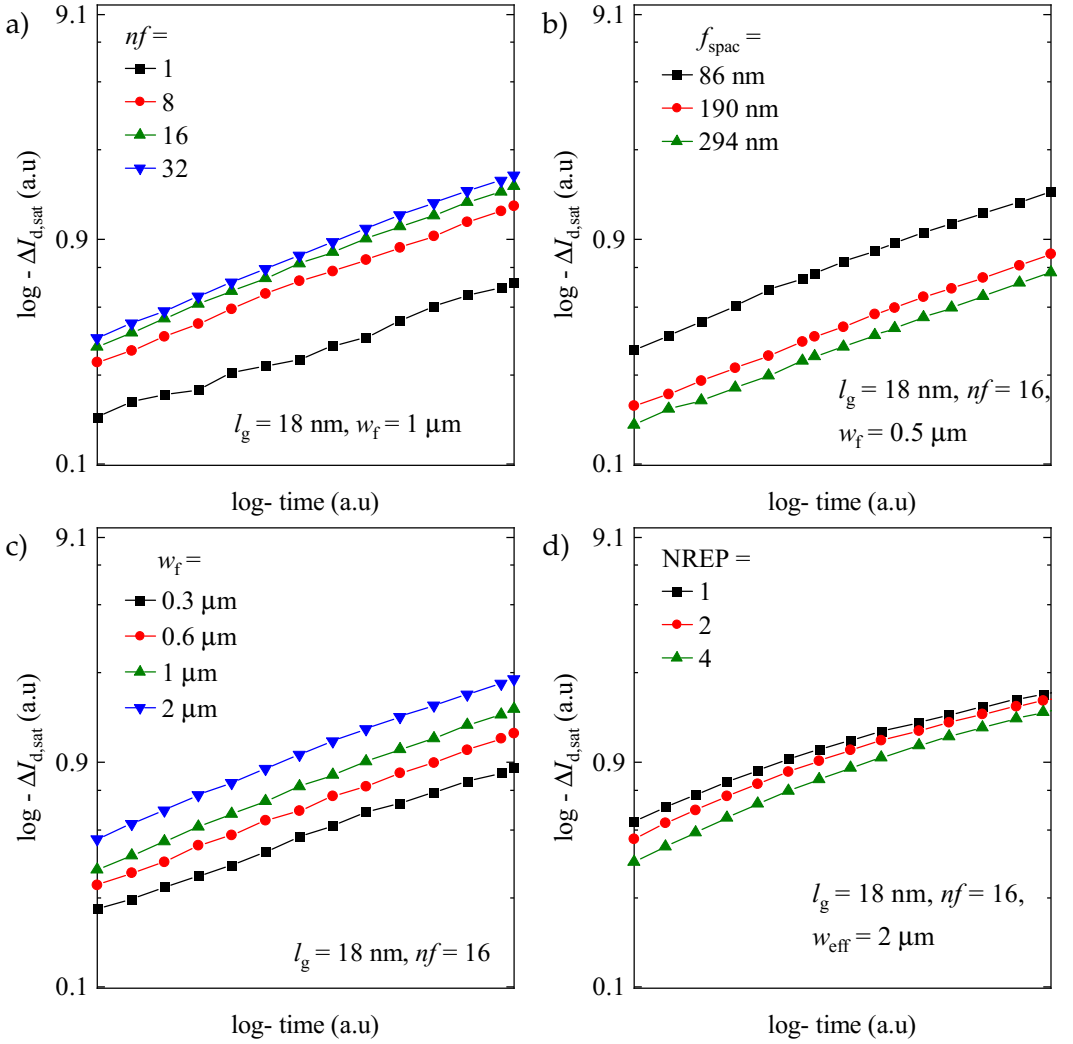


FIGURE 6.8: Evolution of $I_{d,sat}$ degradation as a function of HC stress time plotted for (a) number of fingers ($nf$) scaling, (b) different spacing between adjacent fingers ($f_{spac}$), (c) gate width ($w_f$) scaling, and (d) structures with different NREP (Fig. 4.15(a),(b) and (c)). The median of several devices is plotted, and every device is stressed for the same HC stress condition (Stress C).

The drift of $I_{d,sat}$ with respect to time for different layout dimensions is shown in Fig. 6.8. As the hot carrier stress is done at the same chuck temperature for all devices, the $\Delta I_{d,sat}$ dependence on the self-heating is observed. In Fig. 6.8(a), it is shown that the lowest $\Delta I_{d,sat}$ is observed for the single finger device and then subsequent larger $\Delta I_{d,sat}$ as the number of fingers increases. The trend of $\Delta I_{d,sat}$ among the number of fingers correlates to the $R_{th}$ trend as a function of $nf$ (Fig. 4.9) with a similar steep increase for measured $I_{d,sat}$ degradation from single finger device to the 8 finger device. At higher $nf$, comparatively less significant dependence for the number of fingers is observed. In terms of spacing between the gates, $f_{spac}$ = 294 nm shows the lowest amount of HCD, while $f_{spac}$ = 190 nm showed an optimum trade-off between minimizing both HCD and spacing distance as depicted in Fig. 6.8(b). Devices with larger $w_f$ resulted in enhanced $\Delta I_{d,sat}$ due to self-heating (Fig. 6.8(c)). Similarly, in Fig. 6.8(d), structures with NREP similarly, show improved HCD for a higher number of NREP due to the reduction in $R_{th}$. However, the difference in $\Delta I_{d,sat}$ drift reduces for longer stress times but did not vanish completely. This implies that the chuck temperature does not correspond to

the device temperature. Depending on the raised temperature due to self-heating, which is the function of device geometry, the degradation trends and monitored parameters are influenced.

### 6.2.1 Inclusion of Thermal resistance in Hot-carrier Degradation modeling

With the help of the measured $R_{th}$, the internal device temperature ($T_{device}$) including ambient and rise in temperature due to self-heating can be extracted using equation 4.7. Various device geometries are subjected to worst-case hot carrier stress at different temperatures ranging from -45 °C to 200 °C. The resultant Id,sat degradation is then plotted as a function of the internal device temperature at a specific stress time, as shown in Fig. 6.9. When corrected for the actual stress temperature at the device level, the HCD follows an $exp(-E_a/k_B T_{device})$ trend where $k_B$ is the Boltzmann constant. The $T_{device}$ should not be confused with junction temperature. Junction temperature is conventionally used to represent the peak temperature within a device; however, the self-heating extraction methodology used to extract $R_{th}$ is based on the device's electrical response, reflecting an average device temperature. The plot shows that all the devices with varied $w_f$, $nf$, and $f_{spac}$ are following the trend line showcasing the potential of HCD modeling, including $R_{th}$. It is important to note that the device temperature and $R_{th}$ could vary depending on the temperature gradient of the device to the ambient. In scenarios where the heat dissipation to ambient is hindered or masked, the device temperature would rise, resulting in larger HCD. Therefore, it is imperative to consider the system's thermal performance while taking $R_{th}$ into account for HCD modeling.

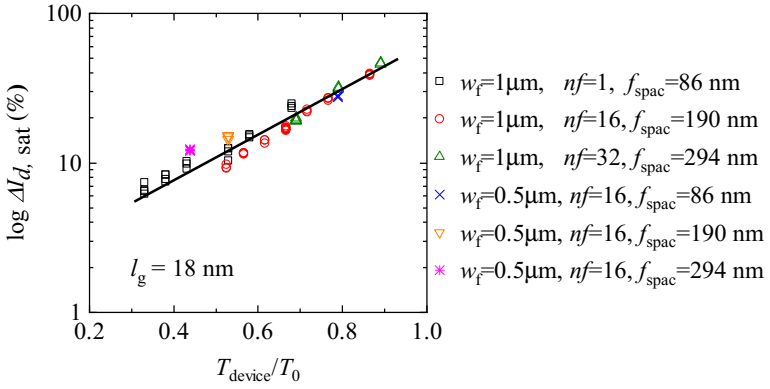


FIGURE 6.9: Correlation of $I_{d,sat}$ degradation with normalized device temperature ($T_{device}$) for different device geometries stressed at worst-case biasing with approximately the same current density. The solid line serves as a guide to the eye for the assumed trend.

### 6.2.2 Convolution of Bias Temperature Instability component in Hot-carrier Degradation

BTI is inherently characterized by stressing the devices at high $V_{gs}$ and elevated temperatures. Although BTI is a function of temperature, self-heating is not a concern during the stress as there is no current in the device. Only during the intermediate monitoring can self-heating occur depending on the measurement conditions. As BTI constitutes a recovery component, the measurement time needs to be as short as possible for accurate characterization. The inherent nature of fast

characterization also aids in minimizing the effect of self-heating during measurement. As $\tau_{th}$ reaching less than 100 ns [203] and the typical fast measurement setups requires few microseconds, the measurement is not entirely free of self-heating. It could lead to a thermally enhanced recovery effect distorting the BTI results [321]. On the other hand, depending on the characterization conditions, the monitored parameter could also be influenced by self-heating. For instance, the monitoring done below or above the $V_{ZTC}$ bias point would have a different effect on $I_d$ (Fig. 4.7). The offset remains throughout the entire BTI characterization. The extent of the offset will depend on the proximity of the monitoring condition to the $V_{ZTC}$ bias point and drift of transfer characteristics due to BTI degradation.

The convolution of parasitic BTI in HCD as a secondary effect of self-heating cannot be ruled out as it is more susceptible to the worst-case stress condition $V_{gs} = V_{ds}$ compared to $V_{gs} = V_{ds}/2$ (in bulk technologies). The correlation of $\Delta I_{d,lin}$ and $\Delta V_{th}$ can serve as an indicator for the qualitative distinction of contributing BTI component in HCD. Arfaoui, Federspiel, Mora, *et al.* in [149] and Federspiel, Rafik, Angot, *et al.* in [312] presented this correlation to distinguish the degradation modes into carrier energy where BTI is classified as low energy and HCD as higher energy ($V_{gs} \leq V_{ds}$) stress mode. The resultant degradation of BTI assumes to be uniform along the channel and predominantly affects the $V_{th}$, while $\Delta I_{d,lin}$ indicates the contribution of localized damage as well.

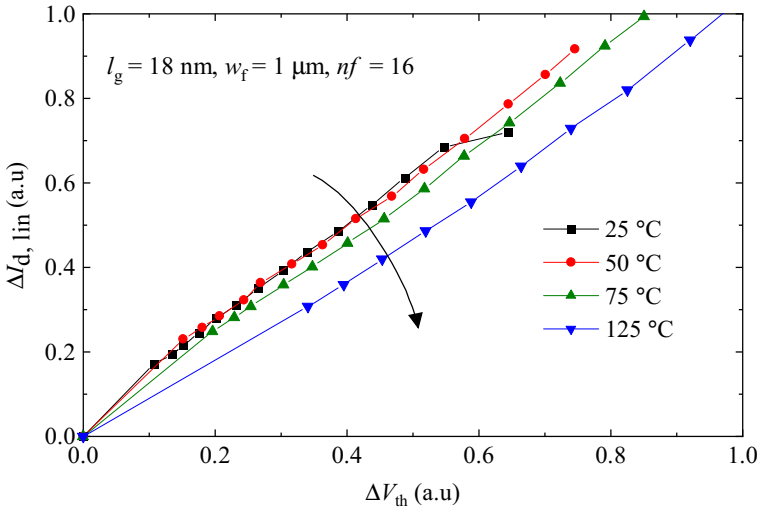


FIGURE 6.10: Correlation of $I_{d,lin}$ degradation evolution in absolute values over stress time with $V_{th}$ shift for a device stressed in HCD mode at different temperatures. Arrow represents the increment of stress temperature.

It can be seen in Fig. 6.10 that as the temperature is increased for the hot carrier stress, $V_{th}$ tends to degrade more for the same amount of drift in $I_{d,lin}$. The $\Delta V_{th}$ and $\Delta I_{d,lin}$ correlation plotted in Fig. 6.11 shows an increase in $\Delta V_{th}$ contribution for the devices exhibiting larger HCD. It is evident from the plots (Fig. 6.11) that the scaling of HCD correlates with the increased temperature arising from geometry-dependent self-heating. Thus, it is important to account for the temperature effect of self-heating in addition to chuck temperature for the characterization and modeling of HCD.

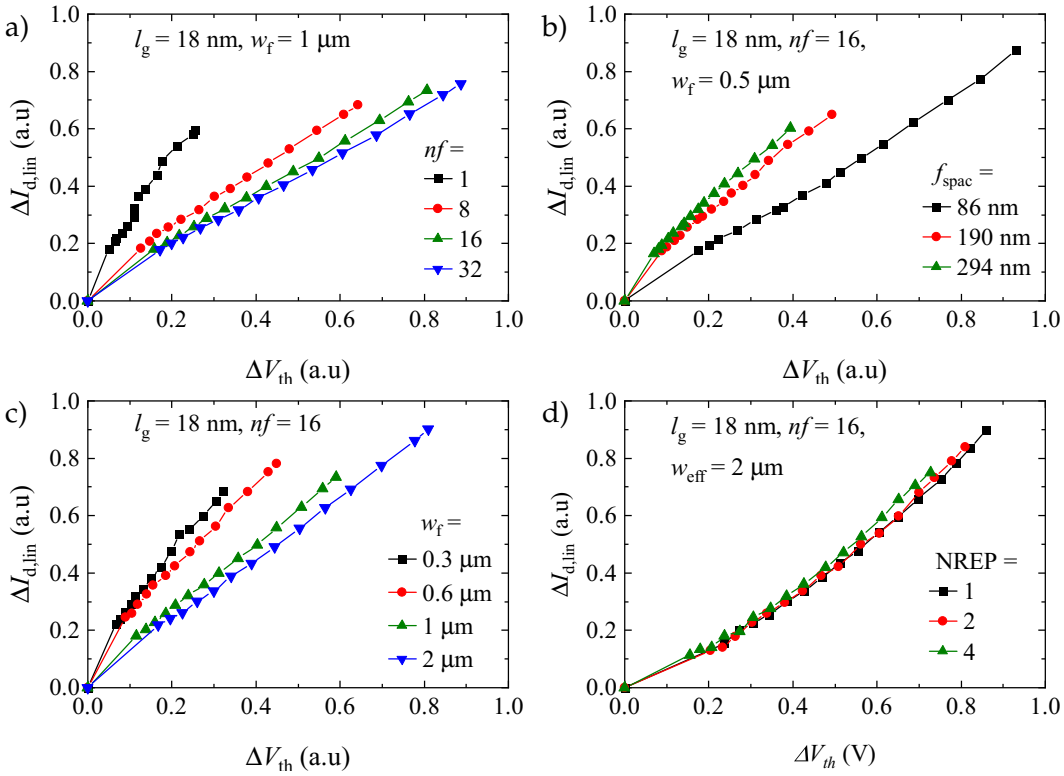


FIGURE 6.11: Absolute magnitude of $\Delta I_{d,lin}$ vs. $\Delta V_{th}$ correlation during HC stress for (a) $nf$ scaling, (b) different $f_{spac}$, (c) $w_f$ scaling, and (d) various NREP. All devices shown in this plot are stressed for the same HC stress condition (Stress C).

### 6.2.3 Effect of Source and Drain Placement in Multi-finger Layout

In devices with a multi-finger layout, the source and drain are shared between adjacent fingers. The implication of these shared source and drain regions in terms of HC reliability should be investigated, as indicated already by the degradation scaling trend with $nf$. To study the effect of sharing a drain or a source region, the two-finger structures are designed with respective shared drain and source regions as shown in Fig. 6.12. Measured values of normalized $I_{d,sat}$ are 149.9 µA/µm, 128 µA/µm, and 132.5 µA/µm for structure with no shared S/D (DUT_N), structure with shared drain (DUT_D), and structure with shared source (DUT_S), respectively. DUT_D and DUT_S exhibit 8.1% and 6.9% lower $I_{d,sat}$, respectively, as compared to the reference DUT_N. Lowering of $I_{d,sat}$ can be associated with self-heating or current crowding effect due to restricted drain and source shared regions leading to increased series resistance.

Fig. 6.13 plots the measured $I_d$ and $V_{th}$ degradation as a function of time for these structures under HC stress. The degradation of $I_{d,lin}$ is comparable among these structures (Fig. 6.13(a)). However, for $I_{d,sat}$, $V_{th,lin}$, and $V_{th,sat}$, the DUT_D degrades more than DUT_S and DUT_N. DUT_S shows comparable degradation of all DC parameters to the reference structure. The higher amount of degradation in DUT_D can be due to the following reasons: (i) the shared drain region could experience the damage from the hot carriers of both channel region; in other words, an interaction of both degraded regions on the respective sides of the shared drain leads to an enhanced overall degradation (ii) current crowding effect under the shared drain leading to an enhanced electric field and eventually higher degradation (iii) self-heating in such short channel devices lead to the creation of

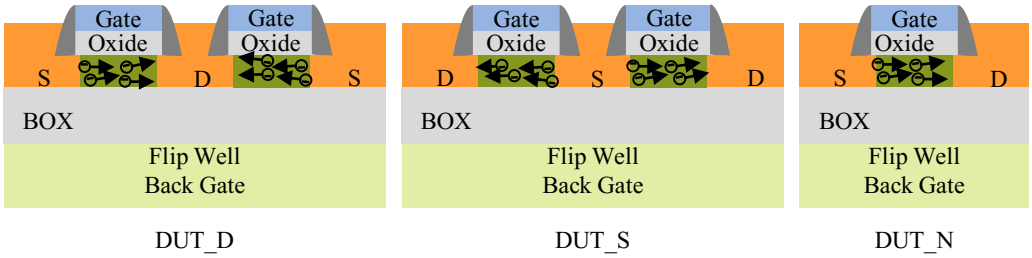


FIGURE 6.12: Illustration of n-MOSFET structures designed to evaluate the effect of shared source and drain. DUT_D and DUT_S are two finger structures with alternate drain and source shared region compared to a reference structure DUT_N. Electrons in the channel region depict the direction under HC stress conditions.

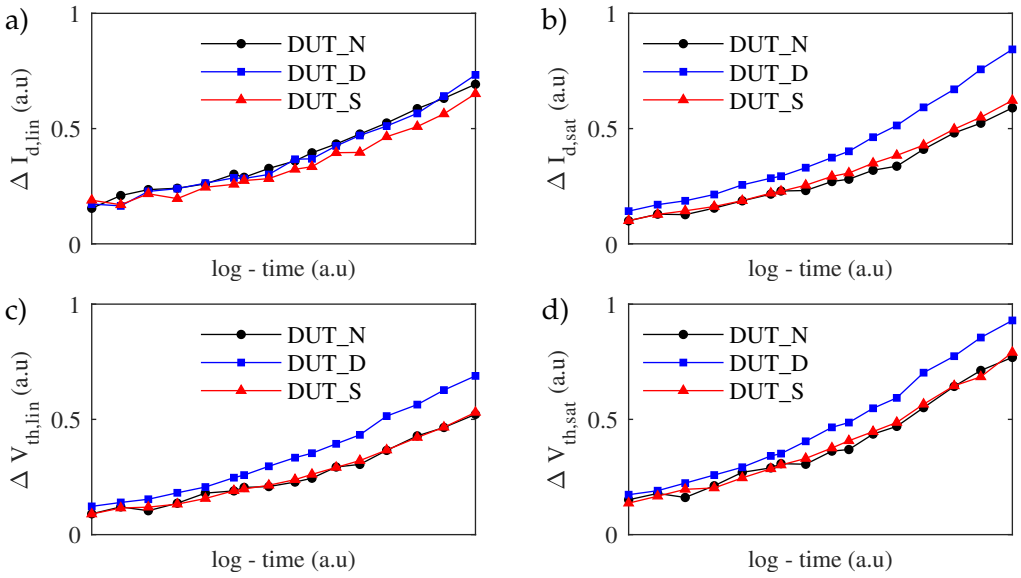


FIGURE 6.13: Plot of time-resolved degradation magnitude of DC parameters: (a) $I_{d,lin}$, (b) $I_{d,sat}$, (c) $V_{th,lin}$, and (d) $V_{th,sat}$ for structures shown in Fig. 6.12. All devices are stressed for the same HC stress condition.

local hot-spot near drain region as explained in section 4.2, this local hot-spot in case of shared drain raise the temperature of the device from both channels and result in more stringent HC stress condition. The second reason is reported in [322] and demonstrated through 2D simulations in a bulk device. The third reason seems more plausible in the studied devices as the interaction of degraded region will need extremely high energy carriers and less possibility of current crowding in FDSOI devices with un-doped channel and source/drain regions grown by dual in-situ doped epi process.

In order to validate the hypothesis of thermally coupled local hotspot induced by self-heating in the shared drain structure, 2D technology computer-aided design (TCAD) simulations have been performed. The layout of DUT_N, DUT_D, and DUT_S contains dummy gates that are generated by standard RF parameterized cell (PCell). The dummy gates are essential to consider for the self-heating simulations as it defines the vicinity of reflective boundary to the heat source. The reflective boundary in simulation also imitates the presence of STI in the actual device. In these simulations, the heat generation and thermal coupling are not calibrated with experiments. The main aim of the simulation is to compare and

conceptually understand the impact of heat generation and thermal coupling in the respective structures. In addition, the effects of middle-of-line (MOL) and BEOL are ignored to speed up the process and device simulations. An ideal surface thermal conduction is assumed at the gate, drain, and source contacts. Fig. 6.14 shows the simulated lattice temperature profile in DUT_D and DUT_S structures. The high-temperature hotspots are visible near the drain regions in both structures [323]. The relative comparison of local temperature in the channel (lateral direction) between the two structures is plotted in Fig. 6.15. The peak temperature near the drain region in a structure with a shared drain is higher compared to the structure with a shared source. A relatively higher peak temperature can result in higher HCD. Further, the rise in peak temperature for DUT_D can be explained as (i) current flowing through a single drain region resulting in a higher number of scattering events (ii) effective thermal coupling of local hotspot near drain region due to close vicinity.

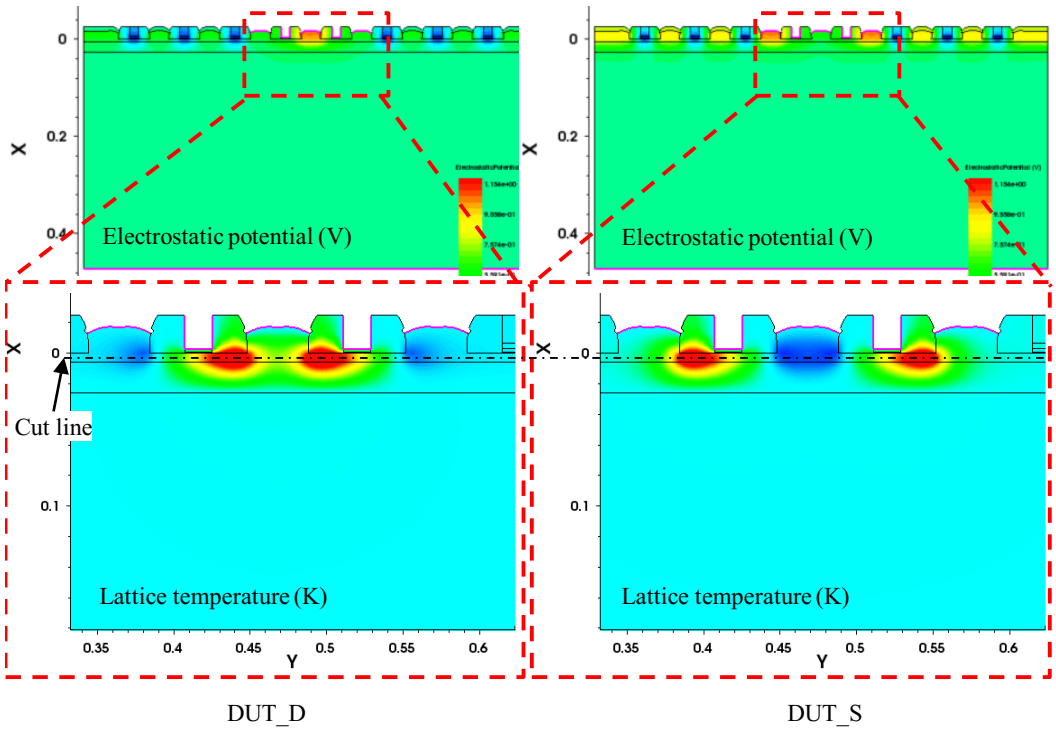


FIGURE 6.14: 2D cross-section of simulated layouts of DUT_D and DUT_S structures. The top images show the complete structure with simulated electric potential. The bottom images show the zoomed-in active area of the whole structure with lattice temperature profile in on-condition. Blue and red colors represent the lowest and maximum values, respectively.

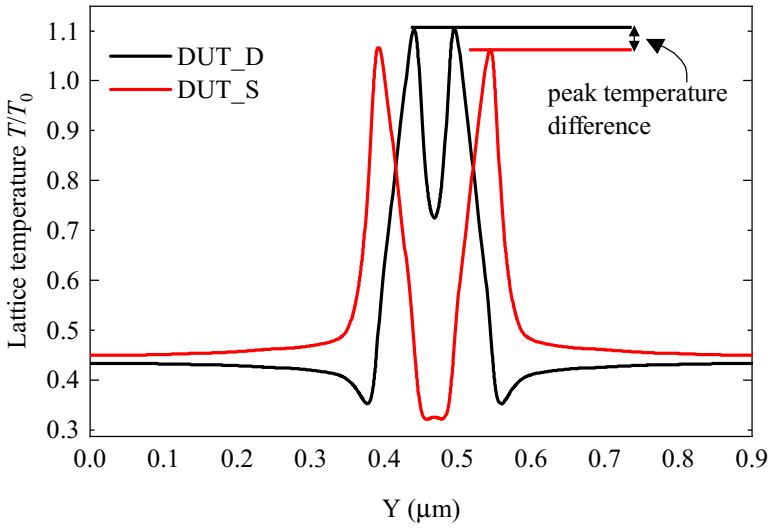


FIGURE 6.15: Lattice temperature profile along Y-direction for the two-finger structure with shared drain and shared source. The profile is extracted for the cut line shown in Fig. 6.14.

## 6.3 $V_{th}$ turn-around effect in p-MOSFET

Hot carrier degradation typically results in the decrement of drain current and increase of threshold voltage due to charge stored in bulk oxide traps and interface traps. However, in some cases, an increased contribution of inverse polarity stored charges in the interface and oxide traps results in turn-around phenomenon. The amphoteric nature of interface traps depending on silicon surface potential has been used to explain the turn-around behavior in n-MOSFET subjected to radiation damage [324]. The turn-around phenomenon is observed under hot carrier stress [130], [135], [325] and NBTI stress [326] in n-MOSFETs.

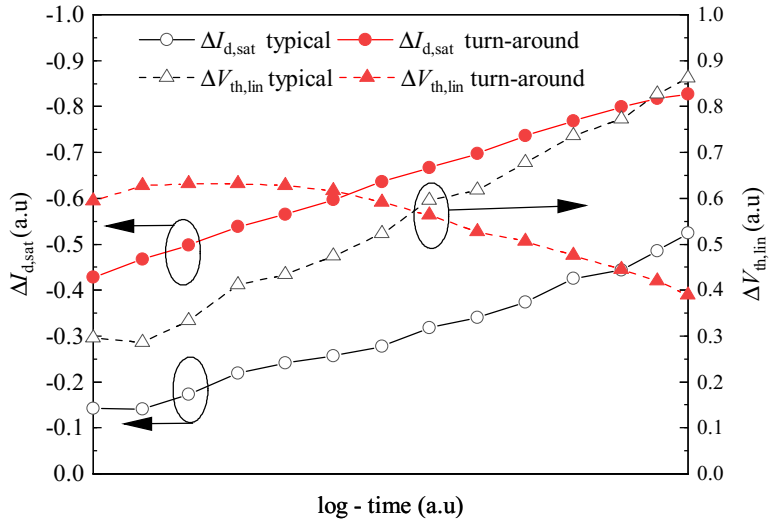


FIGURE 6.16: Plot of $\Delta I_{d,sat}$ (circle marker, left y-axis) and $\Delta V_{th,lin}$ (triangle marker, right y-axis) as a function of HC stress time. The figure demonstrates the measured typical (hollow marker) and turn-around (solid marker) phenomenon in terms of the $\Delta I_{d,sat}$ and $\Delta V_{th,lin}$ degradation. For the turn-around characteristics, the $I_{d,sat}$ continues to decrease with stress time while $V_{th,lin}$ first increase and then start decreasing.

The turn-around is not a commonly observed phenomenon and rarely reported in the literature. Fig. 6.16 illustrates the typically measured and turn-around phenomenon under HC stress on a p-MOSFET. It can be observed that although $I_{d,sat}$ keeps on degrading, the turn-around phenomenon is visible for the $\Delta V_{th}$. In literature, [130], [326] this phenomenon is associated with the interplay of interface traps and oxide traps contributions. For the case of n-MOSFET under hot carrier stress, the secondary generated holes due to impact ionization governed by single and multiple particle processes are responsible for the reversal of $V_{th}$ degradation [130], [327]. However, only p-MOSFET exhibits the $V_{th}$ turn-around phenomenon for the devices investigated in this study. The turn-around phenomenon is p-MOSFET similarly can be associated with the impact of secondary generated electron resulting from accelerated holes' impact ionization. It is interesting to note that the turn-around phenomenon depends on stress voltage, stress time, temperature, and device layout parameters. However, the device layout parameters can be directly correlated to the temperature because of transistor geometry-dependent self-heating.

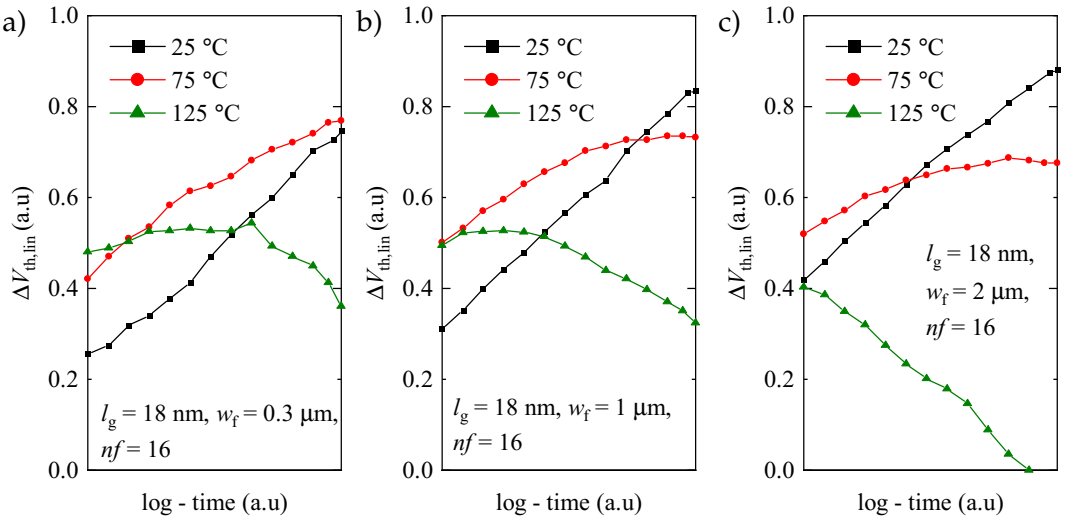


FIGURE 6.17: Turn-around phenomenon of $\Delta V_{th,lin}$ in the p-MOSFETs plotted vs. HC stress time at different temperatures for (a) $w_f$ = 0.3 µm, (b) $w_f$ = 1 µm, and (c) $w_f$ = 2 µm. The stress voltage is the same across all devices and temperatures.

The time-resolved $I_{d,sat}$ degradation for the p-MOSFET shown in Fig. 6.1(b) indicates the saturation of $\Delta I_{d,sat}$ for longer stress times and a prominent scaling of saturation effect with stress voltage. The saturation of $\Delta I_{d,sat}$ is related to the $V_{th}$ turn-around phenomenon, and for the case of stronger $V_{th}$ reversal, even a recovery of $I_{d,sat}$ degradation can be observed for Stress C in Fig. 6.1(b) and Fig. 6.2. The dependence of the $V_{th}$ turn-around phenomenon on temperature can be clearly observed in Fig. 6.17 and Fig. 6.18. In all of these plots, the room temperature measured $V_{th,lin}$ degradation does not show a turn-around phenomenon, while as the temperature rise, the $V_{th,lin}$ starts to saturate and eventually turn around with respect to the stress time. Similar temperature dependence is reported in [130], [326]. The trapping and de-trapping in oxide bulk are governed by non-elastic trap-assisted tunneling [328]. High temperature, which accelerates the trapping and de-trapping in bulk oxide, explains the observed temperature dependence [169], [328]. Fig. 6.17 plot the evolution of the turn-around phenomenon with respect to the gate width. The turn-around phenomenon progressively becomes

stronger for the larger widths, which can be associated with the increased temperature caused by more pronounced self-heating. A similar trend is observed with respect to the number of fingers (Fig. 6.18). For the device with $nf$ = 1, no turn-around phenomenon is observed, while for $nf$ = 32, $\Delta V_{th}$ jumped to a constant increase for $T$ = 75 °C and $T$ = 125 °C, $\Delta V_{th}$ starts to recover after an initial increase. Note that for all cases, the $\Delta V_{th}$ initially increases for the very first measurement after the application of HC stress. The very first measurement is obtained after several seconds (> one digit) of stress time. However, it is plausible that the turn-around phenomenon starts even before few seconds, especially for the case of Fig. 6.17(c) and Fig. 6.18(c).

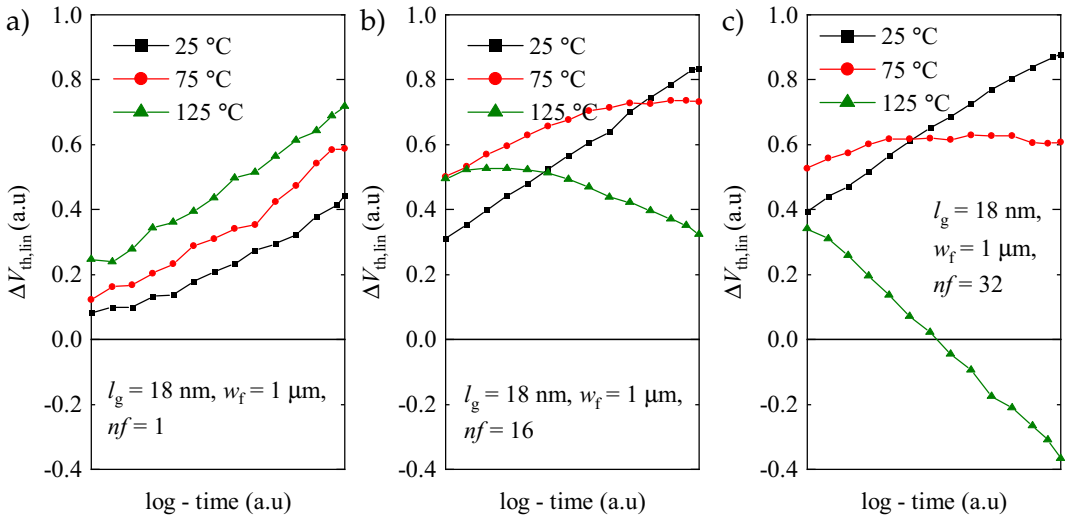


FIGURE 6.18: Behavior of turn-around phenomenon with respect to the number of fingers scaling. $\Delta V_{th}$ vs. $t$ is plotted for n-MOSFET at different temperatures for (a) $nf$ = 1, (b) $nf$ = 16, and (c) $nf$ = 32.

# Chapter 7

# Deconvolution of Hot-carrier Degradation and Bias Temperature Instability using Scattering parameters

Throughout the development of semiconductor devices, two main degradation mechanisms HCD and BTI have remained in the focus, especially when FEOL reliability is considered. With the advancement and improvement in process generations for achieving higher efficiency or lower power consumption, these degradation mechanisms have competed to be a candidate who should be given higher importance than others. Initially, HCD was treated as the foremost degradation mechanism [134], [329], [330] and with the technology scaling, BTI start to become a growing concern [331], [332] especially with the addition of nitrided gate oxide [168], [174]. HCD evolved from a single-particle mechanism to a multi-particle mechanism in ultra-scaled dimensions and remained one of the key players in reliability. The dominance of either BTI or HCD is linked to a certain application's operating conditions. In general, BTI mainly affects the digital and combinational logic circuits [330], [333].

On the other hand, analog applications operate over a range of gate/drain bias conditions. However, this range of the bias is specific to a certain class of analog applications such as an oscillator, amplifier, switch, current mirror, etc. Thus, becoming more prone to HCD effects [330], [334]. Nevertheless, in a real use case, depending on the operating conditions, the devices encounter several types of stresses. The final effect on performance is aggregated contribution of multiple degradation mechanisms. The knowledge of each aging mechanism optimizes processing technologies and deploys counterbalancing techniques/practices particular to the dominant mechanism. It is not trivial to distinguish and experimentally extract the number of different stress types while a device is in a typical use case condition where the bias conditions are not related to a specific stress mode. Measurement and set up artifacts also occasionally lead to incorrect analysis and conclusions, e.g., applying BTI stress via two different SMUs for source and drain on large device results in an HC stress component due to a slight mismatch between SMU voltages. In this study, it is observed that the same SMU must be used for source and drain during the BTI stress to avoid a parasitic HCD contribution. As the S-parameter analysis of BTI (section 5.1.3) and HCD (section 6.1.2) stress reveals a unique signature related to each stress mode, it can be exploited to distinguish the contribution of the individual stress mode. In literature, there exist few reports about such experimental-based separation

techniques and methodologies [335], [336]. In most cases for such analysis, circuit simulation tools are used assuming quasi-static approximation for the applied waveform and resultant degradation effects [337], [338].

This chapter highlights the unique effects seen in S-parameter analysis after HC and BTI stress. For verification and complementing the knowledge about observed effects, TCAD simulations are carried out using the Synopsys Sentaurus tool. Various trap types and their corresponding influence on simulated small-signal parameters are analyzed. The last part of this chapter demonstrates an experimental approach to validate the utilization of S-parameters for the deconvolution of HC stress contribution.

## 7.1 Small-Signal Parameter Signatures for Hot-carrier Degradation and Bias Temperature Instability

Through a small-signal model, different components and regions of a transistor and its associated behavior can be accessed. These model components include physically existing entities such as gate oxide capacitance, and series resistances. Other components represent more behavioral related entities such as conductance and distributed capacitances/resistances. Due to applied voltage and temperature stress, such components' perturbations can reveal information about the nature and localization of created defects. As shown in the previous chapters, BTI and HCD share many resultant effects, especially in conductances and bias-dependent shifts. However, two components that stand out to show different behavior are series resistances and distributed gate capacitances. A simple, well-established difference of defect localization between HC and BTI stress can be seen through these components' lenses. As shown already in Fig. 6.6, $C_{gs}$ and $C_{gd}$ exhibit an explicit change of contributing ratio to $C_{gg}$ after HC stress arising from the local change of flatband voltage due to drain side defects. The unique signature of a relatively larger increase in series drain resistance as compared to the source resistance due to HC stress can be seen in Fig. 6.4 and Fig. 5.9. Extraction of these individual components, especially $C_{gs}$ and $C_{gd}$, cannot be effortlessly done without acquiring S-parameters in nano-scaled devices with such short gate lengths and gate widths. In modern nano-scaled devices with ultrathin gate oxide, the gate leakage currents severely affect the accuracy of Charge Pumping and C-V measurement techniques [119], [339]. Hence, S-parameters opportune the distinction of individual stress mode contribution using the exclusive signature of HCD mode.

## 7.2 TCAD Dynamic Simulation of Defects

TCAD tools are well established and readily used for simulating the semiconductor fabrication process and device behavior. Within device simulations TCAD tools, various reliability aspects can be simulated [340] using incorporated models leading to the creation of electrical field and thermal driven bulk and interface traps. Modeling, calibration, and verification of such simulated behavior with the one acquired through experiments is out of scope for this study. However, a simple approach to investigate such defects can be adopted by manually introducing the traps and charges that mimic the degraded device. This would serve the purpose as the intention is to analyze and qualitatively compare the effects on small-signal analysis. Using this approach, various traps are simulated with varying

concentrations and locations within different materials and interfaces. The 2D simulation is carried out on a standard FDSOI device structure with similar dimensions and operating voltages to one characterized throughout this work. The device simulator supports the frequency domain simulation at each DC step for given frequency points by applying small-signal analogous to the RF characterization. The output results are in the form of small-signal conductances ($A$) and capacitance matrix ($C$) for all different contact to contact (also defined as ports in Fig. 3.1) combinations. This equates to the Y-parameters matrix as:

$$Y = A + 2\pi f C \tag{7.1}$$

The capacitance matrix is computed based on the charge-based capacitance model [246] ($C_{ij} = -\partial Q_i / \partial V_j$ for terminals $i \neq j$). To simulate the behavior of BTI stressed devices, fixed charges (FC) are introduced at the $Si/SiO_2$ interface. However, to mimic the localized nature of HCD, the interface traps are placed at the gate oxide and SOI interface near the drain region. The variation of interface traps location is studied in the following sections. It should be noted that the simulation is aimed at capturing the electrons; hence the acceptor-type interface traps are needed. Having an interface trap energy of zero with reference to the conduction band will place the traps at the edge of the silicon conduction band. For the simulations performed in this work, the trap energy of 0.2 eV with reference to the conduction band edge is chosen. It is important to note that the RF small-signal capacitances are simulated at $f$ = 20 GHz to match with the extraction frequency of experimental data presented in chapter 5 and 6. At such a high frequency, the traps are initially occupied and cannot follow the variation of applied small-signal, i.e., fixed interface trap state.

### 7.2.1 Fixed Charges

For a first order representation of the PBTI effect, negatively charged interface states are considered, which constitute the dominant contribution of the permanent BTI degradation component. FC are placed uniformly throughout the $Si/SiO_2$ interface, as marked in Fig. 7.1. The simulated electric field profile across the lateral direction for two different sheet charge concentration is shown. Due to placed charges, the electric field under the gate region is uniformly reduced, resulting in the $V_{th}$ increase of 34 mV and 187 mV for the charge concentration of $1 \times 10^{12}$ $cm^{-2}$ and $5 \times 10^{12}$ $cm^{-2}$, respectively. A similar effect of $\Delta V_{th}$ is also seen in the plot (Fig. 7.2) of small-signal capacitance vs. gate bias. The capacitances exhibit a simple bias-dependent shift which scales with the charge concentration.

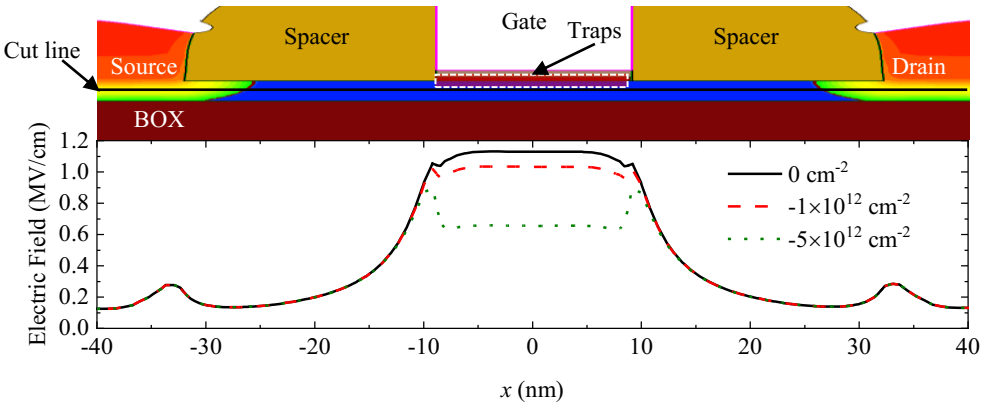


FIGURE 7.1: Plot of simulated lateral electric field profile (extracted at the cut line) for different fixed charges concentration. The dotted rectangle box highlight the region where FC are placed.

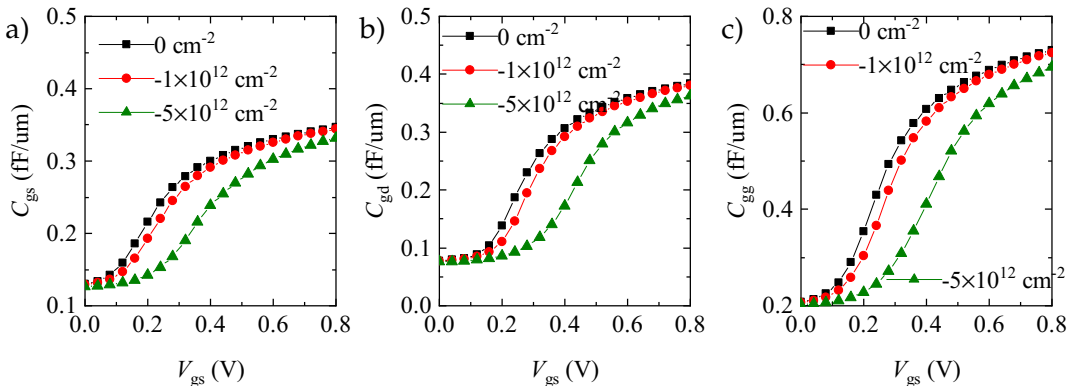


FIGURE 7.2: Simulated small-signal capacitances (a) $C_{gs}$, (b) $C_{gd}$, and (c) $C_{gg}$ for an n-MOSFET plotted over gate bias for different concentrations of FC. The capacitances are extracted at $f$ = 20 GHz and $V_{ds}$ = 0.05 V.

### 7.2.2 Interface Traps near Gate

Interface traps are placed in the 4.5 nm vicinity of channel length towards the drain end, as shown in Fig. 7.3. It can be seen from the lateral electric field profile that due to placed interface trap charges (ITC), the electric field under that region is reduced due to an increase of local flatband voltage. Due to localized defects, $V_{th,lin}$ and $V_{th,sat}$ shift differently. Extracted values of $\Delta V_{th,lin}$ and $\Delta V_{th,sat}$ are (8 mV, 21 mV, 34 mV) and (3 mV, 8 mV, 15 mV) for the trap concentration of ($1 \times 10^{12}$ cm$^{-2}$, $2 \times 10^{12}$ cm$^{-2}$, $3 \times 10^{12}$ cm$^{-2}$) respectively. The reduction of electric field scales with the charge concentration and the corresponding effect on capacitance behavior is shown in Fig. 7.4. Due to ITC near the drain region, the $C_{gs}$ does not show significant change, while a noticeable reduction of $C_{gd}$ and a rather slight decrease of $C_{gg}$ is observed. The size of the area where the interface traps are placed also reflects the amount of change visible in capacitances. For a small region of the defects and lower density of interface traps, the capacitances become less sensitive (see Appendix D).

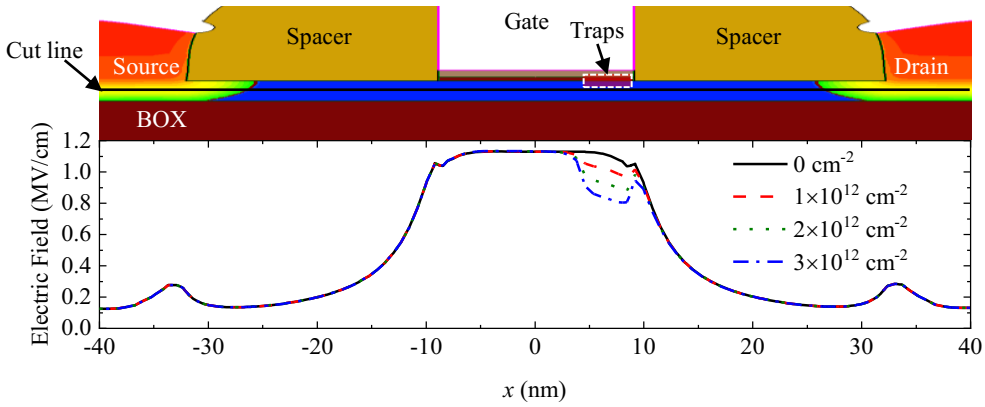


FIGURE 7.3: Electrical field profile at the cut line for the interface traps introduced at the gate oxide and SOI interface within the cross-section of 4.5 nm.

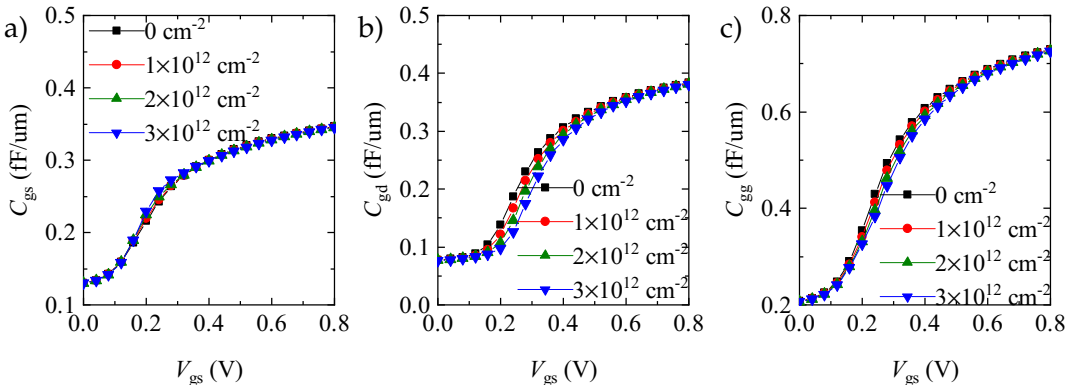


FIGURE 7.4: Simulated (a) $C_{gs}$, (b) $C_{gd}$, and (c) $C_{gg}$ for an n-MOSFET plotted vs. $V_{gs}$ for different concentrations of ITC at the gate oxide and SOI interface. The capacitances are extracted at $f$ = 20 GHz and $V_{ds}$ = 0.05 V.

### 7.2.3 Interface Traps near Spacer Region

For the case of the accelerated electric field under HC stress, the high carriers tend to extend the damaged region to the interface of SOI and spacer. The perturbation of the electric field profile caused by interface traps near the spacer region is shown in Fig. 7.5. Interface traps are placed with a 4.5 nm region starting from the end of the overlapping gate to the channel region. The resultant shift in $\Delta V_{th,lin}$ and $\Delta V_{th,sat}$ is extracted as (8 mV, 22 mV, 43 mV) and (3 mV, 8 mV, 15 mV) for the trap concentration of ($1 \times 10^{12}$ cm$^{-2}$, $2 \times 10^{12}$ cm$^{-2}$, $3 \times 10^{12}$ cm$^{-2}$), respectively. $V_{th,lin}$ and $V_{th,sat}$ increase to a similar extent as shown for the case of ITC near gate region except for the $\Delta V_{th,lin}$ for $3 \times 10^{12}$ cm$^{-2}$. Although with similar $V_{th}$ degradation, the changes in capacitances are amplified for the case of ITC near the spacer region, as depicted in Fig. 7.6. The behavior of $C_{gg}$ remains the same while the increment of $C_{gs}$ and $C_{gd}$ is clearly visible. Notice the increase of $C_{gs}$ for trap concentration of $3 \times 10^{12}$ cm$^{-2}$, the shape of the curve starts to show a hump at approx mid-range of $V_{gs}$. The changes in small-signal capacitances also depend on these traps' allocated size and location within the spacer region interface. The closer it is to the drain region, the stronger the effect will be (see Appendix D). For the case where the traps' location is in very close vicinity to the drain region, the electric field near the source region starts to increase (Fig. D.5).

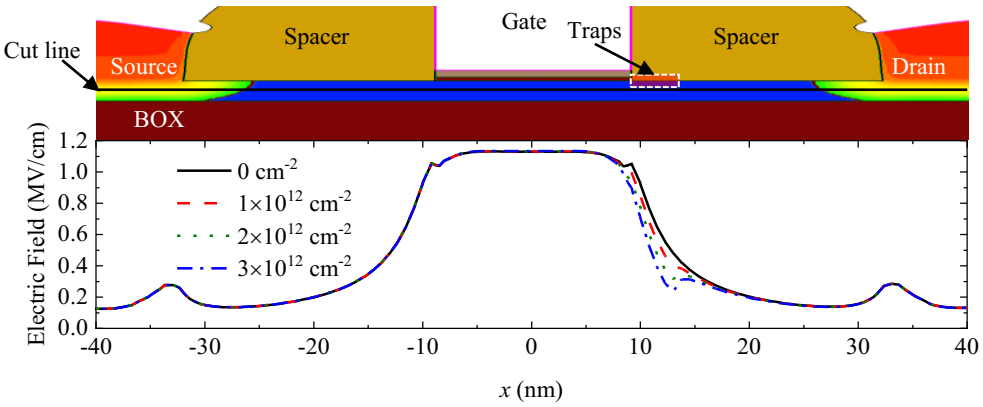


FIGURE 7.5: Electrical field profile at the cut line for the interface traps placed at the interface of spacer and SOI within the cross-section of 4.5 nm.

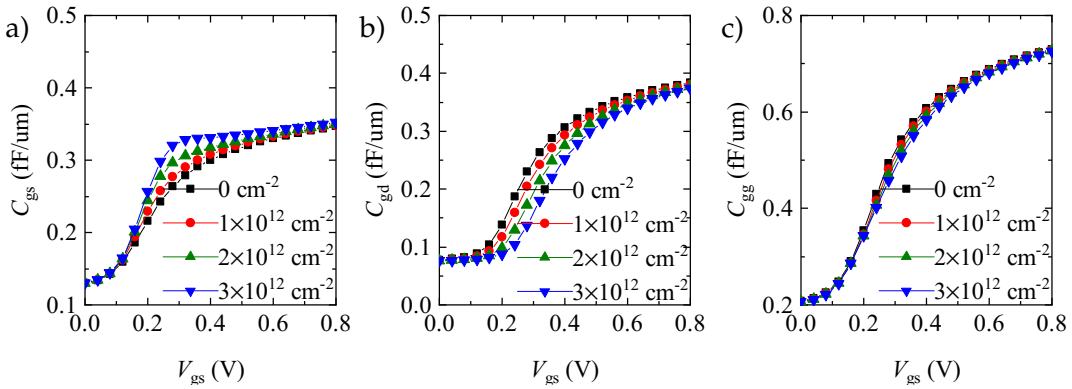


FIGURE 7.6: (a) $C_{gs}$, (b) $C_{gd}$, and (c) $C_{gg}$ vs. $V_{gs}$ for an n-MOSFET with different concentrations of ITC at the interface of spacer and SOI. The capacitances are obtained from the TCAD simulation at $f$ = 20 GHz and $V_{ds}$ = 0.05 V.

### 7.2.4 Combination of Traps

To simulate a mixture of BTI and HC stress, the fixed charges and interface trap charges of different locations are placed in a combined fashion. As shown in Fig. 7.7, the resulting electric field profile exhibits the effects of an individual trap scheme (in terms of type and localization), as discussed in the previous sections. Similarly, the small-signal capacitance in Fig. 7.8 also shows the corresponding combined changes of each trap effect. The $V_{th}$ shift caused by the combination of these traps is additive, as listed in table 7.1. It is important to emphasize that there is no interaction between these traps at such high frequencies and thus enables the separation of their exclusive effect.

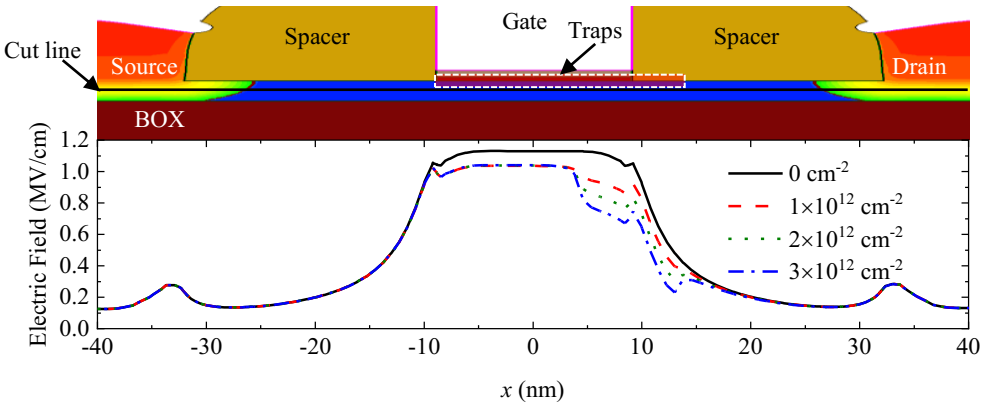


FIGURE 7.7: Plot of simulated lateral electric field for the combination of traps shown in Fig. 7.1, Fig. 7.3, and Fig. 7.5

TABLE 7.1: Resultant increase in $V_{th,lin}$ after introducing different types of traps at different locations and concentrations. The trap concentration for FC is fixed to $1 \times 10^{12}$ cm$^{-2}$.

| **Trap concentration** | **FC** | **ITC near gate** | **ITC near spacer** | **Summation** | **Combined Simulation** |
|---|---|---|---|---|---|
| $\times 10^{12}$ cm$^{-2}$ | $1 \times 10^{12}$ cm$^{-2}$ $\Delta V_{th}$(mV) | $\Delta V_{th}$(mV) | $\Delta V_{th}$(mV) | $\Delta V_{th}$(mV) | $\Delta V_{th}$(mV) |
| 1 | 34 | 8 | 8 | 50 | 51 |
| 2 | 34 | 21 | 22 | 77 | 78 |
| 3 | 34 | 34 | 43 | 111 | 113 |

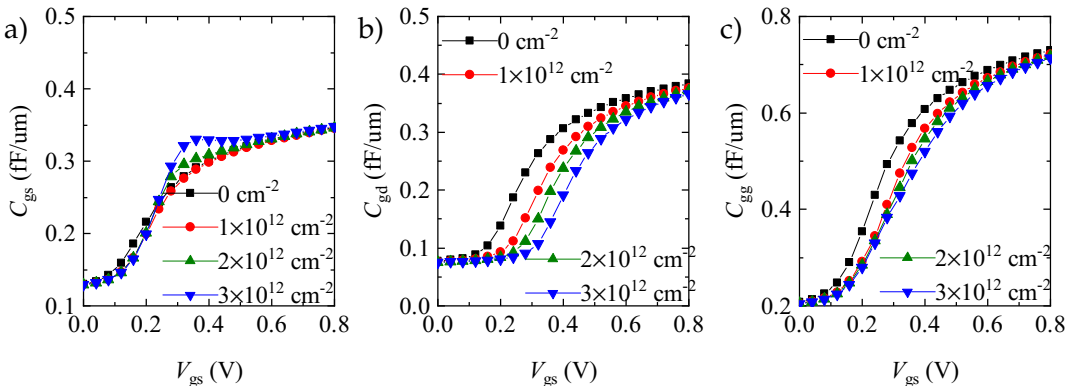


FIGURE 7.8: Behavior of small-signal capacitances (a) $C_{gs}$, (b) $C_{gd}$, and (c) $C_{gg}$ with respect to $V_{gs}$ simulated for a combination of different trap profiles as shown in Fig. 7.7. The capacitances are computed at $f$ = 20 GHz and $V_{ds}$ = 0.05 V.

### 7.2.5 Drain Series Resistance effect

Fig. 7.9 shows the effect of added extra series resistance at the drain terminal on the capacitance behavior. The effect of pure series drain resistance increment perfectly counterbalances the increase in $C_{gs}$ to the decrease in $C_{gd}$. The shift of capacitance effect is mainly visible at higher gate biases, contrary to the shift in capacitances observed previously in the mid-range gate bias. This can be explained by the addition of series resistance which is not influenced by the defect in the gate oxide,

eliminating the non-uniformity of flatband voltage. An increment of drain series resistance also occurred due to created defects and traps; however, the capacitance changes only arise from altered electrostatic potential.

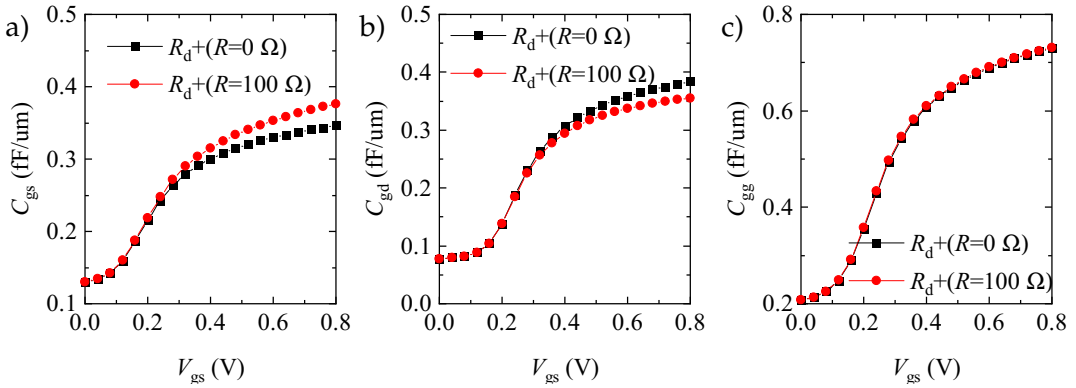


FIGURE 7.9: Effect of adding series drain resistance of 100 Ω on (a) $C_{gs}$, (b) $C_{gd}$, and (c) $C_{gg}$ plotted vs. $V_{gs}$.

### 7.2.6 $\Delta V_{th}$ Correction

To filter out the shift of bias point due to traps and charges, $\Delta V_{th}$ corrected capacitances are plotted in Fig. 7.10. It can be observed that $C_{gg}$ after $\Delta V_{th}$ compensation (Fig. 7.10(c)) shows a slight increase at the lower gate biases for the simulation having a combination of different trap profiles. The $\Delta V_{th}$ shift entirely compensates for FC-related changes. An apparent vertical increase of $C_{gs}$ is observed after $\Delta V_{th}$ correction for the interface traps. $\Delta V_{th}$ corrected $C_{gd}$, on the other hand, depicts slight decrement for the interface traps.

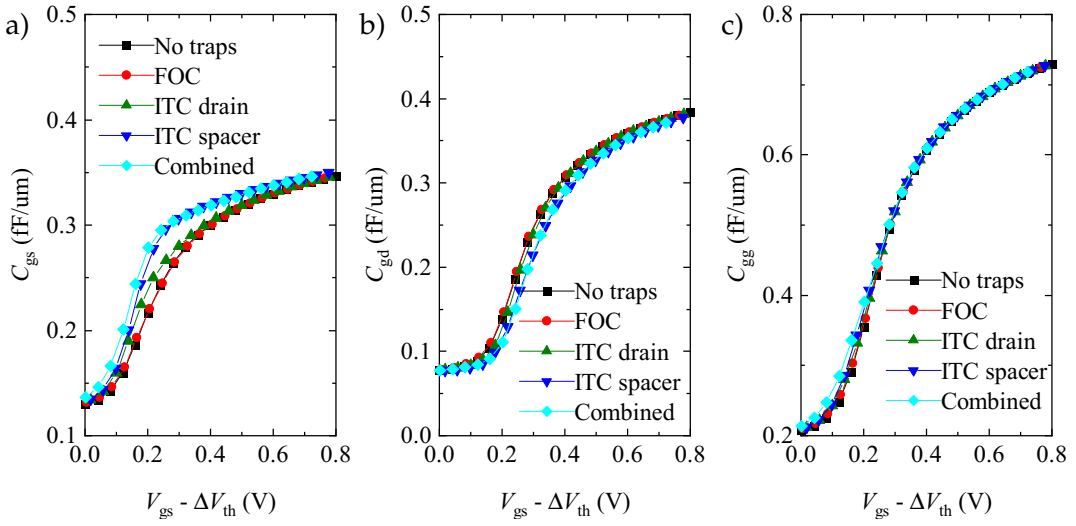


FIGURE 7.10: Plot of $\Delta V_{th}$ corrected capacitance (a) $C_{gs}$, (b) $C_{gd}$, and (c) $C_{gg}$ with respect to $V_{gs}$ shown for different trap profiles.

## 7.3 Empirical Modeling based deconvolution of Hot-carrier Degradation

After validation of experimentally observed changes with TCAD simulations, a measurement methodology can be devised to utilize the unique signature of interface traps generated by HC stress. For such methodology, the capacitance and resistance changes are empirically modeled to quantize and correlate with applied HC stress using the power-law model as follows:

$$\Delta RF_parameters = a \times \Delta DC_parameters^{b} \tag{7.2}$$

$$\Delta RF_parameters = a \times \frac{t}{t_o}^{b} \tag{7.3}$$

where $a$ and $b$ are the (dimensionless) fitting parameters. The empirical correlation of $\Delta C$ and $\Delta R$ can be established with the stress time or with degraded DC parameters such as $V_{\text{th,lin}}$, $V_{\text{th,sat}}$, $I_{\text{d,lin}}$, or $I_{\text{d,sat}}$. Several devices are stressed in HCD mode for the different duration to formulate the correlations. Fig. 7.12(a) shows the $\Delta V_{\text{th}}$ corrected shift of small-signal capacitances as a function of $V_{\text{th,lin}}$ shift caused by HC stress. The trend of increased $C_{\text{gs}}$, $C_{\text{gg}}$, and decreased $C_{\text{gd}}$ matched well with the TCAD simulations. Another parameter of interest, i.e., change of series drain resistance, is shown in Fig. 7.12(b). It can be seen that the measurement data points are rather coarse. To improve the accuracy of empirical relation, the individual effect can be merged together. Fig. 7.12(c) shows the difference of capacities component and summation of series resistance components to reflect an enhanced signal. Similar relation of $\Delta V_{\text{th}}$ corrected small-signal component changes with respect to stress time is shown in Fig. 7.11.

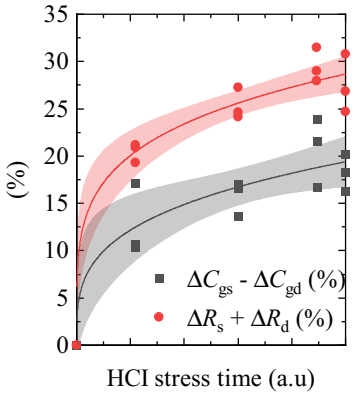


FIGURE 7.11: $\Delta V_{\text{th}}$ corrected $\Delta C$ and $\Delta R$ plotted vs. HC stress duration.

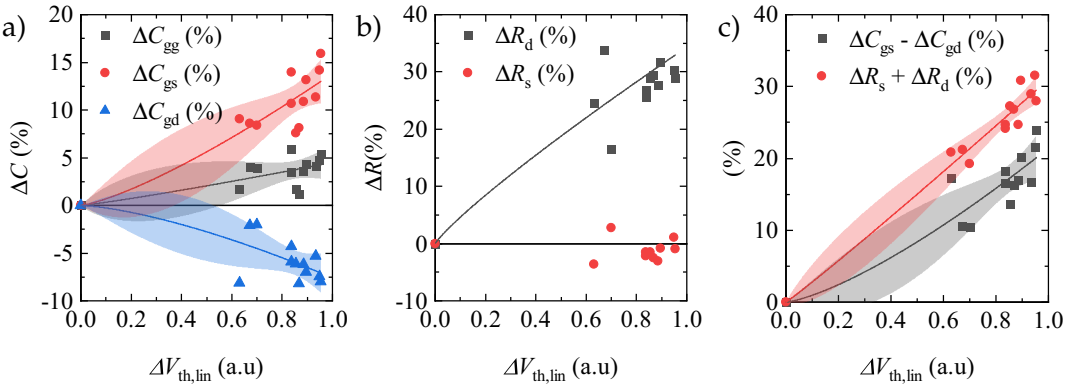


FIGURE 7.12: Plot of $\Delta V_{\text{th}}$ corrected shift of (a) $C$ and (b) R (c) summation of $\Delta C$ and $\Delta R$ effect plotted vs. $V_{\text{th,lin}}$ degradation caused by HC stress of different duration.

To validate the experimental deconvolution of HCD and BTI, a simple form of mixed stress sequence shown in Fig. 7.13 is devised with varying duration of

different stress modes. S-parameters are acquired before and after the entire stress sequence. Initially, the n-MOSFETs are stressed with HC followed by the subsequent PBTI stress. The duration of each stress is depicted in Fig. 7.13. After stress, the small-signal parameters are corrected for the resultant $V_{th}$ shift. The final $\Delta V_{th}$ includes the $\Delta V_{th}$ contribution from both BTI and HCD. The contribution of BTI is assumed to be only $V_{th}$ shift, as demonstrated in section 5.1.3 and TCAD simulation of FC. Using the established empirical relation of $\Delta$RF with respect to stress time and degraded DC parameters (equation 7.3), the contribution of HCD is computed from $V_{th}$ corrected $\Delta$C and $\Delta$R. The computed HCD component from the entire stress sequence is plotted in Fig. 7.14. The extracted duration of HC stress shows good matching with the actual duration of stress. Better accuracy is achieved using the series resistance component. Similarly, the HCD contribution of other degraded parameters can be computed using equation 7.2. The presented deconvolution methodology considers the following assumptions: (i) in terms of BTI stress, no contribution of interface traps (which could result in $\mu_{eff}$ degradation or degradation of parameters other than $V_{th}$). (ii) The experimental validation is performed in a stress type sequence starting with HC followed by BTI. As the degradation component due to bulk oxide traps and interface traps under HC stress are a function of stress time, the method might need calibration in case of alternating BTI and HC stress.

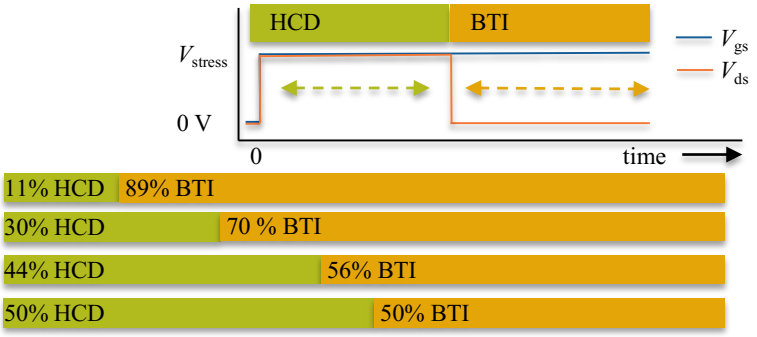


FIGURE 7.13: Mixed sequence of BTI and HC stress modes to validate the deconvolution methodology. Four different variations of BTI to HC stress duration are applied to the n-MOSFET devices.

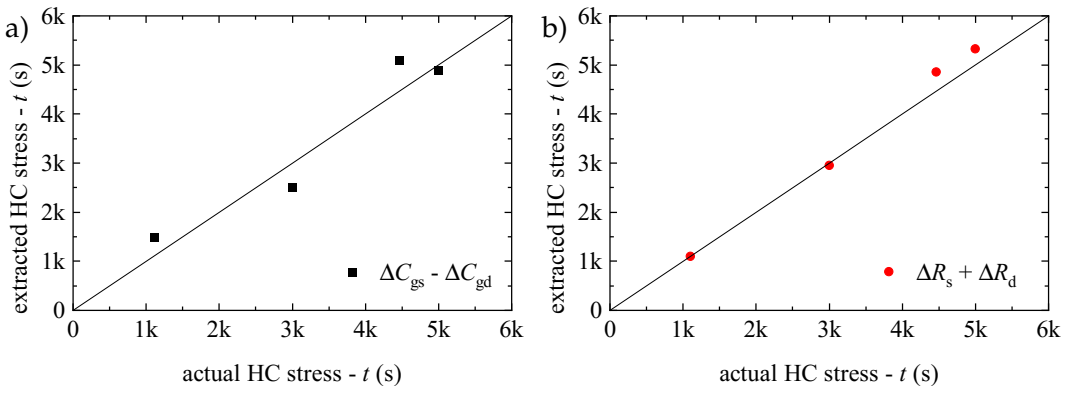


FIGURE 7.14: Comparison of actual vs. extracted HC stress duration within the mixed stress sequence shown in Fig. 7.13. The computation is performed using the empirical relation of (a) Small signal capacitances (b) series resistances. The solid line shows an ideal correlation.

# Chapter 8

# Conclusion and Recommendations

## 8.1 General Conclusions

In this dissertation, several advancements have been made in accounting reliability effects in RF small-signal domain. The work presented focuses on the MOSFETs used in RF applications. Nevertheless, the conclusion is not limited to specifically RF MOSFETs, and the obtained knowledge can be applied to MOSFET degradation mechanisms in general. Moreover, the potential of S-parameters to provide insights about device degradation is explored by developing new characterization methodologies.

Before analyzing the impact of any degradation mechanism, self-heating effects in MOSFETs having frequently used RF layouts have been studied. The work presented in this dissertation began with reliability characterization of multi-finger devices; however, soon, it was realized that different magnitudes of observed degradation depending on device layout could not be explained by the degradation mechanism itself. The temperature kinetics must be known in order to understand the degradation effects. $R_{th}$ is found to be a function of device geometric parameters such as $nf$, $w_{\mathrm{g}}$, $l_{\mathrm{g}}$, $f_{\mathrm{spac}}$. Significant thermal performance is achieved by increasing $f_{\mathrm{spac}}$, and an optimum value of $f_{\mathrm{spac}}$ = 190 nm is observed in terms of $R_{th}$ and total device footprint. An empirical model based on the equivalent thermal network as a function of device geometrical dimensions is derived. For further optimum thermal performance, the layouts with NREP (number of repetitions along gate poly line) and NRX (number of active area slices) are proposed.

For BTI characterization several devices are stressed to evaluate the impact of the recoverable and permanent component of BTI stress on DC parameters. Furthermore, the impact of BTI permanent degradation component on the small-signal performance of FDSOI MOSFETs is analyzed. Degradation in n-MOSFET due to PBTI is dominated by oxide defects, whereas p-MOSFET suffers from both interface and oxide defects. The small-signal RF parameters were majorly affected by a shift of the bias point. The correlation between DC degraded parameters and S-parameters enables the post-stress modeling of the small-signal parameters. Changes in RF parameters subjected to BTI stress should be accounted for to ensure consistent performance and impedance matching. A new S-parameter based OTF BTI characterization technique (**S**OTF-BTI) is demonstrated utilizing the S-parameters measurements at the stress level. Through S-parameters, the gain parameter was extracted and correlated with the shift of gate bias and ultimately to the shift of $V_{\mathrm{th}}$. The results are sensitive to the accuracy of the initial $g_{\mathrm{ds}}$ at $t_0$ and $\partial V_{\mathrm{gs}}/\partial g_{\mathrm{ds}}$. This technique fundamentally provides an opportunity to avoid the recovery effect during the BTI characterization. Using the **S**OTF-BTI technique, the $\Delta V_{\mathrm{th}}$ is monitored for the PBTI in n-MOSFET and NBTI in p-MOSFET resulting in a larger $\Delta V_{\mathrm{th}}$ compared to the "fast-Id" method for the longer stress times. The

n-MOSFETs are observed to be less prone to fitting error of $\partial V_{gs}/\partial g_{ds}$ as compared to p-MOSFETs. In order to improve the accuracy of the method, multiple devices should be measured to improve the precision statistically. The proposed setup integrates the reliability characterization and S-parameters which aids the reliability assessment beyond DC parameters and implies RF parameters as the potential indicator of device lifetime.

For hot-carrier degradation analysis, it is shown that the HC stress has a prominent effect on $I_d$ and $V_{th}$ degradation. From S-parameter analysis, it is established that the degradation in small-signal gain parameters is directly correlated with the DC parameters degradation. HC stress has not impacted the frequency behavior of the S-parameters. Extraction of series resistance component shows a dominant increase of $R_d$. The corresponding gain degradation effects are propagated to RF key FoMs, i.e., $f_t$ and $f_{max}$. The distribution of small-signal capacitance reveals a unique HCD degradation signature caused by the change of local flatband voltage at the drain side. $\Delta V_{th}$ corrected $C_{gg}$ before and after stress remains the same. However, $\Delta V_{th}$ corrected $C_{gs}$ and $C_{gd}$ increases and decreases after HC stress, respectively. The changes in small-signal capacitances are then qualitatively verified with the TCAD dynamic simulations. Simulated small-signal capacitances for different fixed charges and interface trapped charges match with the observed experimental trends after BTI and HC stress. It is shown that the fixed charges at the $Si/SiO_2$ mimicking PBTI stress results in the $V_{th}$ driven shift of CV characteristics. The TCAD simulation of interface traps near a drain and spacer region resembling the effect of HC stress results in an increment of gate-source capacitance and decrement of gate-source capacitance. However, the total gate capacitance when corrected for $V_{th}$ remains mainly unaffected as observed experimentally. Based on the unique signature of HCD and BTI degradation observed in small-signal capacitances a new deconvolution technique is demonstrated. The technique is validated through a mixed HC and BTI stress sequence. HCD component in a mixed stress sequence is filtered out using empirically established relations for changes in small-signal capacitances and series resistances.

Based on the experimentally observed trends of device degradation and self-heating, an essential correlation is established. The measured HCD is directly correlated with the increased temperatures caused by the self-heating. Extracted $R_{th}$ for varied geometries are used to calculate the device internal temperature during HC stress. This enables the modeling of HCD by including $R_{th}$ for the correct temperature assessment. As the temperature rises, the secondary BTI effect in HCD becomes prominent, and the $V_{th}$ shift component tends to increase compared to the $\Delta I_d$ component. This emphasizes that it is important to consider self-heating during HC stress, especially for the multi-finger RF layouts. The change of degradation mechanism based on device geometry needs to be appropriately accounted for in the lifetime calculation.

## 8.2 Recommendations for Future Work

As several conclusions and insights into the field of RF reliability are presented in the previous section, this work also put forward some new questions and outlooks for future work.

- While modeling the self-heating dependence on device geometric parameters, the total number of drain and source contacts are considered. Unavailability

of designs with a different number of contacts while fixing the other layout parameters results in the lack of information regarding the relative impact of contacts on self-heating. In the next iteration, structures with different number of contacts should be analyzed to separate the corresponding effects.

- The impact of small-signal performance analyzed under DC HC and BTI stress conditions reveals that most of the degradation can be translated back to the MOSFET's DC metric. It is, however, necessary to evaluate the same under alternating stress conditions to find out quasi-static approximation and a step forward toward scalable RF reliability models.

- During the application of **S**OTF-BTI-BTI techniques, the drain bias is always grounded to avoid any parasitic HC stress effect. An impact of a small drain bias on accuracy needs to be evaluated. Furthermore, under such small drain bias, a correlation between resultant degradation and FDSOI transistor width can be investigated for potential parasictic HC effect. Statistical analysis of data obtained through this technique should improve the accuracy of the method.

- The separation of HCD and BTI degradation in mixed-mode stress is demonstrated on a relatively simple sequence. The validation should be performed on alternating stress sequences.

- An important recommendation in terms of degradation mechanism, which is out of scope for this dissertation, is Off-state HC stress. As in analog/RF applications, the device experience almost all different modes of operation; it is necessary to quantify the impact of Off-state HC stress. This would enable a step towards a complete, scalable RF reliability model.

As there is always room for improvement, it is also required to conclude the topics with an open end and interesting outlook.

# Appendix A

# Directly measured S-parameters and extracted Y-parameters

After calibration, S-parameters are measured for several devices at different bias conditions. An example of one such measurement at a fixed bias and frequency of 1 GHz to 50 GHz is shown in figure A.1. Figures A.2 and A.3 show the median values of the real and imaginary part of all 2-port Y-parameters with respect to frequency in saturation ($|V_{ds}| = 0.8$ V) for n-MOSFET and p-MOSFET, respectively. Bias and frequency dependence can be observed for the converted Y-parameters. $Y_{12}$, which indicates reverse gain, is relatively insensitive to the gate bias, whereas $Re(Y_{21})$ shows transconductance is stable over the specified range of frequency.

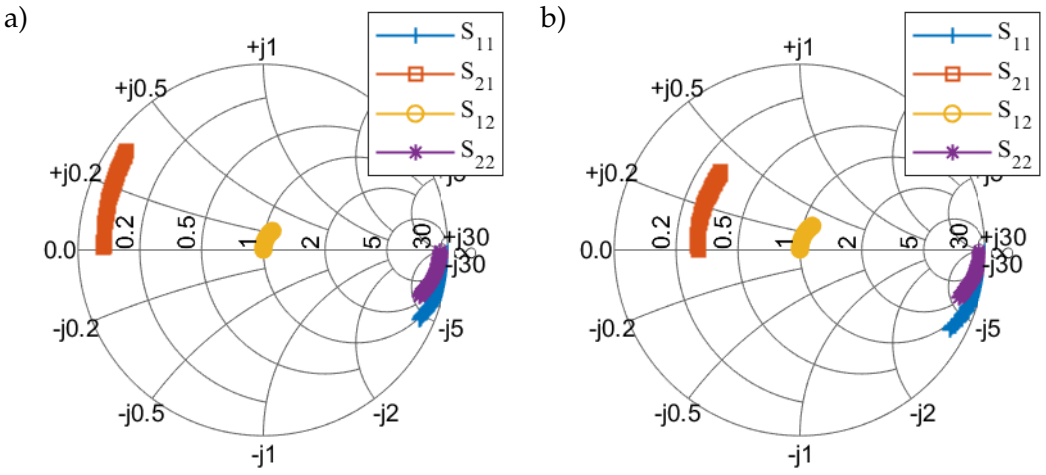


FIGURE A.1: Measured S-parameters after VNA calibration at $|V_{gs}| = 0.26$ V and $|V_{ds}| = 0.8$ V for (a) n-MOSFET and (b) p-MOSFET respectively with device dimension of $l_g = 18$ nm, $w_f = 1$ $\mu$m, and $nf = 16$.

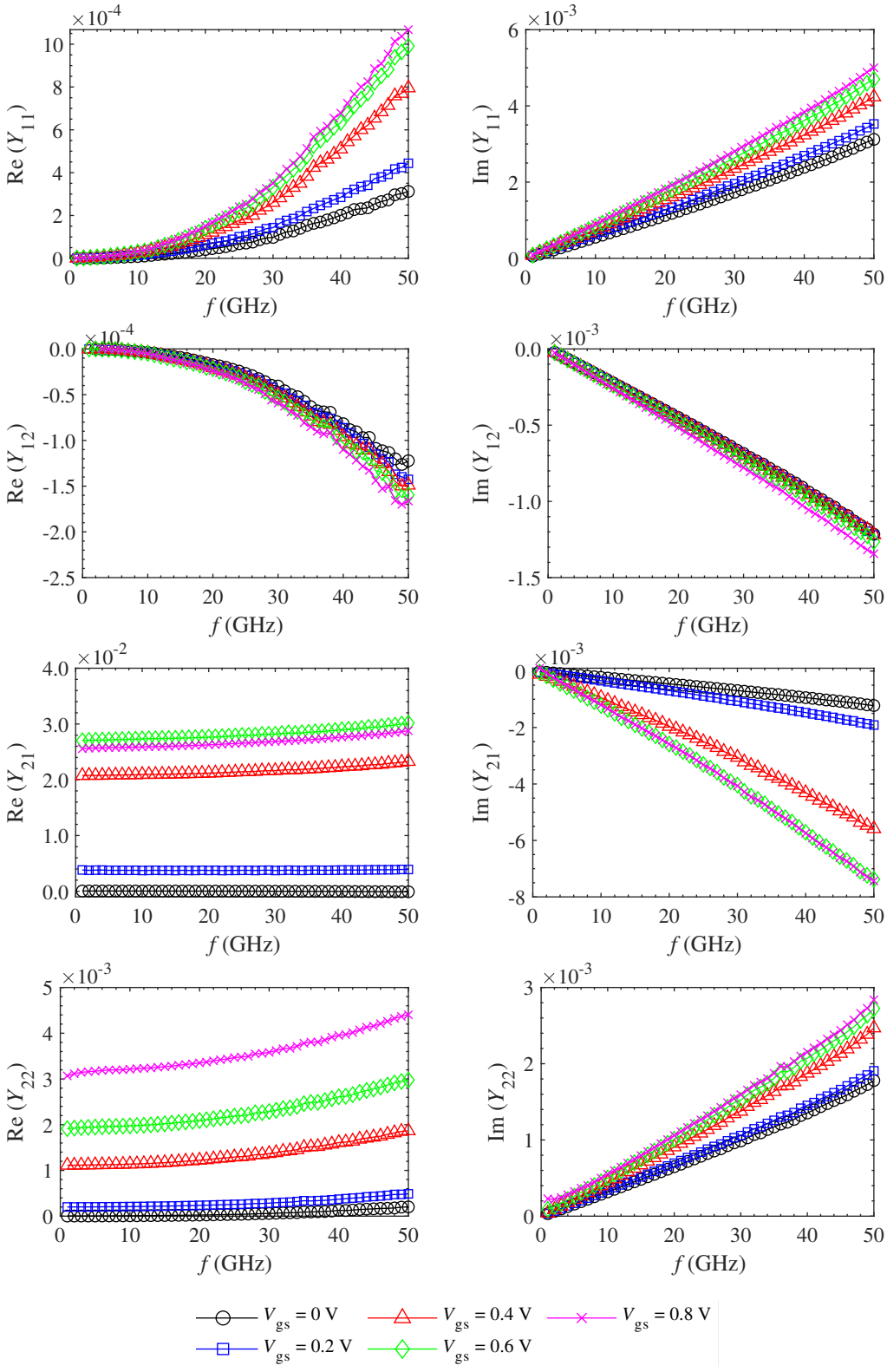


FIGURE A.2: Real and imaginary part of 2-port Y-parameters extracted from measured S-parameters of FDSOI n-MOSFET ($l_g$ = 18 nm, $w_f$ = 1 $\mu$m, and $nf$ = 16) over a range of gate bias and a fixed drain bias of $V_{ds}$ = 0.8 V.

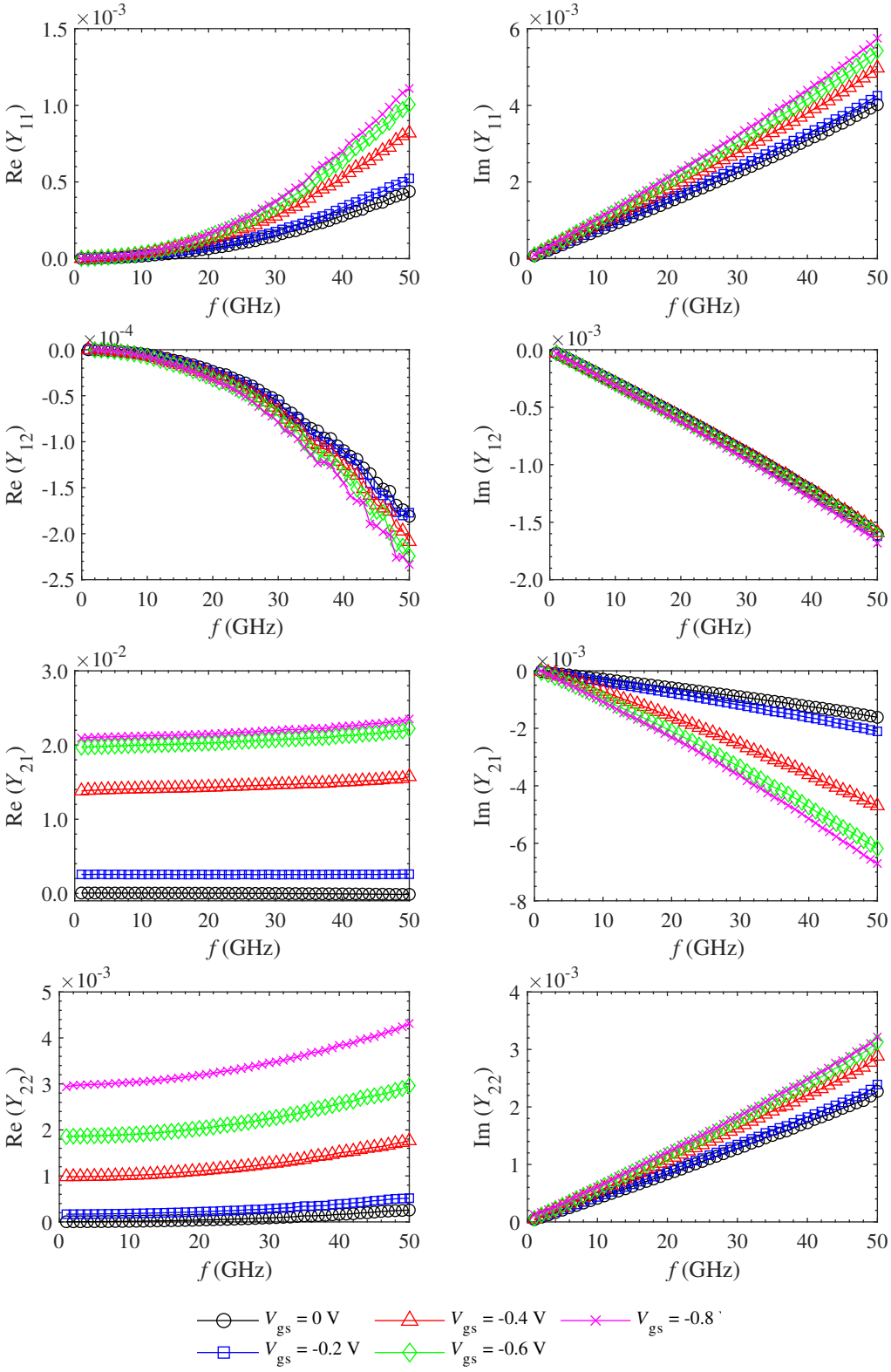


FIGURE A.3: Real and imaginary part of 2-port Y-parameters extracted from measured S-parameters of FDSOI p-MOSFET ($l_g$ = 18 nm, $w_f$ = 1 $\mu$m, and $nf$ = 16)over a range of gate bias and a fixed drain bias of $V_{ds}$ = -0.8 V.

# Appendix B

# Device Dimensions for Thermal Resistance Modeling

TABLE B.1: Device geometrical dimensions used for the modeling of thermal resistance ($R_{th}$).

| $l_g$ (nm) | $w_f$ (µm) | $nf$ | $f_{spac}$ (nm) |
|---|---|---|---|
| 18 | 0.3 | 16 | 86 |
| 18 | 0.5 | 16 | 86 |
| 18 | 1 | 16 | 86 |
| 18 | 5 | 16 | 86 |
| 18 | 0.5 | 1 | 86 |
| 18 | 0.5 | 8 | 86 |
| 18 | 0.5 | 16 | 86 |
| 18 | 0.5 | 32 | 86 |
| 18 | 0.5 | 64 | 86 |
| 18 | 0.5 | 128 | 86 |
| 18 | 0.5 | 32 | 86 |
| 24 | 0.5 | 32 | 80 |
| 28 | 0.5 | 32 | 76 |
| 40 | 0.5 | 32 | 90 |
| 60 | 0.5 | 32 | 110 |
| 100 | 0.5 | 32 | 110 |
| 18 | 0.5 | 16 | 86 |
| 18 | 0.5 | 16 | 190 |
| 18 | 0.5 | 16 | 294 |

# Appendix C

# Frequency response of HCD

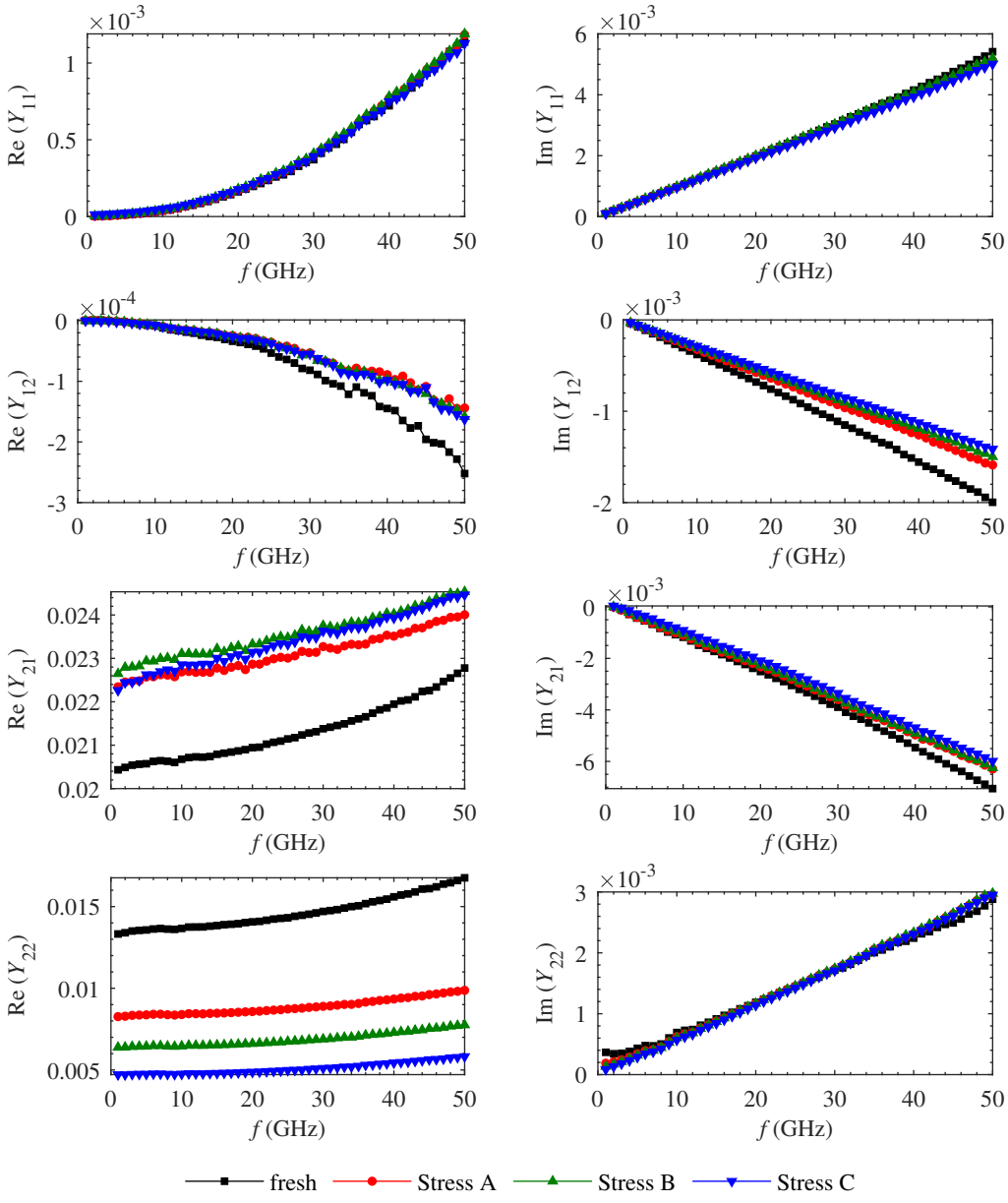


FIGURE C.1: Frequency behavior of real and imaginary part of 2-port Y-parameters of FDSOI n-MOSFET ($l_g$ = 18 nm, $w_f$ = 1 $\mu$m, and $nf$ = 16) at bias condition of $V_{gs}$ = 0.8 V, $V_{ds}$ = 0.8 V for fresh and HC stressed devices under different stress voltages.

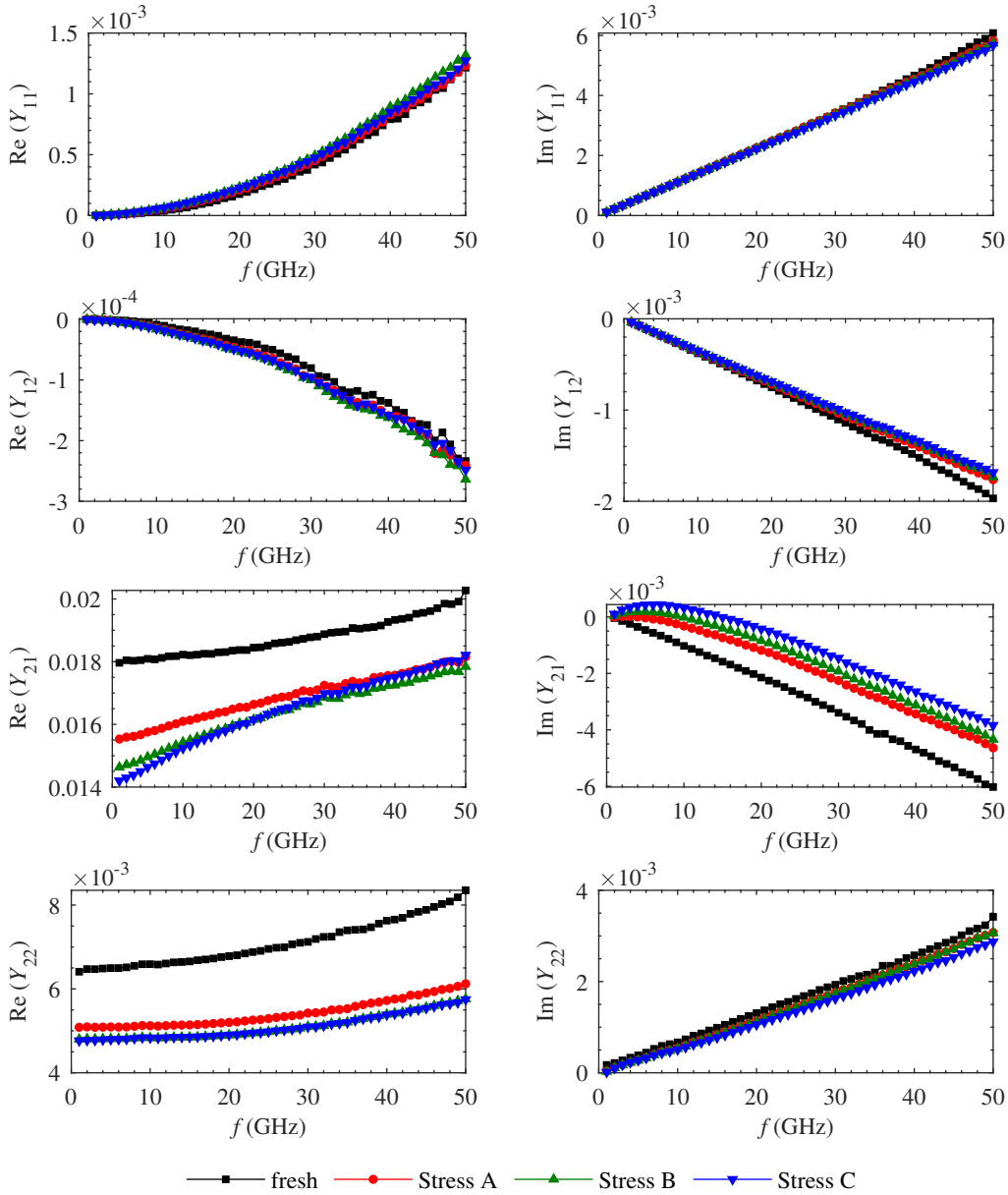


FIGURE C.2: Frequency behavior of real and imaginary part of 2-port Y-parameters of FDSOI p-MOSFET ($l_g$ = 18 nm, $w_f$ = 1 $\mu$m, and $nf$ = 16) at bias condition of $V_{gs}$ = -0.8 V, $V_{ds}$ = -0.8 V for fresh and HC stressed devices under different stress voltages.

# Appendix D

# Localization Effect of Interface Traps

**Interface Traps near Gate**

Interface traps are introduced at the gate oxide and SOI interface within the cross-section of 2 nm near the drain side, as shown in Fig. D.1. Compared to the larger cross-section of interface traps, as shown in Fig. 7.3, the resulting capacitance changes (Fig. D.2) are greatly reduced.

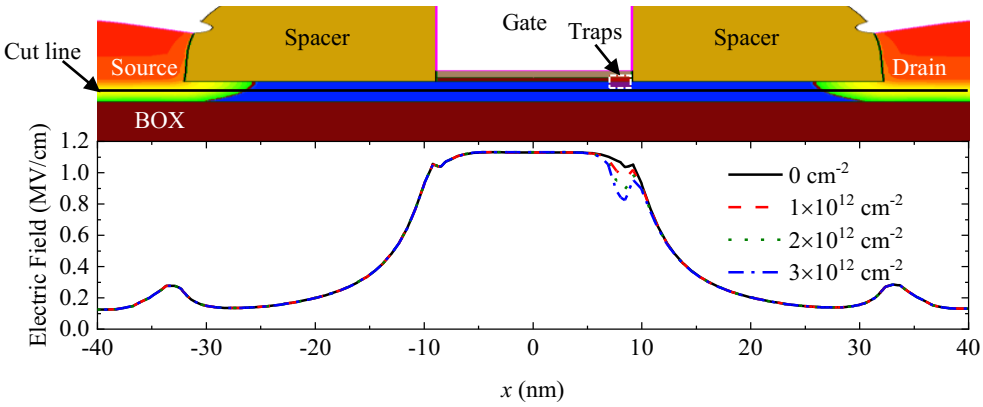


FIGURE D.1: Electrical field profile at the cut line for the interface traps introduced at the gate oxide and SOI interface within the cross-section of 2 nm.

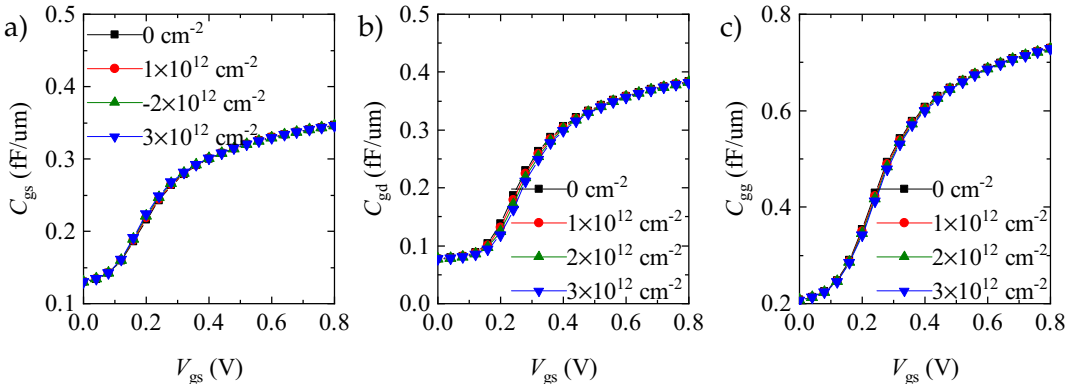


FIGURE D.2: Simulated (a) $C_{gs}$, (b) $C_{gd}$, and (c) $C_{gg}$ for an n-MOSFET plotted vs. $V_{gs}$ for different concentrations of ITC at the interface of the gate oxide and SOI, shown in Fig. D.1. The capacitances are extracted at $f$ = 20 GHz and $V_{ds}$ = 0.05 V.

**Interface Traps near Spacer Region**

Interface traps introduced at the interface of spacer and SOI within the cross-section of 10 nm at the end of gate and channel overlap as shown in Fig. D.3. The resulting changes in the small-signal capacitance (Fig. D.4) show a significant increase of $C_{gs}$ and decrement of $C_{gd}$/. For the trap concentration of $5 \times 10^{12}$ cm$^{-2}$, almost all the $C_{gg}$ capacitance contribution is from $C_{gs}$. $C_{gd}$ is reduced to almost overlap capacitance. Shifting the location of such interface traps with similar cross-section towards the drain region (Fig. D.5) results in a similar but stronger capacitance shift trend as shown in Fig. D.6. For the trap concentration of $5 \times 10^{12}$ cm$^{-2}$, $C_{gd}$ tends to degrade even below miller capacitance value to extreme shift in local electrostatic potential at the drain side.

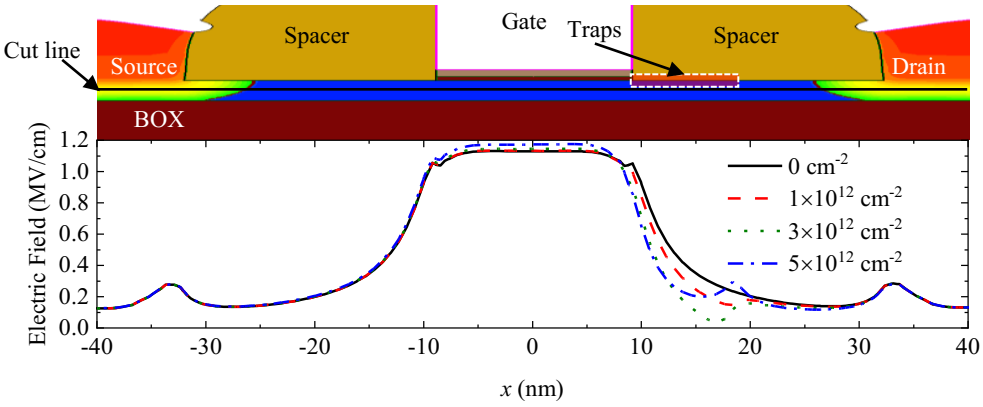


FIGURE D.3: Electrical field profile at the cut line for the interface traps placed at the interface of spacer and SOI within the cross-section of 10 nm

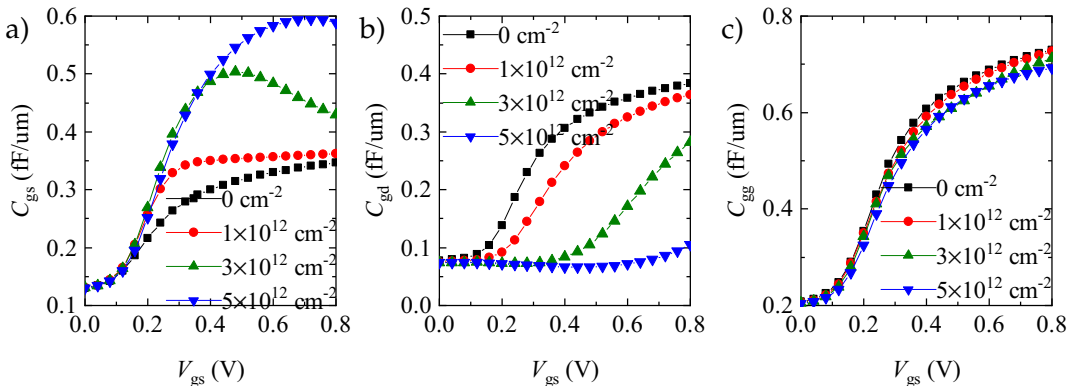


FIGURE D.4: (a) $C_{gs}$, (b) $C_{gd}$, and (c) $C_{gg}$ vs. $V_{gs}$ for an n-MOSFET with different concentrations of ITC at the interface of spacer and SOI as shown in Fig. D.3. The capacitances are obtained from the TCAD simulation at $f$ = 20 GHz and $V_{ds}$ = 0.05 V.

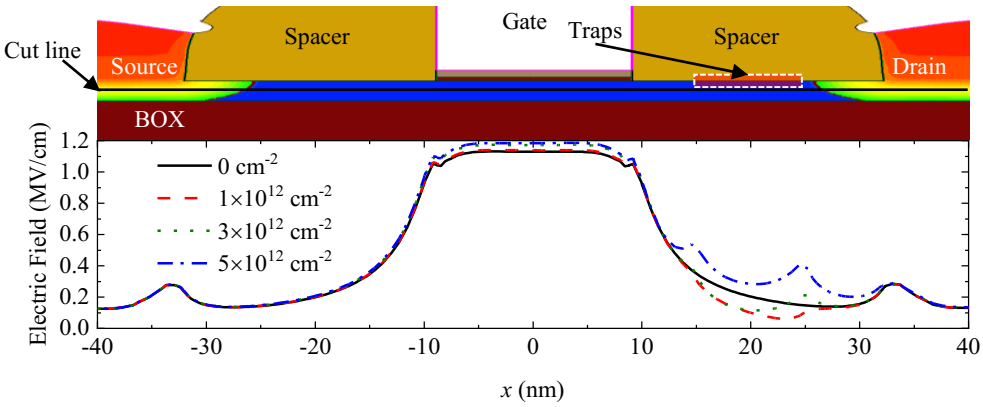


FIGURE D.5: Electrical field profile at the cut line for the interface traps placed at the interface of spacer and SOI within the cross-section of 10 nm closest to the drain region.

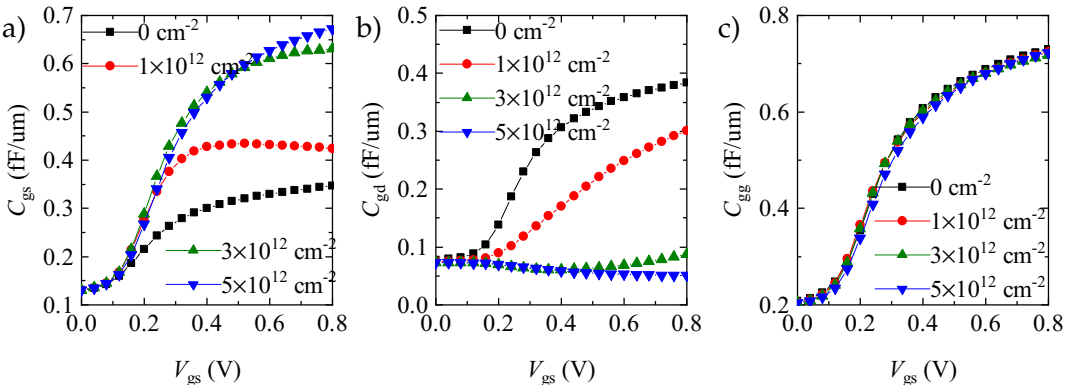


FIGURE D.6: (a) $C_{gs}$, (b) $C_{gd}$, and (c) $C_{gg}$ vs. $V_{gs}$ for an n-MOSFET with different concentrations of ITC at the interface of spacer and SOI as shown in Fig. D.5. The capacitances are obtained from the TCAD simulation at $f$ = 20 GHz and $V_{ds}$ = 0.05 V

# Bibliography


[1] R. Carter, J. Mazurier, L. Pirro, *et al.*, "22nm FDSOI technology for emerging mobile, Internet-of-Things, and RF applications," in *2016 IEEE International Electron Devices Meeting (IEDM)*, IEEE, 2016, pp. 2–2.

[2] S. Ong, S. Lehmann, W. Chow, *et al.*, "A 22nm FDSOI Technology Optimized for RF/mmWave Applications," in *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Jun. 2018, pp. 72–75. DOI: 10.1109/RFIC.2018.8429035.

[3] S. N. Ong, L. H. K. Chan, K. W. J. Chew, *et al.*, "22nm FD-SOI Technology with Back-biasing Capability Offers Excellent Performance for Enabling Efficient, Ultra-low Power Analog and RF/Millimeter-Wave Designs," in *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Jun. 2019, pp. 323–326. DOI: 10.1109/RFIC.2019.8701768.

[4] M. Wiatr and S. Kolodinski, "22FDX™ Technology and Add-on-Functionalities," in *ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC)*, Sep. 2019, pp. 70–73. DOI: 10.1109/ESSDERC.2019.8901819.

[5] J. Bardeen and W. H. Brattain, "The transistor, a semi-conductor triode," *Physical Review*, vol. 74, no. 2, p. 230, 1948.

[6] W. Shockley, "The theory of p-n junctions in semiconductors and p-n junction transistors," *The Bell System Technical Journal*, vol. 28, no. 3, pp. 435–489, Jul. 1949, ISSN: 0005-8580. DOI: 10.1002/j.1538-7305.1949.tb03645.x.

[7] L. J. Edgar, "Device for controlling electric current," pat., US Patent 1,900,018, Mar. 7, 1933.

[8] M. M. Atalla, E. Tannenbaum, and E. J. Scheibner, "Stabilization of silicon surfaces by thermally grown oxides," *Bell System Technical Journal*, vol. 38, no. 3, pp. 749–783, 1959.

[9] R. G. Arns, "The other transistor: Early history of the metal-oxide semiconductor field-effect transistor," *Engineering Science and Education Journal*, vol. 7, no. 5, pp. 233–240, Oct. 1998, ISSN: 0963-7346. DOI: 10.1049/esej:19980509.

[10] R. Bassett, "New technology, new people, new organizations: The rise of the MOS transistor, 1945-1975," *Business and Economic History*, pp. 1–7, 1998.

[11] G. E. Moore, "Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp.114 ff.," *IEEE Solid-State Circuits Society Newsletter*, vol. 11, no. 3, pp. 33–35, Sep. 2006, ISSN: 1098-4232. DOI: 10.1109/N-SSC.2006.4785860.

[12] G. E. Moore, "Progress in digital integrated electronics," in *Electron Devices Meeting*, vol. 21, 1975, pp. 11–13.

[13] M. M. Waldrop, "The chips are down for Moore's law," *Nature News*, vol. 530, no. 7589, p. 144, 2016.

[14] S. Greengard, "Can nanosheet transistors keep Moore's law alive?" *Communications of the ACM*, vol. 63, no. 3, pp. 10–12, Feb. 24, 2020, ISSN: 0001-0782, 1557-7317. DOI: 10 . 1145 / 3379493. [Online]. Available: https://dl.acm.org/doi/10.1145/3379493 (visited on 11/26/2020).

[15] N. Bloom, C. I. Jones, J. Van Reenen, and M. Webb, "Are ideas getting harder to find?" *American Economic Review*, vol. 110, no. 4, pp. 1104–44, 2020.

[16] C. E. Leiserson, N. C. Thompson, J. S. Emer, *et al.*, "There's plenty of room at the Top: What will drive computer performance after Moore's law?" *Science*, vol. 368, no. 6495, 2020.

[17] J. Shalf, "The future of computing beyond Moore's law," *Philosophical Transactions of the Royal Society A*, vol. 378, no. 2166, p. 20 190 061, 2020.

[18] F. D'Agostino and D. Quercia, "Short-channel effects in MOSFETs," *Introduction to VLSI design (EECS 467)*, vol. 70, pp. 71–72, 2000.

[19] S.-H. Oh, D. Monroe, and J. M. Hergenrother, "Analytic description of short-channel effects in fully-depleted double-gate and cylindrical, surrounding-gate MOSFETs," *IEEE electron device letters*, vol. 21, no. 9, pp. 445–447, 2000.

[20] S. Veeraraghavan and J. G. Fossum, "Short-channel effects in SOI MOSFETs," *IEEE Transactions on Electron Devices*, vol. 36, no. 3, pp. 522–528, 1989.

[21] Q. Xie, C.-J. Lee, J. Xu, C. Wann, J. Y.-C. Sun, and Y. Taur, "Comprehensive analysis of short-channel effects in ultrathin SOI MOSFETs," *IEEE Transactions on Electron Devices*, vol. 60, no. 6, pp. 1814–1819, 2013.

[22] A. Chaudhry and M. J. Kumar, "Controlling short-channel effects in deep-submicron SOI MOSFETs for improved reliability: A review," *IEEE Transactions on Device and Materials Reliability*, vol. 4, no. 1, pp. 99–109, 2004.

[23] A. B. Kaul, *Microelectronics to Nanoelectronics: Materials, Devices & Manufacturability*. CRC Press, Dec. 19, 2017, 467 pp., ISBN: 978-1-351-83238-0. Google Books: 2AhEDwAAQBAJ.

[24] E. Amat, T. Kauerauf, R. Degraeve, *et al.*, "Channel hot-carrier degradation in short-channel transistors with high-$ k $/metal gate stacks," *IEEE Transactions on Device and Materials reliability*, vol. 9, no. 3, pp. 425–430, 2009.

[25] C. Auth, A. Cappellani, J.-S. Chun, *et al.*, "45nm high-k+ metal gate strain-enhanced transistors," in *2008 Symposium on VLSI Technology*, IEEE, 2008, pp. 128–129.

[26] J. Kavalieros, B. Doyle, S. Datta, *et al.*, "Tri-gate transistor architecture with high-k gate dielectrics, metal gates and strain engineering," in *2006 Symposium on VLSI Technology, 2006. Digest of Technical Papers.*, IEEE, 2006, pp. 50–51.

[27] M. Chu, Y. Sun, U. Aghoram, and S. E. Thompson, "Strain: A solution for higher carrier mobility in nanoscale MOSFETs," *Annual Review of Materials Research*, vol. 39, pp. 203–229, 2009.

[28] N. Xu, B. Ho, F. Andrieu, *et al.*, "Carrier-mobility enhancement via strain engineering in future thin-body MOSFETs," *IEEE electron device letters*, vol. 33, no. 3, pp. 318–320, 2012.

[29] J.-P. Raskin, A. Viviani, D. Flandre, and J.-P. Colinge, "Substrate crosstalk reduction using SOI technology," *IEEE Transactions on Electron Devices*, vol. 44, no. 12, pp. 2252–2261, 1997.

[30] G. G. Shahidi, "SOI technology for the GHz era," *IBM journal of Research and Development*, vol. 46, no. 2.3, pp. 121–131, 2002.

[31] J.-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*. Springer Science & Business Media, 1997.

[32] O. Kononchuk and B.-Y. Nguyen, *Silicon-on-Insulator (Soi) Technology: Manufacture and Applications*. Elsevier, 2014.

[33] B. Yu, C. H. Wann, E. D. Nowak, K. Noda, and C. Hu, "Short-channel effect improved by lateral channel-engineering in deep-submicronmeter MOSFET's," *IEEE Transactions on Electron Devices*, vol. 44, no. 4, pp. 627–634, 1997.

[34] J. Kedzierski, M. Ieong, E. Nowak, *et al.*, "Extension and source/drain design for high-performance FinFET devices," *IEEE Transactions on Electron Devices*, vol. 50, no. 4, pp. 952–958, 2003.

[35] A. A. Orouji and M. J. Kumar, "Nanoscale SOI MOSFETs with electrically induced source/drain extension: Novel attributes and design considerations for suppressed short-channel effects," *Superlattices and Microstructures*, vol. 39, no. 5, pp. 395–405, 2006.

[36] H. Shang, M. M. Frank, E. P. Gusev, *et al.*, "Germanium channel MOSFETs: Opportunities and challenges," *IBM Journal of Research and Development*, vol. 50, no. 4.5, pp. 377–386, 2006.

[37] S. Oktyabrsky and D. Y. Peide, *Fundamentals of III-V Semiconductor MOSFETs*. Springer, 2010.

[38] H. Liu, A. T. Neal, and P. D. Ye, "Channel length scaling of MoS2 MOSFETs," *ACS nano*, vol. 6, no. 10, pp. 8563–8569, 2012.

[39] A. Nourbakhsh, A. Zubair, R. N. Sajjad, *et al.*, "MoS2 field-effect transistor with sub-10 nm channel length," *Nano letters*, vol. 16, no. 12, pp. 7798–7806, 2016.

[40] J.-P. Colinge, *FinFETs and Other Multi-Gate Transistors*. Springer, 2008, vol. 73.

[41] M. Lebby, V. Sabnis, and P. B. Atanackovic, "Multilayered box in FDSOI MOSFETS," pat., US Patent 7,821,066, Oct. 26, 2010.

[42] J.-P. Noel, O. Thomas, M.-A. Jaud, *et al.*, "Multi-$ V_ ${$T$}$ $ UTBB FDSOI device architectures for low-power CMOS circuit," *IEEE Transactions on Electron Devices*, vol. 58, no. 8, pp. 2473–2482, 2011.

[43] N. Planes, O. Weber, V. Barral, *et al.*, "28nm FDSOI technology platform for high-speed low-voltage digital applications," in *2012 Symposium on VLSI Technology (VLSIT)*, IEEE, 2012, pp. 133–134.

[44] T. Ohtou, N. Sugii, and T. Hiramoto, "Impact of parameter variations and random dopant fluctuations on short-channel fully depleted SOI MOSFETs with extremely thin BOX," *IEEE electron device letters*, vol. 28, no. 8, pp. 740–742, 2007.

[45] A. Asenov, "Simulation of statistical variability in nano MOSFETs," in *2007 IEEE Symposium on VLSI Technology*, IEEE, 2007, pp. 86–87.

[46] K. Kuhn, C. Kenyon, A. Kornfeld, *et al.*, "Managing Process Variation in Intel's 45nm CMOS Technology.," *Intel Technology Journal*, vol. 12, no. 2, 2008.

[47] N. Sugii, R. Tsuchiya, T. Ishigaki, Y. Morita, H. Yoshimoto, and S. Kimura, "Local Vth Variability and Scalability in Silicon-on-Thin-BOX (SOTB) CMOS With Small Random-Dopant Fluctuation," *IEEE Transactions on Electron Devices*, vol. 57, no. 4, pp. 835–845, Apr. 2010, ISSN: 1557-9646. DOI: 10.1109/TED.2010.2040664.

[48] H. Mahmoodi, S. Mukhopadhyay, and K. Roy, "Estimation of delay variations due to random-dopant fluctuations in nanoscale CMOS circuits," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 9, pp. 1787–1796, Sep. 2005, ISSN: 1558-173X. DOI: 10.1109/JSSC.2005.852164.

[49] S. Wang, G. Leung, A. Pan, C. O. Chui, and P. Gupta, "Evaluation of digital circuit-level variability in inversion-mode and junctionless FinFET technologies," *IEEE transactions on electron devices*, vol. 60, no. 7, pp. 2186–2193, 2013.

[50] Y. Ye, S. Gummalla, C.-C. Wang, C. Chakrabarti, and Y. Cao, "Random variability modeling and its impact on scaled CMOS circuits," *Journal of computational electronics*, vol. 9, no. 3-4, pp. 108–113, 2010.

[51] K. Bernstein and N. J. Rohrer, *SOI Circuit Design Concepts*. Springer Science & Business Media, 2007.

[52] C.-H. Dai, T.-C. Chang, A.-K. Chu, *et al.*, "On the origin of gate-induced floating-body effect in PD SOI p-MOSFETs," *IEEE electron device letters*, vol. 32, no. 7, pp. 847–849, 2011.

[53] J. G. Fossum, M. M. Pelella, and S. Krishnan, "Scalable PD/SOI CMOS with floating bodies," *IEEE Electron Device Letters*, vol. 19, no. 11, pp. 414–416, 1998.

[54] R. V. Joshi, S. Mukhopadhyay, D. W. Plass, Y. H. Chan, C.-T. Chuang, and A. Devgan, "Variability analysis for sub-100 nm PD/SOI CMOS SRAM cell," in *Proceedings of the 30th European Solid-State Circuits Conference*, IEEE, 2004, pp. 211–214.

[55] B. Vandana, "Study of floating body effect in SOI technology," *Int. J. Mod. Eng. Res*, vol. 3, no. 3, pp. 1817–1824, 2013.

[56] J.-P. Colinge, "Thin-film SOI technology: The solution to many submicron CMOS problems," in *International Technical Digest on Electron Devices Meeting*, IEEE, 1989, pp. 817–820.

[57] B. Doris, M. Ieong, T. Kanarsky, *et al.*, "Extreme scaling with ultra-thin Si channel MOSFETs," in *Digest. International Electron Devices Meeting,*, IEEE, 2002, pp. 267–270.

[58] L. T. Su, J. B. Jacobs, J. E. Chung, and D. A. Antoniadis, "Deep-submicrometer channel design in silicon-on-insulator (SOI) MOSFET's," *IEEE Electron Device Letters*, vol. 15, no. 9, pp. 366–369, 1994.

[59] E. Suzuki, K. Ishii, S. Kanemaru, *et al.*, "Highly suppressed short-channel effects in ultrathin SOI n-MOSFETs," *IEEE Transactions on Electron Devices*, vol. 47, no. 2, pp. 354–359, 2000.

[60] V. P. Trivedi and J. G. Fossum, "Nanoscale FD/SOI CMOS: Thick or thin box?" *IEEE electron device letters*, vol. 26, no. 1, pp. 26–28, 2004.

[61] R. Tsuchiya, M. Horiuchi, S. Kimura, *et al.*, "Silicon on thin BOX: A new paradigm of the CMOSFET for low-power high-performance application featuring wide-range back-bias control," in *IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004.*, IEEE, 2004, pp. 631–634.

[62] J. P. Colinge, H. K. Hu, and S. Peng, "Fabrication of thin silicon-on-insulator flims using laser recrystallisation," *Electronics Letters*, vol. 21, no. 23, pp. 1102–1103, Nov. 1985, ISSN: 0013-5194. DOI: 10.1049/el:19850782.

[63] J. Colinge, "Subthreshold slope of thin-film SOI MOSFET's," *IEEE Electron Device Letters*, vol. 7, no. 4, pp. 244–246, Apr. 1986, ISSN: 1558-0563. DOI: 10.1109/EDL.1986.26359.

[64] H. Matsuhashi, "FD-SOI Device and Process Technologies," in *Fully-Depleted SOI CMOS Circuits and Technology: For Ultralow-Power Applications*, T. Sakurai, A. Matsuzawa, and T. Douseki, Eds., Boston, MA: Springer US, 2006, pp. 23–81, ISBN: 978-0-387-29218-2. DOI: 10.1007/978-0-387-29218-2_2. [Online]. Available: https://doi.org/10.1007/978-0-387-29218-2_2 (visited on 11/30/2020).

[65] J.-P. Noel, O. Thomas, M.-A. Jaud, *et al.*, "Multi-Vt UTBB FDSOI device architectures for low-power CMOS circuit," *IEEE Transactions on Electron Devices*, vol. 58, no. 8, pp. 2473–2482, 2011.

[66] L. Nyssens, A. Halder, B. K. Esfeh, *et al.*, "Self-Heating in FDSOI UTBB MOSFETs at Cryogenic Temperatures and its Effect on Analog Figures of Merit," *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 789–796, 2020, ISSN: 2168-6734. DOI: 10.1109/JEDS.2020.2999632.

[67] C. Schwan, K. W. Chew, T. Feudel, *et al.*, "Low Power FDSOI Technology and Devices for RF Applications," *ECS Transactions*, vol. 75, no. 8, p. 21, Aug. 18, 2016, ISSN: 1938-5862. DOI: 10.1149/07508.0021ecst. [Online]. Available: https://iopscience.iop.org/article/10.1149/07508.0021ecst/meta (visited on 11/30/2020).

[68] J. Noel, O. Thomas, M. Jaud, *et al.*, "UT2B-FDSOI device architecture dedicated to low power design techniques," in *2010 Proceedings of the European Solid State Device Research Conference*, Sep. 2010, pp. 210–213. DOI: 10.1109/ESSDERC.2010.5618389.

[69] F. Andrieu, O. Weber, J. Mazurier, *et al.*, "Low leakage and low variability Ultra-Thin Body and Buried Oxide (UT2B) SOI technology for 20nm low power CMOS and beyond," in *2010 Symposium on VLSI Technology*, Jun. 2010, pp. 57–58. DOI: 10.1109/VLSIT.2010.5556122.

[70] S. Burignat, M. K. M. Arshad, J. Raskin, *et al.*, "Drain / substrate coupling impact on DIBL of Ultra Thin Body and BOX SOI MOSFETs with undoped channel," in *2009 Proceedings of the European Solid State Device Research Conference*, Sep. 2009, pp. 141–144. DOI: 10.1109/ESSDERC.2009.5331323.

[71] S. Burignat, D. Flandre, M. K. Md Arshad, *et al.*, "Substrate impact on threshold voltage and subthreshold slope of sub-32nm ultra thin SOI MOSFETs with thin buried oxide and undoped channel," *Solid-State Electronics*, Selected Full-Length Extended Papers from the EUROSOI 2009 Conference, vol. 54, no. 2, pp. 213–219, Feb. 1, 2010, ISSN: 0038-1101. DOI: 10.1016/j.sse.2009.12.021. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0038110109003645 (visited on 11/30/2020).

[72] C. Fenouillet-Beranger, P. Perreau, S. Denorme, *et al.*, "Impact of a 10nm Ultra-Thin BOX (UTBOX) and Ground Plane on FDSOI devices for 32nm node and below," in *2009 Proceedings of the European Solid State Device Research Conference*, Sep. 2009, pp. 89–92. DOI: 10.1109/ESSDERC.2009.5331588.

[73] C. Fenouillet-Beranger, P. Perreau, L. Tosti, *et al.*, "Low power UTBOX and back plane (BP) FDSOI technology for 32nm node and below," in *2011 IEEE International Conference on IC Design & Technology*, IEEE, 2011, pp. 1–4.

[74] W. Schwarzenbach, X. Cauchy, O. Bonnin, *et al.*, "Ultra Thin silicon substrate for next generation technology nodes," in *2010 International Symposium on Semiconductor Manufacturing (ISSM)*, Oct. 2010, pp. 1–3.

[75] C. Maleville, "Extending planar device roadmap beyond node 20nm through ultra thin body technology," in *Proceedings of 2011 International Symposium on VLSI Technology, Systems and Applications*, Apr. 2011, pp. 1–4. DOI: 10.1109/VTSA.2011.5872261.

[76] K. Cheng, A. Khakifirooz, P. Kulkarni, *et al.*, "Extremely thin SOI (ETSOI) CMOS with record low variability for low power system-on-chip applications," in *2009 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2009, pp. 1–4. DOI: 10.1109/IEDM.2009.5424422.

[77] A. Khakifirooz, K. Cheng, P. Kulkarni, *et al.*, "Challenges and opportunities of extremely thin SOI (ETSOI) CMOS technology for future low power and general purpose system-on-chip applications," in *System and Application Proceedings of 2010 International Symposium on VLSI Technology*, Apr. 2010, pp. 110–111. DOI: 10.1109/VTSA.2010.5488928.

[78] N. Rodriguez, F. Andrieu, C. Navarro, O. Faynot, F. Gamiz, and S. Cristoloveanu, "Properties of 22nm node extremely-thin-SOI MOSFETs," in *IEEE 2011 International SOI Conference*, Oct. 2011, pp. 1–2. DOI: 10.1109/SOI.2011.6081681.

[79] T. Ishigaki, R. Tsuchiya, Y. Morita, *et al.*, "Silicon on thin BOX (SOTB) CMOS for ultralow standby power with forward-biasing performance booster," *Solid-State Electronics*, Papers Selected from the 38th European Solid-State Device Research Conference – ESSDERC'08, vol. 53, no. 7, pp. 717–722, Jul. 1, 2009, ISSN: 0038-1101. DOI: 10.1016/j.sse.2009.02.008. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0038110109000756 (visited on 11/30/2020).

[80] L. Nyssens, A. Halder, B. K. Esfeh, *et al.*, "28-nm FD-SOI CMOS RF Figures of Merit Down to 4.2 K," *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 646–654, 2020, ISSN: 2168-6734. DOI: 10.1109/JEDS.2020.3002201.

[81] O. El-Aassar and G. M. Rebeiz, "Design of Low-Power Sub-2.4 dB Mean NF 5G LNAs Using Forward Body Bias in 22 nm FDSOI," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 10, pp. 4445–4454, Oct. 2020, ISSN: 1557-9670. DOI: 10.1109/TMTT.2020.3012538.

[82] Z. Zhao, S. Lehmann, L. Lucci, *et al.*, "22FDX® fMAX Optimization through Parasitics Reduction and GM Boost," in *ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC)*, Sep. 2019, pp. 166–169. DOI: 10.1109/ESSDERC.2019.8901693.

[83] E. T. Breyer, H. Mulaosmanovic, T. Mikolajick, and S. Slesazeck, "Reconfigurable NAND/NOR logic gates in 28 nm HKMG and 22 nm FD-SOI FeFET technology," in *2017 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2017, pp. 28.5.1–28.5.4. DOI: 10.1109/IEDM.2017.8268471.

[84] T. Herrmann, A. Zaka, N. K. Subramani, Z. Zhao, S. Lehmann, and Y. Andee, "RF performance improvement on 22FDX® platform and beyond," in *2019 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, Sep. 2019, pp. 1–4. DOI: 10.1109/SISPAD.2019.8870435.

[85] C. Mazuré, R. Ferrant, B. Nguyen, W. Schwarzenbach, and C. Moulin, "FDSOI: From substrate to devices and circuit applications," in *2010 Proceedings of ESSCIRC*, Sep. 2010, pp. 45–51. DOI: 10.1109/ESSCIRC.2010.5619767.

[86] T. Skotnicki, "Heading for decananometer CMOS - Is navigation among icebergs still a viable strategy?" In *30th European Solid-State Device Research Conference*, Sep. 2000, pp. 19–33. DOI: 10.1109/ESSDERC.2000.194714.

[87] Z. Lu, N. Collaert, M. Aoulaiche, *et al.*, "Realizing super-steep subthreshold slope with conventional FDSOI CMOS at low-bias voltages," in *2010 International Electron Devices Meeting*, Dec. 2010, pp. 16.6.1–16.6.3. DOI: 10.1109/IEDM.2010.5703377.

[88] A. Khakifirooz, K. Cheng, Q. Liu, *et al.*, "Extremely thin SOI for system-on-chip applications," in *Proceedings of the IEEE 2012 Custom Integrated Circuits Conference*, Sep. 2012, pp. 1–4. DOI: 10.1109/CICC.2012.6330618.

[89] E. Beigne, A. Valentian, B. Giraud, *et al.*, "Ultra-Wide Voltage Range designs in Fully-Depleted Silicon-On-Insulator FETs," in *2013 Design, Automation Test in Europe Conference Exhibition (DATE)*, Mar. 2013, pp. 613–618. DOI: 10.7873/DATE.2013.135.

[90] J. Colinge, "Recent advances in SOI technology," in *Proceedings of 1994 IEEE International Electron Devices Meeting*, Dec. 1994, pp. 817–820. DOI: 10.1109/IEDM.1994.383299.

[91] G. J. Hu, "A better understanding of CMOS latch-up," *IEEE Transactions on Electron Devices*, vol. 31, no. 1, pp. 62–67, Jan. 1984, ISSN: 1557-9646. DOI: 10.1109/T-ED.1984.21474.

[92] T. B. Hook, "Fully depleted devices for designers: FDSOI and FinFETs," in *Proceedings of the IEEE 2012 Custom Integrated Circuits Conference*, Sep. 2012, pp. 1–7. DOI: 10.1109/CICC.2012.6330653.

[93] O. Weber, O. Faynot, F. Andrieu, *et al.*, "High immunity to threshold voltage variability in undoped ultra-thin FDSOI MOSFETs and its physical understanding," in *2008 IEEE International Electron Devices Meeting*, Dec. 2008, pp. 1–4. DOI: 10.1109/IEDM.2008.4796663.

[94] J. Cai, Z. Ren, A. Majumdar, *et al.*, "Will SOI have a life for the low-power market?" In *2008 IEEE International SOI Conference*, Oct. 2008, pp. 15–16. DOI: 10.1109/SOI.2008.4656272.

[95] S. Makovejev, V. Kilchytska, M. M. Arshad, *et al.*, "Self-heating and substrate effects in ultra-thin body ultra-thin BOX devices," in *Ulis 2011 Ultimate Integration on Silicon*, IEEE, 2011, pp. 1–4.

[96] T. Lehndorff, U. Abelein, A. Alsioufy, *et al.*, "Extended lifetime qualification concepts for automotive semiconductor components," *Universität der Bundeswehr München*, 2020.

[97] A. Alsioufy, A. Hirler, T. Lehndorff, *et al.*, "Technology Black Box: A Pioneering Tool for Semiconductor Technology Development in the Automotive Industry,"

[98] J. McPherson, *Reliability Physics and Engineering: Time-To-Failure Modeling*. Boston, MA: Springer US, 2010, ISBN: 978-1-4419-6347-5 978-1-4419-6348-2. DOI: 10.1007/978-1-4419-6348-2. [Online]. Available: http://link.springer.com/10.1007/978-1-4419-6348-2 (visited on 12/02/2020).

[99] R. Baumann, "From COTS to space grade electronics-improving reliability for Harsh environments," in *Proc. IEEE Int. Integrated Reliability Workshop Final Rep.*, 2014, p. 51.

[100] D. Hoffpauir, "COTS Components in Spacecraft Systems: Understanding the Risk," NASA Engineering & Safety Center (NESC), Technical Update. [Online]. Available: http://www.nasa.gov/offices/nesc/articles/cots-components-in-spacecraft-systems.html (visited on 12/02/2020).

[101] S. Borkar, "Design challenges of technology scaling," *IEEE Micro*, vol. 19, no. 4, pp. 23–29, Jul. 1999, ISSN: 1937-4143. DOI: 10.1109/40.782564.

[102] J. Srinivasan, S. V. Adve, P. Bose, and J. A. Rivers, "The impact of technology scaling on lifetime reliability," in *International Conference on Dependable Systems and Networks, 2004*, Jun. 2004, pp. 177–186. DOI: 10.1109/DSN.2004.1311888.

[103] J. H. Stathis, "Reliability limits for the gate insulator in CMOS technology," *IBM Journal of Research and Development*, vol. 46, no. 2.3, pp. 265–286, 2002.

[104] E. Wu, J. Sune, W. Lai, *et al.*, "Interplay of voltage and temperature acceleration of oxide breakdown for ultra-thin gate oxides," *Solid-State Electronics*, vol. 46, no. 11, pp. 1787–1798, 2002.

[105] C.-K. Hu, R. Rosenberg, H. S. Rathore, D. B. Nguyen, and B. Agarwala, "Scaling effect on electromigration in on-chip Cu wiring," in *Proceedings of the IEEE 1999 International Interconnect Technology Conference (Cat. No. 99EX247)*, IEEE, 1999, pp. 267–269.

[106] D. S. Gardner, J. D. Meindl, and K. C. Saraswat, "Interconnection and electromigration scaling theory," *IEEE Transactions on Electron Devices*, vol. 34, no. 3, pp. 633–643, Mar. 1987, ISSN: 1557-9646. DOI: 10.1109/T-ED.1987.22974.

[107] L. Cao, K. J. Ganesh, L. Zhang, *et al.*, "Grain structure analysis and effect on electromigration reliability in nanoscale Cu interconnects," *Applied Physics Letters*, vol. 102, no. 13, p. 131 907, Apr. 1, 2013, ISSN: 0003-6951. DOI: 10.1063/1.4799484. [Online]. Available: https://aip.scitation.org/doi/full/10.1063/1.4799484 (visited on 12/06/2020).

[108] D. G. Pierce and P. G. Brusius, "Electromigration: A review," *Microelectronics Reliability*, Reliability Physics of Advanced Electron Devices, vol. 37, no. 7, pp. 1053–1072, Jul. 1, 1997, ISSN: 0026-2714. DOI: 10.1016/S0026-2714(96)00268-5. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271496002685 (visited on 12/06/2020).

[109] S. Beyne, O. V. Pedreira, I. D. Wolf, Z. T\ Hokei, and K. Croes, "A novel electromigration characterization method based on low-frequency noise measurements," *Semiconductor Science and Technology*, vol. 34, no. 7, p. 075 002, Jun. 2019, ISSN: 0268-1242. DOI: 10.1088/1361-6641/ab1963. [Online]. Available: https://doi.org/10.1088%2F1361-6641%2Fab1963 (visited on 12/06/2020).

[110] W. Weisenberger, B. Dodson, and A. Christou, "RF Reliability Testing of L-Band Power Transistors," in *S-MTT International Microwave Symposium Digest*, vol. 74, Jun. 1974, pp. 138–138. DOI: 10.1109/MWSYM.1974.1123511.

[111] D. Stephens, T. Vanhoucke, and J. Donkers, "RF reliability of short channel NMOS devices," in *2009 IEEE Radio Frequency Integrated Circuits Symposium*, IEEE, 2009, pp. 343–346.

[112] C. Yu and J. S. Yuan, "RF reliability subject to dynamic voltage stress in NMOS circuits [power amplifier example]," in *2005 IEEE International Reliability Physics Symposium, 2005. Proceedings. 43rd Annual.*, IEEE, 2005, pp. 431–434.

[113] G. T. Sasse, F. G. Kuper, and J. Schmitz, "MOSFET degradation under RF stress," *IEEE transactions on electron devices*, vol. 55, no. 11, pp. 3167–3174, 2008.

[114] S. Naseh, M. J. Deen, and O. Marinov, "Effects of hot-carrier stress on the RF performance of 0.18 /spl mu/m technology NMOSFETs and circuits," in *2002 IEEE International Reliability Physics Symposium. Proceedings. 40th Annual (Cat. No.02CH37320)*, Apr. 2002, pp. 98–104. DOI: 10.1109/RELPHY.2002.996616.

[115] J. P. Walko and B. Abadeer, "RF S-parameter degradation under hot carrier stress," in *2004 IEEE International Reliability Physics Symposium. Proceedings*, IEEE, 2004, pp. 422–425.

[116] C.-H. Liu, R.-L. Wang, Y.-K. Su, C.-H. Tu, and Y.-Z. Juang, "DC and RF Degradation Induced by High RF Power Stresses in 0.18-$$\backslash$mu$\backslash$hbox ${$m$}$ $ nMOSFETs," *IEEE Transactions on Device and Materials Reliability*, vol. 10, no. 3, pp. 317–323, 2010.

[117] L. Negre, D. Roy, S. Boret, P. Scheer, D. Gloria, and G. Ghibaudo, "Advanced 45nm MOSFET small-signal equivalent circuit aging under DC and RF hot carrier stress," in *2011 International Reliability Physics Symposium*, IEEE, 2011, HV–1.

[118] D. K. Huynh, Q. H. Le, P. Duhan, D. Wang, T. Kämpfe, and M. Rudolph, "Analysis of Hot-Carrier Degradation in 22nm FDSOI Transistors Using RF Small-Signal Characteristics," in *2020 German Microwave Conference (GeMiC)*, Mar. 2020, pp. 244–247.

[119] G. T. Sasse and J. Schmitz, "Application and Evaluation of the RF Charge-Pumping Technique," *IEEE Transactions on Electron Devices*, vol. 55, no. 3, pp. 881–889, Mar. 2008, ISSN: 1557-9646. DOI: 10.1109/TED.2007.915088.

[120] L. Negre, D. Roy, P. Scheer, D. Gloria, and G. Ghibaudo, "An advanced RF-CV method as a powerful characterization tool for the description of HC induced defect generation at microscopic level," in *2011 IEEE International Integrated Reliability Workshop Final Report*, Oct. 2011, pp. 73–76. DOI: 10.1109/IIRW.2011.6142592.

[121] Enjun Xiao, J. S. Yuan, and Hong Yang, "CMOS RF and DC reliability subject to hot carrier stress and oxide soft breakdown," *IEEE Transactions on Device and Materials Reliability*, vol. 4, no. 1, pp. 92–98, Mar. 2004, ISSN: 1558-2574. DOI: 10.1109/TDMR.2004.824365.

[122] T. Chohan, S. Slesazeck, G. Krause, J. Trommer, S. Lehmann, and T. Mikolajick, "SOTF-BTI - an S-Parameters based on-the-fly Bias Temperature Instability Characterization Method," in *2020 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, Jul. 2020, pp. 1–5. DOI: 10.1109/IPFA49335.2020.9260732.

[123] A. Goetzberger and H. E. Nigh, "Surface charge after annealing of Al-SiO 2-Si structures under bias," *Proceedings of the IEEE*, vol. 54, no. 10, pp. 1454–1454, 1966.

[124] S. Mahapatra and U. Sharma, "A Review of Hot Carrier Degradation in n-Channel MOSFETs—Part I: Physical Mechanism," *IEEE Transactions on Electron Devices*, vol. 67, no. 7, pp. 2660–2671, Jul. 2020, ISSN: 1557-9646. DOI: 10.1109/TED.2020.2994302.

[125] S. Mahapatra and U. Sharma, "A Review of Hot Carrier Degradation in n-Channel MOSFETs—Part II: Technology Scaling," *IEEE Transactions on Electron Devices*, vol. 67, no. 7, pp. 2672–2681, Jul. 2020, ISSN: 1557-9646. DOI: 10.1109/TED.2020.2994301.

[126] S. Tyaginov and T. Grasser, "Modeling of hot-carrier degradation: Physics and controversial issues," in *2012 IEEE International Integrated Reliability Workshop Final Report*, IEEE, 2012, pp. 206–215.

[127] M. G. Ancona, N. S. Saks, and D. McCarthy, "Lateral distribution of hot-carrier-induced interface traps in MOSFETs," *IEEE Transactions on Electron Devices*, vol. 35, no. 12, pp. 2221–2228, 1988.

[128] P. Heremans, R. Bellens, G. Groeseneken, and H. E. Maes, "Consistent model for the hot-carrier degradation in n-channel and p-channel MOSFETs," *IEEE Transactions on Electron Devices*, vol. 35, no. 12, pp. 2194–2209, 1988.

[129] J. F. Chen, S.-Y. Chen, K.-M. Wu, and C. M. Liu, "Investigation of hot-carrier-induced degradation mechanisms in p-type high-voltage drain extended metal–oxide–semiconductor transistors," *Japanese Journal of Applied Physics*, vol. 48, p. 04C039, 4S 2009.

[130] I. Starkov, H. Enichlmair, S. Tyaginov, and T. Grasser, "Analysis of the threshold voltage turn-around effect in high-voltage n-MOSFETs due to hot-carrier stress," in *2012 IEEE International Reliability Physics Symposium (IRPS)*, IEEE, 2012, XT–7.

[131] A. Bravaix, C. Guerin, V. Huard, D. Roy, J. Roux, and E. Vincent, "Hot-Carrier acceleration factors for low power management in DC-AC stressed 40nm NMOS node at high temperature," in *2009 IEEE International Reliability Physics Symposium*, Apr. 2009, pp. 531–548. DOI: 10.1109/IRPS.2009.5173308.

[132] B. Tuttle and C. G. Van de Walle, "Structure, energetics, and vibrational properties of Si-H bond dissociation in silicon," *Physical review B*, vol. 59, no. 20, p. 12 884, 1999.

[133] Chenming Hu, "Lucky-electron model of channel hot electron emission," in *1979 International Electron Devices Meeting*, Dec. 1979, pp. 22–25. DOI: 10.1109/IEDM.1979.189529.

[134] C. Hu, S. C. Tam, F.-C. Hsu, P.-K. Ko, T.-Y. Chan, and K. W. Terrill, "Hot-electron-induced MOSFET degradation-model, monitor, and improvement," *IEEE Journal of Solid-State Circuits*, vol. 20, no. 1, pp. 295–305, 1985.

[135] D. J. DiMaria and J. W. Stasiak, "Trap creation in silicon dioxide produced by hot electrons," *Journal of Applied Physics*, vol. 65, no. 6, pp. 2342–2356, 1989.

[136] D. J. DiMaria, "Defect generation under substrate-hot-electron injection into ultrathin silicon dioxide layers," *Journal of applied physics*, vol. 86, no. 4, pp. 2100–2109, 1999.

[137] S. E. Rauch, F. J. Guarin, and G. LaRosa, "Impact of EE scattering to the hot carrier degradation of deep submicron NMOSFETs," *IEEE Electron Device Letters*, vol. 19, no. 12, pp. 463–465, 1998.

[138] S. E. Rauch and G. La Rosa, "The energy-driven paradigm of NMOSFET hot-carrier effects," *IEEE Transactions on Device and Materials Reliability*, vol. 5, no. 4, pp. 701–705, 2005.

[139] W. McMahon, A. Haggag, and K. Hess, "Reliability scaling issues for nanoscale devices," *IEEE Transactions on Nanotechnology*, vol. 2, no. 1, pp. 33–38, Mar. 2003, ISSN: 1941-0085. DOI: 10.1109/TNANO.2003.808515.

[140] W. McMahon, K. Matsuda, J. Lee, K. Hess, and J. W. Lyding, "The effects of a multiple carrier model of interface trap generation on lifetime extraction for MOSFETs," in *2002 International Conference on Modeling and Simulation of Microsystems-MSM 2002*, 2002, pp. 576–579.

[141] K. Hess, A. Haggag, W. McMahon, *et al.*, "Simulation of Si-SiO/sub 2/defect generation in CMOS chips: From atomistic structure to chip failure rates," in *International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No. 00CH37138)*, IEEE, 2000, pp. 93–96.

[142] S. E. Rauch, G. La Rosa, and F. J. Guarin, "Role of EE scattering in the enhancement of channel hot carrier degradation of deep-submicron NMOSFETs at high V/sub GS/conditions," *IEEE transactions on device and materials reliability*, vol. 1, no. 2, pp. 113–119, 2001.

[143] C. Guérin, V. Huard, and A. Bravaix, "General framework about defect creation at the Si/ Si O 2 interface," *Journal of Applied Physics*, vol. 105, no. 11, p. 114 513, 2009.

[144] S. E. Tyaginov, I. A. Starkov, O. Triebl, *et al.*, "Interface traps density-of-states as a vital component for hot-carrier degradation modeling," *Microelectronics Reliability*, vol. 50, no. 9-11, pp. 1267–1272, 2010.

[145] S. Tyaginov, "Physics-Based Modeling of Hot-Carrier Degradation," in *Hot Carrier Degradation in Semiconductor Devices*, T. Grasser, Ed., Cham: Springer International Publishing, 2015, pp. 105–150, ISBN: 978-3-319-08994-2. DOI: 10.1007/978-3-319-08994-2_4. [Online]. Available: https://doi.org/10.1007/978-3-319-08994-2_4 (visited on 08/11/2020).

[146] M. Song, K. P. MacWilliams, and J. C. Woo, "Comparison of NMOS and PMOS hot carrier effects from 300 to 77 K," *IEEE Transactions on Electron Devices*, vol. 44, no. 2, pp. 268–276, 1997.

[147] W. H. Qin, W. K. Chim, D. S. H. Chan, and C. L. Lou, "Modelling the degradation in the subthreshold characteristics of submicrometre LDD PMOSFETs under hot-carrier stressing," *Semiconductor science and technology*, vol. 13, no. 5, p. 453, 1998.

[148] S. Rauch and G. L. Rosa, "CMOS hot carrier: From physics to end of life projections, and qualification," in *Proc. International Reliability Physics Symposium (IRPS), Tutorial*, 2010.

[149] W. Arfaoui, X. Federspiel, P. Mora, M. Rafik, D. Roy, and A. Bravaix, "Experimental analysis of defect nature and localization under hot-carrier and bias temperature damage in advanced CMOS nodes," in *2013 IEEE International Integrated Reliability Workshop Final Report*, IEEE, 2013, pp. 78–83.

[150] F.-C. Hsu and K.-Y. Chiu, "Temperature dependence of hot-electron-induced degradation in MOSFET's," *IEEE Electron Device Letters*, vol. 5, no. 5, pp. 148–150, 1984.

[151] K. T. Lee, C. Y. Kang, O. S. Yoo, *et al.*, "PBTI-associated high-temperature hot carrier degradation of nMOSFETs with metal-gate/high-$ k $ dielectrics," *IEEE electron device letters*, vol. 29, no. 4, pp. 389–391, 2008.

[152] X. Federspiel, D. Angot, M. Rafik, *et al.*, "28nm node bulk vs FDSOI reliability comparison," in *2012 IEEE International Reliability Physics Symposium (IRPS)*, IEEE, 2012, 3B–1.

[153] T. Chohan, S. Slesazeck, J. Trommer, *et al.*, "Impact of hot carrier stress on small-signal parameters of FD-SOI NMOSFETs," in *2017 IEEE International Integrated Reliability Workshop (IIRW)*, IEEE, 2017, pp. 1–5.

[154] E. Amat, J. Martin-Martinez, M. B. Gonzalez, *et al.*, "Processing dependences of channel hot-carrier degradation on strained-Si p-channel metal-oxide semiconductor field-effect transistors," *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena*, vol. 29, no. 1, 01AB07, 2011.

[155] P. A. Childs and C. C. C. Leung, "A one-dimensional solution of the Boltzmann transport equation including electron–electron interactions," *Journal of Applied Physics*, vol. 79, no. 1, pp. 222–227, 1996.

[156] B. Ricco, E. Sangiorgi, and D. Cantarelli, "Low voltage hot-electron effects in short channel MOSFETs," in *1984 International Electron Devices Meeting*, IEEE, 1984, pp. 92–95.

[157] A. Abramo, C. Fiegna, and F. Venturi, "Hot carrier effects in short MOSFETs at low applied voltages," in *Proceedings of International Electron Devices Meeting*, IEEE, 1995, pp. 301–304.

[158] J. D. Bude, "Gate current by impact ionization feedback in sub-micron MOSFET technologies," in *1995 Symposium on VLSI Technology. Digest of Technical Papers*, IEEE, 1995, pp. 101–102.

[159] Y. Miura and Y. Matukura, "Investigation of Silicon-Silicon Dioxide Interface Using MOS Structure," *Japanese Journal of Applied Physics*, vol. 5, no. 2, p. 180, Feb. 1, 1966, ISSN: 1347-4065. DOI: 10.1143/JJAP.5.180. [Online]. Available: https://iopscience.iop.org/article/10.1143/JJAP.5.180/meta (visited on 12/09/2020).

[160] K. Uwasawa, T. Yamamoto, and T. Mogami, "A new degradation mode of scaled p/sup+/polysilicon gate pMOSFETs induced by bias temperature (BT) instability," in *Proceedings of International Electron Devices Meeting*, IEEE, 1995, pp. 871–874.

[161] G. La Rosa, F. Guarin, S. Rauch, A. Acovic, J. Lukaitis, and E. Crabbe, "NBTI-channel hot carrier effects in PMOSFETs in advanced CMOS technologies," in *1997 IEEE International Reliability Physics Symposium Proceedings. 35th Annual*, IEEE, 1997, pp. 282–286.

[162] D. K. Schroder, "Negative bias temperature instability: What do we understand?" *Microelectronics Reliability*, vol. 47, no. 6, pp. 841–852, 2007.

[163] V. Huard, M. Denais, and C. Parthasarathy, "NBTI degradation: From physical mechanisms to modelling," *Microelectronics Reliability*, vol. 46, no. 1, pp. 1–23, 2006.

[164] J. H. Stathis and S. Zafar, "The negative bias temperature instability in MOS devices: A review," *Microelectronics Reliability*, vol. 46, no. 2-4, pp. 270–286, 2006.

[165] J. H. Stathis, S. Mahapatra, and T. Grasser, "Controversial issues in negative bias temperature instability," *Microelectronics Reliability*, vol. 81, pp. 244–251, 2018.

[166] T. Grasser, T. Aichinger, G. Pobegen, *et al.*, "The 'permanent'component of NBTI: Composition and annealing," in *2011 International Reliability Physics Symposium*, IEEE, 2011, 6A–2.

[167] N. Parihar, N. Goel, A. Chaudhary, and S. Mahapatra, "A modeling framework for NBTI degradation under dynamic voltage and frequency scaling," *IEEE Transactions on Electron Devices*, vol. 63, no. 3, pp. 946–953, 2016.

[168] T. Grasser, B. Kaczer, W. Goes, *et al.*, "The paradigm shift in understanding the bias temperature instability: From reaction–diffusion to switching oxide traps," *IEEE Transactions on Electron Devices*, vol. 58, no. 11, pp. 3652–3666, 2011.

[169] T. Grasser, "Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities," *Microelectronics Reliability*, vol. 52, no. 1, pp. 39–70, 2012.

[170] S. Mahapatra, A. E. Islam, S. Deora, *et al.*, "A critical re-evaluation of the usefulness of RD framework in predicting NBTI stress and recovery," in *2011 International Reliability Physics Symposium*, IEEE, 2011, 6A–3.

[171] T. Grasser, K. Rott, H. Reisinger, M. Waltl, F. Schanovsky, and B. Kaczer, "NBTI in nanoscale MOSFETs—The ultimate modeling benchmark," *IEEE Transactions on Electron Devices*, vol. 61, no. 11, pp. 3586–3593, 2014.

[172] T. Grasser, K. Rott, H. Reisinger, *et al.*, "Hydrogen-related volatile defects as the possible cause for the recoverable component of NBTI," in *2013 IEEE International Electron Devices Meeting*, IEEE, 2013, pp. 15–5.

[173] S. Mahapatra, V. Huard, A. Kerber, V. Reddy, S. Kalpat, and A. Haggag, "Universality of NBTI-From devices to circuits and products," in *2014 IEEE International Reliability Physics Symposium*, IEEE, 2014, 3B–1.

[174] H. Reisinger, O. Blank, W. Heinrigs, A. Muhlhoff, W. Gustin, and C. Schlunder, "Analysis of NBTI degradation-and recovery-behavior based on ultra fast VT-measurements," in *2006 IEEE International Reliability Physics Symposium Proceedings*, IEEE, 2006, pp. 448–453.

[175] T. Grasser, W. Gos, V. Sverdlov, and B. Kaczer, "The universality of NBTI relaxation and its implications for modeling and characterization," in *2007 IEEE International Reliability Physics Symposium Proceedings. 45th Annual*, IEEE, 2007, pp. 268–280.

[176] T. Grasser, H. Reisinger, P.-J. Wagner, F. Schanovsky, W. Gös, and B. Kaczer, "The time dependent defect spectroscopy (TDDS) for the characterization of the bias temperature instability," in *2010 IEEE International Reliability Physics Symposium*, IEEE, 2010, pp. 16–25.

[177] T. Grasser, H. Reisinger, W. Goes, *et al.*, "Switching oxide traps as the missing link between negative bias temperature instability and random telegraph noise," in *2009 IEEE International Electron Devices Meeting (IEDM)*, IEEE, 2009, pp. 1–4.

[178] M. J. Kirton and M. J. Uren, "Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency ($1/f$) noise," *Advances in Physics*, vol. 38, no. 4, pp. 367–468, 1989.

[179] V. Huard, "Two independent components modeling for negative bias temperature instability," in *2010 IEEE International Reliability Physics Symposium*, IEEE, 2010, pp. 33–42.

[180] H. Reisinger, T. Grasser, W. Gustin, and C. Schlünder, "The statistical analysis of individual defects constituting NBTI and its implications for modeling DC-and AC-stress," in *2010 IEEE International Reliability Physics Symposium*, IEEE, 2010, pp. 7–15.

[181] B. Kaczer, T. Grasser, P. J. Roussel, *et al.*, "Origin of NBTI variability in deeply scaled pFETs," in *2010 IEEE International Reliability Physics Symposium*, IEEE, 2010, pp. 26–32.

[182] T. Chohan, S. Slesazeck, J. Trommer, *et al.*, "Impact of BTI Stress on RF Small Signal Parameters of FDSOI MOSFETs," in *2019 IEEE International Integrated Reliability Workshop (IIRW)*, IEEE, 2019, pp. 1–4.

[183] T. Grasser, P.-J. Wagner, P. Hehenberger, W. Goes, and B. Kaczer, "A rigorous study of measurement techniques for negative bias temperature instability," *IEEE Transactions on Device and Materials Reliability*, vol. 8, no. 3, pp. 526–535, 2008.

[184] H. Reisinger, O. Blank, W. Heinrigs, W. Gustin, and C. Schlunder, "A Comparison of Very Fast to Very Slow Components in Degradation and Recovery Due to NBTI and Bulk Hole Trapping to Existing Physical Models," *IEEE Transactions on Device and Materials Reliability*, vol. 7, no. 1, pp. 119–129, Mar. 2007, ISSN: 1558-2574. DOI: 10.1109/TDMR.2007.898229.

[185] M. Denais, C. Parthasarathy, G. Ribes, *et al.*, "On-the-fly characterization of NBTI in ultra-thin gate oxide PMOSFET's," in *IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004.*, IEEE, 2004, pp. 109–112.

[186] Y. S. Ju and K. E. Goodson, "Phonon scattering in silicon films with thickness of order 100 nm," *Applied Physics Letters*, vol. 74, no. 20, pp. 3005–3007, 1999.

[187] S. Mazumder and A. Majumdar, "Monte Carlo study of phonon transport in solid thin films including dispersion and polarization," *J. Heat Transfer*, vol. 123, no. 4, pp. 749–759, 2001.

[188] D. Ferry, *Semiconductor Transport*. CRC Press, 2016.

[189] E. Pop, K. Banerjee, P. Sverdrup, R. Dutton, and K. Goodson, "Localized heating effects and scaling of sub-0.18 micron CMOS devices," in *International Electron Devices Meeting. Technical Digest (Cat. No.01CH37224)*, Dec. 2001, pp. 31.1.1–31.1.4. DOI: 10.1109/IEDM.2001.979598.

[190] M. Artaki and P. J. Price, "Hot phonon effects in silicon field-effect transistors," *Journal of applied physics*, vol. 65, no. 3, pp. 1317–1320, 1989.

[191] M. Lundstrom, *Fundamentals of Carrier Transport*. Cambridge university press, 2009.

[192] C. Fiegna, Y. Yang, E. Sangiorgi, and A. G. O'Neill, "Analysis of Self-Heating Effects in Ultrathin-Body SOI MOSFETs by Device Simulation," *IEEE Transactions on Electron Devices*, vol. 55, no. 1, pp. 233–244, Jan. 2008, ISSN: 1557-9646. DOI: 10.1109/TED.2007.911354.

[193] G. Chen, "Nonlocal and nonequilibrium heat conduction in the vicinity of nanoparticles," 1996.

[194] P. G. Sverdrup, Y. Sungtaek Ju, and K. E. Goodson, "Sub-continuum simulations of heat conduction in silicon-on-insulator transistors," *J. Heat Transfer*, vol. 123, no. 1, pp. 130–137, 2001.

[195] E. Pop, S. Sinha, and K. E. Goodson, "Heat Generation and Transport in Nanometer-Scale Transistors," *Proceedings of the IEEE*, vol. 94, no. 8, pp. 1587–1601, Aug. 2006, ISSN: 1558-2256. DOI: 10.1109/JPROC.2006.879794.

[196] M. A. Panzer, M. Shandalov, J. A. Rowlette, *et al.*, "Thermal properties of ultrathin hafnium oxide gate dielectric films," *IEEE Electron Device Letters*, vol. 30, no. 12, pp. 1269–1271, 2009.

[197] T. Yamane, N. Nagai, S.-i. Katayama, and M. Todoki, "Measurement of thermal conductivity of silicon dioxide thin films using a 3$ømega$ method," *Journal of applied physics*, vol. 91, no. 12, pp. 9772–9776, 2002.

[198] D. Vasileska, K. Raleva, and S. M. Goodnick, "Self-Heating Effects in Nanoscale FD SOI Devices: The Role of the Substrate, Boundary Conditions at Various Interfaces, and the Dielectric Material Type for the BOX," *IEEE Transactions on Electron Devices*, vol. 56, no. 12, pp. 3064–3071, Dec. 2009, ISSN: 1557-9646. DOI: 10.1109/TED.2009.2032615.

[199] S. Makovejev, J. Raskin, D. Flandre, *et al.*, "Comparison of small-signal output conductance frequency dependence in UTBB SOI MOSFETs with and without ground plane," in *IEEE 2011 International SOI Conference*, Oct. 2011, pp. 1–2. DOI: 10.1109/SOI.2011.6081717.

[200] K. Raleva, D. Vasileska, S. M. Goodnick, and M. Nedjalkov, "Modeling thermal effects in nanodevices," *IEEE Transactions on Electron Devices*, vol. 55, no. 6, pp. 1306–1316, 2008.

[201] M. Braccioli, G. Curatola, Y. Yang, E. Sangiorgi, and C. Fiegna, "Simulation of self-heating effects in different SOI MOS architectures," *Solid-state electronics*, vol. 53, no. 4, pp. 445–451, 2009.

[202] N. Rinaldi, "Small-signal operation of semiconductor devices including self-heating, with application to thermal characterization and instability analysis," *IEEE Transactions on Electron Devices*, vol. 48, no. 2, pp. 323–331, Feb. 2001, ISSN: 1557-9646. DOI: 10.1109/16.902734.

[203] S. Makovejev, S. H. Olsen, V. Kilchytska, and J.-P. Raskin, "Time and Frequency Domain Characterization of Transistor Self-Heating," *IEEE Transactions on Electron Devices*, vol. 60, no. 6, pp. 1844–1851, Jun. 2013, ISSN: 1557-9646. DOI: 10.1109/TED.2013.2259174.

[204] S. Makovejev, B. K. Esfeh, V. Barral, *et al.*, "Wide frequency band assessment of 28 nm FDSOI technology platform for analogue and RF applications," *Solid-State Electronics*, vol. 108, pp. 47–52, 2015.

[205] N. Rodriguez, C. Navarro, F. Andrieu, O. Faynot, F. Gamiz, and S. Cristoloveanu, "Self-heating effects in ultrathin FD SOI transistors," in *IEEE 2011 International SOI Conference*, Oct. 2011, pp. 1–2. DOI: 10.1109/SOI.2011.6081685.

[206] B. Tenbroek, M. Lee, W. Redman-White, J. Bunyan, and M. Uren, "Self-heating effects in SOI MOSFETs and their measurement by small signal conductance techniques," *IEEE Transactions on Electron Devices*, vol. 43, no. 12, pp. 2240–2248, Dec. 1996, ISSN: 1557-9646. DOI: 10.1109/16.544417.

[207] K. Chain, J.-h. Huang, J. Duster, P. K. Ko, and C. Hu, "A MOSFET electron mobility model of wide temperature range (77-400 K) for IC simulation," *Semiconductor science and technology*, vol. 12, no. 4, p. 355, 1997.

[208] A. K. Goel and T. H. Tan, "High-temperature and self-heating effects in fully depleted SOI MOSFETs," *Microelectronics Journal*, vol. 37, no. 9, pp. 963–975, Sep. 1, 2006, ISSN: 0026-2692. DOI: 10.1016/j.mejo.2006.01.006. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026269206000188 (visited on 07/28/2020).

[209] S. N. Mohammad, "Unified model for drift velocities of electrons and holes in semiconductors as a function of temperature and electric field," *Solid-State Electronics*, vol. 35, no. 10, pp. 1391–1396, Oct. 1992, ISSN: 0038-1101. DOI: 10.1016/0038-1101(92)90072-K. (visited on 07/09/2023).

[210] D. Wolpert and P. Ampadu, "Temperature Effects in Semiconductors," in *Managing Temperature Effects in Nanoscale Adaptive Systems*, D. Wolpert and P. Ampadu, Eds., New York, NY: Springer, 2012, pp. 15–33, ISBN: 978-1-4614-0748-5. DOI: 10.1007/978-1-4614-0748-5_2.

[211] T. Chohan, Z. Zhao, S. Lehmann, *et al.*, "Implication of Self-Heating Effect on Device Reliability Characterization of Multi-Finger n-MOSFETs on 22FDSOI," *IEEE Transactions on Device and Materials Reliability*, vol. 22, no. 3, pp. 387–395, Sep. 2022, ISSN: 1558-2574. DOI: 10.1109/TDMR.2022.3183630.

[212] J. Wu, Y. Fang, B. Markman, H.-Y. Tseng, and M. J. W. Rodwell, "$L_g = 30$ nm InAs Channel MOSFETs Exhibiting $f_\textit max =410$ GHz and $f_t = 357$ GHz," *IEEE Electron Device Letters*, vol. 39, no. 4, pp. 472–475, Apr. 2018, ISSN: 1558-0563. DOI: 10.1109/LED.2018.2803786.

[213] S. Yadav, A. Bellaouar, J. Wong, *et al.*, "Demonstration and Modelling of Excellent RF Switch Performance of 22nm FD-SOI Technology for Millimeter-Wave Applications," in *ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC)*, Sep. 2019, pp. 170–173. DOI: 10.1109/ESSDERC.2019.8901823.

[214] C. B. Zota, C. Convertino, M. Sousa, D. Caimi, K. Moselund, and L. Czornomaz, "High-Frequency Quantum Well InGaAs-on-Si MOSFETs With Scaled Gate Lengths," *IEEE Electron Device Letters*, vol. 40, no. 4, pp. 538–541, Apr. 2019, ISSN: 1558-0563. DOI: 10.1109/LED.2019.2902519.

[215] C. B. Zota, C. Convertino, V. Deshpande, *et al.*, "InGaAs-on-Insulator MOSFETs Featuring Scaled Logic Devices and Record RF Performance," in *2018 IEEE Symposium on VLSI Technology*, Jun. 2018, pp. 165–166. DOI: 10.1109/VLSIT.2018.8510631.

[216] K. Chabak, D. Walker, A. Green, *et al.*, "Sub-Micron Gallium Oxide Radio Frequency Field-Effect Transistors," in *2018 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP)*, Jul. 2018, pp. 1–3. DOI: 10.1109/IMWS-AMP.2018.8457153.

[217] F. Sischka and T. Gneiting, "Rf mos measurements," *International journal of high speed electronics and systems*, vol. 11, no. 04, pp. 887–951, 2001.

[218] G. A. Campbell and R. M. Foster, "Maximum Output Networks for Telephone Substation and Repeater Circuits," *Transactions of the American Institute of Electrical Engineers*, vol. XXXIX, no. 1, pp. 231–290, Jan. 1920, ISSN: 2330-9431. DOI: 10.1109/T-AIEE.1920.4764962.

[219] E. Matthews, "The Use of Scattering Matrices in Microwave Circuits," *IRE Transactions on Microwave Theory and Techniques*, vol. 3, no. 3, pp. 21–26, Apr. 1955, ISSN: 2331-088X. DOI: 10.1109/TMTT.1955.1124941.

[220] C. G. Montgomery, R. H. Dicke, and E. M. Purcell, *Principles of Microwave Circuits*. Iet, 1987.

[221] F. Ellinger, *Radio Frequency Integrated Circuits and Technologies*. Berlin Heidelberg: Springer-Verlag, 2007, ISBN: 978-3-540-35790-2. DOI: 10.1007/978-3-540-35790-2.

[222] D. M. Pozar, *Microwave Engineering*. John wiley & sons, 2009.

[223] D. A. Frickey, "Conversions between S, Z, Y, H, ABCD, and T parameters which are valid for complex source and load impedances," *IEEE Transactions on microwave theory and techniques*, vol. 42, no. 2, pp. 205–211, 1994.

[224] D. Koller, S. Durant, C. Rowland, E. Bryerton, and J. Hesler, "Initial measurements with WM164 (1.1–1.5THz) VNA extenders," in *2016 41st International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz)*, Sep. 2016, pp. 1–2. DOI: 10.1109/IRMMW-THz.2016.7758434.

[225] J. L. Hesler, Y. Duan, B. Foley, and T. W. Crowe, "THz vector network analyzer measurements and calibration," in *21st Int. Symp. on Space Terahertz Technology, Oxford*, 2010, pp. 23–25.

[226] A. K. Fung, D. Dawson, L. Samoska, K. Lee, C. Oleson, and G. Boll, "On-Wafer Vector Network Analyzer Measurements in the 220-325 GHz Frequency Band," in *2006 IEEE MTT-S International Microwave Symposium Digest*, Jun. 2006, pp. 1931–1934. DOI: 10.1109/MWSYM.2006.249811.

[227] A. Fung, L. Samoska, G. Chattopadhyay, *et al.*, "Two-Port Vector Network Analyzer Measurements Up to 508 GHz," *IEEE Transactions on Instrumentation and Measurement*, vol. 57, no. 6, pp. 1166–1170, Jun. 2008, ISSN: 1557-9662. DOI: 10.1109/TIM.2007.915125.

[228] A. Rumiantsev and R. Doerner, "RF Probe Technology: History and Selected Topics," *IEEE Microwave Magazine*, vol. 14, no. 7, pp. 46–58, Nov. 2013, ISSN: 1557-9581. DOI: 10.1109/MMM.2013.2280241.

[229] G. Fisher, "A guide to Successful on Wafer Millimeter wave Rf characterisation," p. 116,

[230] R. Rimolo-Donadio, C. Schuster, X. Gu, Y. H. Kwark, and M. B. Ritter, "Analysis and Optimization of the Recessed Probe Launch for High Frequency Measurements of PCB Interconnects," in *2008 Design, Automation and Test in Europe*, Mar. 2008, pp. 252–255. DOI: 10.1109/DATE.2008.4484891.

[231] A. Rumiantsev and N. Ridler, "VNA calibration," *IEEE Microwave magazine*, vol. 9, no. 3, pp. 86–99, 2008.

[232] A. Davidson, K. Jones, and E. Strid, "LRM and LRRM calibrations with automatic determination of load inductance," in *36th ARFTG Conference Digest*, vol. 18, IEEE, 1990, pp. 57–63.

[233] A. M. E. Safwat and L. Hayden, "Sensitivity Analysis of Calibration Standards for SOLT and LRRM," in *58th ARFTG Conference Digest*, vol. 40, Nov. 2001, pp. 1–10. DOI: 10.1109/ARFTG.2001.327488.

[234] S. El Ghouli, P. Scheer, M. Minondo, *et al.*, "Analog and RF modeling of FDSOI UTBB MOSFET using Leti-UTSOI model," in *2016 MIXDES - 23rd International Conference Mixed Design of Integrated Circuits and Systems*, Jun. 2016, pp. 41–46. DOI: 10.1109/MIXDES.2016.7529697.

[235] K. Ng and W. Lynch, "Analysis of the gate-voltage-dependent series resistance of MOSFET's," *IEEE Transactions on Electron Devices*, vol. 33, no. 7, pp. 965–972, Jul. 1986, ISSN: 1557-9646. DOI: 10.1109/T-ED.1986.22602.

[236] E. Torres-Rios, R. Torres-Torres, G. Valdovinos-Fierro, and E. Gutierrez-D, "A method to determine the gate bias-dependent and gate bias-independent components of MOSFET series resistance from S-parameters," *IEEE Transactions on Electron Devices*, vol. 53, no. 3, pp. 571–573, Mar. 2006, ISSN: 1557-9646. DOI: 10.1109/TED.2006.870328.

[237] K. Lim and X. Zhou, "A physically-based semi-empirical series resistance model for deep-submicron MOSFET I-V modeling," *IEEE Transactions on Electron Devices*, vol. 47, no. 6, pp. 1300–1302, Jun. 2000, ISSN: 1557-9646. DOI: 10.1109/16.842978.

[238] M. K. Md Arshad, V. Kilchytska, M. Emam, F. Andrieu, D. Flandre, and J. P. Raskin, "Effect of parasitic elements on UTBB FD SOI MOSFETs RF figures of merit," *Solid-State Electronics*, Selected Papers from EuroSOI 2013, vol. 97, pp. 38–44, Jul. 1, 2014, ISSN: 0038-1101. DOI: 10.1016/j.sse.2014.04.027. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0038110114000756 (visited on 09/21/2020).

[239] B. Heydari, M. Bohsali, E. Adabi, and A. M. Niknejad, "Millimeter-Wave Devices and Circuit Blocks up to 104 GHz in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2893–2903, Dec. 2007, ISSN: 1558-173X. DOI: 10.1109/JSSC.2007.908743.

[240] R. Torres-Torres, R. Murphy-Arteaga, and S. Decoutere, "MOSFET bias dependent series resistance extraction from RF measurements," *Electronics Letters*, vol. 39, no. 20, pp. 1476–1478, Oct. 2003, ISSN: 0013-5194. DOI: 10.1049/el:20030936.

[241] D. Esseni, H. Iwai, M. Saito, and B. Ricco, "Nonscaling of MOSFET's linear resistance in the deep submicrometer regime," *IEEE Electron Device Letters*, vol. 19, no. 4, pp. 131–133, Apr. 1998, ISSN: 1558-0563. DOI: 10.1109/55.663537.

[242] J. E. Meyer, "MOS models and circuit simulation," *RCA Rev.*, vol. 32, no. 1, pp. 42–63, 1971.

[243] D. E. Ward and R. W. Dutton, "A charge-oriented model for MOS transistor capacitances," *IEEE Journal of Solid-State Circuits*, vol. 13, no. 5, pp. 703–708, 1978.

[244] M. A. Cirit, "The Meyer model revisited: Why is charge not conserved? (MOS transistor)," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 8, no. 10, pp. 1033–1037, Oct. 1989, ISSN: 1937-4151. DOI: 10.1109/43.39064.

[245] Ping Yang, B. D. Epler, and P. K. Chatterjee, "An Investigation of the Charge Conservation Problem for MOSFET Circuit Simulation," *IEEE Journal of Solid-State Circuits*, vol. 18, no. 1, pp. 128–138, Feb. 1983, ISSN: 1558-173X. DOI: 10.1109/JSSC.1983.1051909.

[246] Y. Tsividis and C. McAndrew, *Operation and Modeling of the MOS Transistor*. Oxford University Press, 2011, 723 pp., ISBN: 978-0-19-517015-3.

[247] J. Hoentschel, L. Pirro, R. Carter, and M. Horstmann, "22FDX® Technologies for Ultra-Low Power IoT, RF and mmWave Applications," *Composants nanoélectroniques*, vol. 2, no. 1, 2019, ISSN: 25163914. DOI: 10.21494/ISTE.OP.2019.0321. [Online]. Available: https://www.openscience.fr/22FDX-R-Technologies-for-Ultra-Low-Power-IoT-RF-and-mmWave-Applications (visited on 10/18/2020).

[248] J. Watts, K. Sundaram, K. W. Johnny Chew, *et al.*, "RF-pFET in fully depleted SOI demonstrates 420 GHz FT," in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Jun. 2017, pp. 84–87. DOI: 10.1109/RFIC.2017.7969023.

[249] A. Shameli and P. Heydari, "Ultra-low power RFIC design using moderately inverted MOSFETs: An analytical/experimental study," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 2006*, Jun. 2006, 4 pp.–. DOI: 10.1109/RFIC.2006.1651193.

[250] Y. Tsividis, "Moderate inversion in MOS devices," *Solid-State Electronics*, vol. 25, no. 11, pp. 1099–1104, Nov. 1982, ISSN: 0038-1101. DOI: 10.1016/0038-1101(82)90148-4.

[251] T. Takahashi, T. Matsuki, T. Shinada, Y. Inoue, and K. Uchida, "Comparison of self-heating effect (SHE) in short-channel bulk and ultra-thin BOX SOI MOSFETs: Impacts of doped well, ambient temperature, and SOI/BOX thicknesses on SHE," in *2013 IEEE International Electron Devices Meeting*, Dec. 2013, pp. 7.4.1–7.4.4. DOI: 10.1109/IEDM.2013.6724581.

[252] S. Makovejev, N. Planes, M. Haond, D. Flandre, J. Raskin, and V. Kilchytska, "Self-heating in 28 nm bulk and FDSOI," in *EUROSOI-ULIS 2015: 2015 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon*, Jan. 2015, pp. 41–44. DOI: 10.1109/ULIS.2015.7063768.

[253] S. Sinha, E. Pop, and K. E. Goodson, "A split-flux model for phonon transport near hotspots," in *ASME International Mechanical Engineering Congress and Exposition*, vol. 47071, 2004, pp. 75–85.

[254] S. Sinha and K. E. Goodson, "Multiscale thermal modeling in nanoelectronics," *International Journal for Multiscale Computational Engineering*, vol. 3, no. 1, 2005.

[255] E. Pop, J. A. Rowlette, R. W. Dutton, and K. E. Goodson, "Joule heating under quasi-ballistic transport conditions in bulk and strained silicon devices," in *2005 International Conference On Simulation of Semiconductor Processes and Devices*, IEEE, 2005, pp. 307–310.

[256] E. N. Kumar, V. D. Maheta, S. Purawat, *et al.*, "Material dependence of NBTI physical mechanism in silicon oxynitride (SiON) p-MOSFETs: A comprehensive study by ultra-fast on-the-fly (UF-OTF) I DLIN technique," in *2007 IEEE International Electron Devices Meeting*, IEEE, 2007, pp. 809–812.

[257] D. Blackburn, "Temperature measurements of semiconductor devices - a review," in *Twentieth Annual IEEE Semiconductor Thermal Measurement and Management Symposium (IEEE Cat. No.04CH37545)*, Mar. 2004, pp. 70–80. DOI: 10.1109/STHERM.2004.1291304.

[258] A. Hefner, D. Berning, D. Blackburn, C. Chapuy, and S. Bouche, "A high-speed thermal imaging system for semiconductor device analysis," in *Seventeenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium (Cat. No.01CH37189)*, Mar. 2001, pp. 43–49. DOI: 10.1109/STHERM.2001.915143.

[259] A. Yasuda, H. Yamaguchi, Y. Tanabe, N. Owada, and S. Hirasawa, "Direct measurement of localized joule heating in silicon devices by means of newly developed high resolution IR microscopy," in *29th Annual Proceedings Reliability Physics 1991*, Apr. 1991, pp. 245–249. DOI: 10.1109/RELPHY.1991.146022.

[260] P. Mautry and J. Trager, "Investigation of self-heating in VLSI and ULSI MOSFETs," in *International Conference on Microelectronic Test Structures*, Mar. 1990, pp. 221–226. DOI: 10.1109/ICMTS.1990.67907.

[261] L. Su, J. Chung, D. Antoniadis, K. Goodson, and M. Flik, "Measurement and modeling of self-heating in SOI nMOSFET's," *IEEE Transactions on Electron Devices*, vol. 41, no. 1, pp. 69–75, Jan. 1994, ISSN: 1557-9646. DOI: 10.1109/16.259622.

[262] D. Walkey, T. Smy, R. Dickson, J. Brodsky, D. Zweidinger, and R. Fox, "Equivalent circuit modeling of static substrate thermal coupling using VCVS representation," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 9, pp. 1198–1206, Sep. 2002, ISSN: 1558-173X. DOI: 10.1109/JSSC.2002.801200.

[263] S. Khandelwal, J. Watts, E. Tamilmani, and L. Wagner, "Scalable thermal resistance model for single and multi-finger silicon-on-insulator MOSFETs," in *2011 IEEE ICMTS International Conference on Microelectronic Test Structures*, Apr. 2011, pp. 182–185. DOI: 10.1109/ICMTS.2011.5976843.

[264] R. Bunyan, M. Uren, J. Alderman, and W. Eccleston, "Use of noise thermometry to study the effects of self-heating in submicrometer SOI MOSFETs," *IEEE Electron Device Letters*, vol. 13, no. 5, pp. 279–281, May 1992, ISSN: 1558-0563. DOI: 10.1109/55.145053.

[265] K. Jenkins and J.-C. Sun, "Measurement of I-V curves of silicon-on-insulator (SOI) MOSFET's without self-heating," *IEEE Electron Device Letters*, vol. 16, no. 4, pp. 145–147, Apr. 1995, ISSN: 1558-0563. DOI: 10.1109/55.372496.

[266] K. Jenkins, J.-C. Sun, and J. Gautier, "Characteristics of SOI FET's under pulsed conditions," *IEEE Transactions on Electron Devices*, vol. 44, no. 11, pp. 1923–1930, Nov. 1997, ISSN: 1557-9646. DOI: 10.1109/16.641362.

[267] C. Anghel, A. Ionescu, N. Hefyene, and R. Gillon, "Self-heating characterization and extraction method for thermal resistance and capacitance in high voltage MOSFETs," in *ESSDERC '03. 33rd Conference on European Solid-State Device Research, 2003.*, Sep. 2003, pp. 449–452. DOI: 10.1109/ESSDERC.2003.1256910.

[268] W. Jin, W. Liu, S. Fung, P. Chan, and C. Hu, "SOI thermal impedance extraction methodology and its significance for circuit simulation," *IEEE Transactions on Electron Devices*, vol. 48, no. 4, pp. 730–736, Apr. 2001, ISSN: 1557-9646. DOI: 10.1109/16.915707.

[269] S. Makovejev, S. Olsen, and J.-P. Raskin, "RF Extraction of Self-Heating Effects in FinFETs," *IEEE Transactions on Electron Devices*, vol. 58, no. 10, pp. 3335–3341, Oct. 2011, ISSN: 1557-9646. DOI: 10.1109/TED.2011.2162333.

[270] A. Scholten, G. Smit, R. Pijper, *et al.*, "Experimental assessment of self-heating in SOI FinFETs," in *2009 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2009, pp. 1–4. DOI: 10.1109/IEDM.2009.5424362.

[271] S. Makovejev, S. Olsen, F. Andrieu, *et al.*, "On extraction of self-heating features in UTBB SOI MOSFETs," in *2012 13th International Conference on Ultimate Integration on Silicon (ULIS)*, IEEE, 2012, pp. 109–112.

[272] F. Shoucair, "Design consideration in high temperature analog CMOS integrated circuits," *IEEE Transactions on components, hybrids, and manufacturing technology*, vol. 9, no. 3, pp. 242–251, 1986.

[273] F. S. Shoucair, "Analytical and experimental methods for zero-temperature-coefficient biasing of MOS transistors," *Electronics Letters*, vol. 25, no. 17, pp. 1196–1198, 1989.

[274] L. M. Camillo, J. A. Martino, E. Simoen, and C. Claeys, "Simple Analytical Model to Study the ZTC Bias Point in PD and FD SOI MOSFETs," in *EuroSOI 2006 Conference Proceedings*, vol. 1, 2006, p. 77.

[275] L. M. Camillo, J. A. Martino, E. Simoen, and C. Claeys, "Investigation of the Gate Length and Drain Bias Dependence of the ZTC Biasing Point Instability of N-and P-Channel PD SOI MOSFETs," *Journal Integrated Circuits and Systems*, vol. 4, no. 2, pp. 61–66, 2009.

[276] Z. D. Prijić, S. S. Dimitrijev, and N. D. Stojadinović, "The determination of zero temperature coefficient point in CMOS transistors," *Microelectronics Reliability*, vol. 32, no. 6, pp. 769–773, 1992.

[277] T. H. Tan and A. K. Goel, "Zero-temperature-coefficient biasing point of a fully-depleted SOI MOSFET," *Microwave and Optical Technology Letters*, vol. 37, no. 5, pp. 366–370, 2003, ISSN: 1098-2760. DOI: 10.1002/mop.10920. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/mop.10920 (visited on 10/28/2020).

[278] L. M. Camillo, J. A. Martino, E. Simoen, and C. Claeys, "The temperature mobility degradation influence on the zero temperature coefficient of partially and fully depleted SOI MOSFETs," *Microelectronics Journal*, vol. 37, no. 9, pp. 952–957, Sep. 1, 2006, ISSN: 0026-2692. DOI: 10.1016/j.mejo.2006.01.008. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026269206000206 (visited on 10/28/2020).

[279] S. Abe, Y. Miyazawa, Y. Nakajima, T. Hanajiri, T. Toyabe, and T. Sugano, "Suppression of DIBL in deca-nano SOI MOSFETs by controlling permittivity and thickness of BOX layers," in *2009 10th International Conference on Ultimate Integration of Silicon*, Mar. 2009, pp. 329–332. DOI: 10.1109/ULIS.2009.4897602.

[280] M. J. Kumar and M. Siva, "The Ground Plane in Buried Oxide for Controlling Short-Channel Effects in Nanoscale SOI MOSFETs," *IEEE Transactions on Electron Devices*, vol. 55, no. 6, pp. 1554–1557, Jun. 2008, ISSN: 1557-9646. DOI: 10.1109/TED.2008.922859.

[281] N. Othman, M. K. M. Arshad, and U. Hashim, "Lower DIBL in inverted substrate of UTBB SOI n-MOSFETs," in *2014 IEEE International Conference on Semiconductor Electronics (ICSE2014)*, Aug. 2014, pp. 76–79. DOI: 10.1109/SMELEC.2014.6920799.

[282] K. K. Young, "Short-channel effect in fully depleted SOI MOSFETs," *IEEE Transactions on Electron Devices*, vol. 36, no. 2, pp. 399–402, Feb. 1989, ISSN: 1557-9646. DOI: 10.1109/16.19942.

[283] E. J. Nowak, "Maintaining the benefits of CMOS scaling when scaling bogs down," *IBM Journal of Research and Development*, vol. 46, no. 2.3, pp. 169–180, 2002.

[284] W. Haensch, E. J. Nowak, R. H. Dennard, *et al.*, "Silicon CMOS devices beyond scaling," *IBM Journal of Research and Development*, vol. 50, no. 4.5, pp. 339–361, 2006.

[285] M. Asheghi, M. N. Touzelbaev, K. E. Goodson, Y. K. Leung, and S. S. Wong, "Temperature-dependent thermal conductivity of single-crystal silicon layers in SOI substrates," 1998.

[286] W. Liu, K. Etessam-Yazdani, R. Hussin, and M. Asheghi, "Modeling and data for thermal conductivity of ultrathin single-crystal SOI layers at high temperature," *IEEE Transactions on Electron Devices*, vol. 53, no. 8, pp. 1868–1876, 2006.

[287] W. Liu and M. Asheghi, "Phonon–boundary scattering in ultrathin single-crystal silicon layers," *Applied Physics Letters*, vol. 84, no. 19, pp. 3819–3821, Apr. 29, 2004, ISSN: 0003-6951. DOI: 10.1063/1.1741039. [Online]. Available: https://aip.scitation.org/doi/10.1063/1.1741039 (visited on 11/04/2020).

[288] M. G. Holland, "Analysis of lattice thermal conductivity," *Physical review*, vol. 132, no. 6, p. 2461, 1963.

[289] E. H. Sondheimer, "Electrical transport in metallic films," *Adv. Phys*, vol. 1, pp. 1–143, 1952.

[290] E. H. Sondheimer, "The mean free path of electrons in metals," *Advances in physics*, vol. 50, no. 6, pp. 499–537, 2001.

[291] D. G. Cahill, W. K. Ford, K. E. Goodson, *et al.*, "Nanoscale thermal transport," *Journal of applied physics*, vol. 93, no. 2, pp. 793–818, 2003.

[292] S. Inoue, H. Ohshima, and T. Shimoda, "Analysis of Degradation Phenomenon Caused by Self-Heating in Low-Temperature-Processed Polycrystalline Silicon Thin Film Transistors," *Japanese Journal of Applied Physics*, vol. 41, p. 6313, 11R Nov. 2002, ISSN: 1347-4065. DOI: 10.1143/JJAP.41.6313. [Online]. Available: https://iopscience.iop.org/article/10.1143/JJAP.41.6313/meta (visited on 07/29/2020).

[293] S.-W. Lee, Y.-J. Kim, S.-J. Park, *et al.*, "Dependence of Self-heating Effect on Width/Length Dimension in p-type Polycrystalline Silicon Thin Film Transistors," *Korea Information Display Society*, pp. 505–508, 2006. [Online]. Available: http://www.koreascience.or.kr/article/CFKO200624282632605.view (visited on 07/29/2020).

[294] T.-Y. Hsieh, T.-C. Chang, T.-C. Chen, *et al.*, "Self-Heating-Effect-Induced Degradation Behaviors in a-InGaZnO Thin-Film Transistors," *IEEE Electron Device Letters*, vol. 34, no. 1, pp. 63–65, Jan. 2013, ISSN: 1558-0563. DOI: 10.1109/LED.2012.2223654.

[295] L. Cai, W. Chen, G. Du, X. Zhang, and X. Liu, "Layout Design Correlated With Self-Heating Effect in Stacked Nanosheet Transistors," *IEEE Transactions on Electron Devices*, vol. 65, no. 6, pp. 2647–2653, Jun. 2018, ISSN: 1557-9646. DOI: 10.1109/TED.2018.2825498.

[296] H.-S. Kim, K. Park, H. Oh, and E. S. Jung, "Effective Gate Layout Methods for RF Performance Enhancement in MOSFETs," *IEEE Electron Device Letters*, vol. 30, no. 10, pp. 1105–1107, Oct. 2009, ISSN: 1558-0563. DOI: 10.1109/LED.2009.2029128.

[297] B. E. Deal, M. Sklar, A. S. Grove, and E. H. Snow, "Characteristics of the surface-state charge (Qss) of thermally oxidized silicon," *Journal of the Electrochemical Society*, vol. 114, no. 3, p. 266, 1967.

[298] S. Mahapatra, K. Joshi, S. Mukhopadhyay, A. Chaudhary, and N. Goel, "Physical mechanism of BTI degradation—Modeling of process and material dependence," in *Fundamentals of Bias Temperature Instability in MOS Transistors*, Springer, 2016, pp. 127–179.

[299] A. A. Katsetos, "Negative bias temperature instability (NBTI) recovery with bake," *Microelectronics Reliability*, vol. 48, no. 10, pp. 1655–1659, 2008.

[300] R. W. Herfst, P. G. Steeneken, M. P. Tiggelman, J. Stulemeijer, and J. Schmitz, "Fast RF-CV characterization through high-speed 1-port S-parameter measurements," *IEEE transactions on semiconductor manufacturing*, vol. 25, no. 3, pp. 310–316, 2012.

[301] D. Angot, V. Huard, X. Federspiel, F. Cacho, and A. Bravaix, "Bias temperature instability and hot carrier circuit ageing simulations specificities in UTBB FDSOI 28nm node," in *2013 IEEE International Reliability Physics Symposium (IRPS)*, Apr. 2013, pp. 5D.2.1–5D.2.5. DOI: 10.1109/IRPS.2013.6532037.

[302] S. Pae, M. Agostinelli, M. Brazier, *et al.*, "BTI reliability of 45 nm high-K+ metal-gate process technology," in *2008 IEEE International Reliability Physics Symposium*, IEEE, 2008, pp. 352–357.

[303] H. Reisinger, U. Brunner, W. Heinrigs, W. Gustin, and C. Schlunder, "A comparison of fast methods for measuring NBTI degradation," *IEEE Transactions on Device and Materials Reliability*, vol. 7, no. 4, pp. 531–539, 2007.

[304] D. P. Ioannou, Y. Tan, R. Logan, *et al.*, "Hot carrier effects on the RF performance degradation of nanoscale LNA SOI nFETs," in *2018 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2018, P–TX.2–1–P–TX.2–3. DOI: 10.1109/IRPS.2018.8353697.

[305] R. W. Herfst, J. Schmitz, and A. J. Scholten, "Simultaneous extraction of threshold voltage and mobility degradation from on-the-fly NBTI measurements," in *2011 International Reliability Physics Symposium*, Apr. 2011, XT.6.1–XT.6.4. DOI: 10.1109/IRPS.2011.5784607.

[306] S. Rangan, N. Mielke, and E. C. Yeh, "Universal recovery behavior of negative bias temperature instability [PMOSFETs]," in *IEEE International Electron Devices Meeting 2003*, IEEE, 2003, pp. 14–3.

[307] V. D. Maheta, E. N. Kumar, S. Purawat, C. Olsen, K. Ahmed, and S. Mahapatra, "Development of an Ultrafast On-the-Fly IDLIN Technique to Study NBTI in Plasma and Thermal Oxynitride p-MOSFETs," *IEEE Transactions on Electron Devices*, vol. 55, no. 10, pp. 2614–2622, 2008.

[308] N. Parihar, N. Goel, S. Mukhopadhyay, and S. Mahapatra, "BTI Analysis Tool—Modeling of NBTI DC, AC Stress and Recovery Time Kinetics, Nitrogen Impact, and EOL Estimation," *IEEE Transactions on Electron Devices*, vol. 65, no. 2, pp. 392–403, Feb. 2018, ISSN: 1557-9646. DOI: 10.1109/TED.2017.2780083.

[309] H. Reisinger, T. Grasser, K. Hofmann, W. Gustin, and C. Schlünder, "The impact of recovery on BTI reliability assessments," in *2010 IEEE International Integrated Reliability Workshop Final Report*, Oct. 2010, pp. 12–16. DOI: 10.1109/IIRW.2010.5706474.

[310] C. Yu and J. S. Yuan, "MOS RF reliability subject to dynamic voltage stress-modeling and analysis," *IEEE transactions on electron devices*, vol. 52, no. 8, pp. 1751–1758, 2005.

[311] L. Brunet, X. Garros, A. Bravaix, *et al.*, "Impact of backside interface on Hot Carriers degradation of thin film FDSOI Nmosfets," in *2012 IEEE International Reliability Physics Symposium (IRPS)*, Apr. 2012, 3B.2.1–3B.2.5. DOI: 10.1109/IRPS.2012.6241806.

[312] X. Federspiel, M. Rafik, D. Angot, F. Cacho, and D. Roy, "Interaction between BTI and HCI degradation in High-K devices," in *2013 IEEE International Reliability Physics Symposium (IRPS)*, Apr. 2013, XT.9.1–XT.9.4. DOI: 10.1109/IRPS.2013.6532124.

[313] C. H. Ling, S. E. Tan, and D. S. Ang, "A study of hot carrier degradation in NMOSEET's by gate capacitance and charge pumping current," *IEEE transactions on electron devices*, vol. 42, no. 7, pp. 1321–1328, 1995.

[314] Y. T. Yeow, C. H. Ling, and L. K. Ah, "Observation of MOSFET degradation due to electrical stressing through gate-to-source and gate-to-drain capacitance measurement," *IEEE electron device letters*, vol. 12, no. 7, pp. 366–368, 1991.

[315] S. Mittl and F. Guarín, "Self-heating and its implications on hot carrier reliability evaluations," in *2015 IEEE International Reliability Physics Symposium*, Apr. 2015, 4A.4.1–4A.4.6. DOI: 10.1109/IRPS.2015.7112726.

[316] T. Chen, C. Zhang, W. Arfaoui, *et al.*, "Excellent 22FDX Hot-Carrier Reliability for PA Applications," in *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Jun. 2019, pp. 27–30. DOI: 10.1109/RFIC.2019.8701760.

[317] J.-T. Park, B.-J. Lee, D.-W. Kim, C.-G. Yu, and H.-K. Yu, "RF performance degradation in nMOS transistors due to hot carrier effects," *IEEE Transactions on Electron Devices*, vol. 47, no. 5, pp. 1068–1072, 2000.

[318] G. T. Sasse, R. J. de Vries, and J. Schmitz, "Methodology for performing RF reliability experiments on a generic test structure," in *2007 IEEE International Conference on Microelectronic Test Structures*, IEEE, 2007, pp. 177–182.

[319] C. D. Presti, F. Carrara, A. Scuderi, S. Lombardo, and G. Palmisano, "Degradation mechanisms in CMOS power amplifiers subject to radio-frequency stress and comparison to the DC case," in *2007 IEEE International Reliability Physics Symposium Proceedings. 45th Annual*, IEEE, 2007, pp. 86–92.

[320] M. Jo, S. Kim, C. Cho, M. Chang, and H. Hwang, "Gate voltage dependence on hot carrier degradation at an elevated temperature in a device with ultrathin silicon oxynitride," *Applied Physics Letters*, vol. 94, no. 5, p. 053 505, 2009.

[321] T. Aichinger, M. Nelhiebel, and T. Grasser, "Unambiguous identification of the NBTI recovery mechanism using ultra-fast temperature changes," in *2009 IEEE International Reliability Physics Symposium*, Apr. 2009, pp. 2–7. DOI: 10.1109/IRPS.2009.5173216.

[322] H. Wong, Y. Fu, J. J. Liou, and Y. Yue, "Hot-carrier reliability and breakdown characteristics of multi-finger RF MOS transistors," *Microelectronics Reliability*, vol. 49, no. 1, pp. 13–16, 2009.

[323] A. Burenkov, V. Belko, and J. Lorenz, "Self-heating of nano-scale SOI MOSFETs: TCAD and molecular dynamics simulations," in *19th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, Sep. 2013, pp. 305–308. DOI: 10.1109/THERMINIC.2013.6675230.

[324] J. R. Srour, "Basic mechanisms of radiation effects on electronic materials, devices, and integrated circuits," NORTHROP RESEARCH AND TECHNOLOGY CENTERPALOS VERDES PENINSULA CA, 1982.

[325] P. Heremans, J. Witters, G. Groeseneken, and H. E. Maes, "Analysis of the charge pumping technique and its application for the evaluation of MOSFET degradation," *IEEE transactions on Electron Devices*, vol. 36, no. 7, pp. 1318–1335, 1989.

[326] A. Benabdelmoumene, B. Djezzar, A. Chenouf, H. Tahi, B. Zatout, and M. Kechouane, "On the turn-around phenomenon in n-MOS transistors under NBTI conditions," *Solid-State Electronics*, vol. 121, pp. 34–40, 2016.

[327] S. Tyaginov, I. Starkov, O. Triebl, *et al.*, "Secondary generated holes as a crucial component for modeling of HC degradation in high-voltage n-MOSFET," in *2011 International Conference on Simulation of Semiconductor Processes and Devices*, IEEE, 2011, pp. 123–126.

[328] M. Houssa, M. Tuominen, M. Naili, *et al.*, "Trap-assisted tunneling in high permittivity gate dielectric stacks," *Journal of Applied Physics*, vol. 87, no. 12, pp. 8615–8620, 2000.

[329] E. Takeda and N. Suzuki, "An empirical model for device degradation due to hot-carrier injection," *IEEE electron device letters*, vol. 4, no. 4, pp. 111–113, 1983.

[330] C. Schlünder, S. Aresu, G. Georgakos, *et al.*, "HCI vs. BTI? - Neither one's out," in *2012 IEEE International Reliability Physics Symposium (IRPS)*, Apr. 2012, 2F.4.1–2F.4.6. DOI: 10.1109/IRPS.2012.6241797.

[331] C. Schlünder, H. Reisinger, S. Aresu, and W. Gustin, "On the PBTI degradation of pMOSFETs and its impact on IC lifetime," in *2011 IEEE International Integrated Reliability Workshop Final Report*, IEEE, 2011, pp. 7–11.

[332] C. Schlünder, R. Brederlow, P. Wieczorek, *et al.*, "Trapping mechanisms in negative bias temperature stressed p-MOSFETs," *Microelectronics Reliability*, vol. 39, no. 6-7, pp. 821–826, 1999.

[333] V. Reddy, A. T. Krishnan, A. Marshall, *et al.*, "Impact of negative bias temperature instability on digital circuit reliability," *Microelectronics Reliability*, vol. 45, no. 1, pp. 31–38, 2005.

[334] R. Thewes, R. Brederlow, C. Schlunder, *et al.*, "Evaluation of MOSFET reliability in analog applications," in *31st European Solid-State Device Research Conference*, IEEE, 2001, pp. 73–80.

[335] Y. Mitani, S. Fukatsu, D. Hagishima, and K. Matsuzawa, "Separation of NBTI component from channel hot carrier degradation in pMOSFETs focusing on recovery phenomenon," in *2011 IEEE International Conference on IC Design Technology*, May 2011, pp. 1–4. DOI: 10.1109/ICICDT.2011.5783215.

[336] J. Keane, X. Wang, D. Persaud, and C. H. Kim, "A high resolution on-chip beat frequency detection system for measuring BTI, HCI, and TDDB," in *2010 IEEE International Conference on Integrated Circuit Design and Technology*, Jun. 2010, pp. 142–145. DOI: 10.1109/ICICDT.2010.5510268.

[337] E. Maricau and G. Gielen, "Background on IC Reliability Simulation," in *Analog IC Reliability in Nanometer CMOS*, ser. Analog Circuits and Signal Processing, E. Maricau and G. Gielen, Eds., New York, NY: Springer, 2013, pp. 79–91, ISBN: 978-1-4614-6163-0. DOI: 10.1007/978-1-4614-6163-0_4. [Online]. Available: https://doi.org/10.1007/978-1-4614-6163-0_4 (visited on 11/15/2020).

[338] M. Jeng, C. Hsiao, K. Su, and C. Lin, "Circuit reliability simulation using TMI2," in *Proceedings of the IEEE 2013 Custom Integrated Circuits Conference*, Sep. 2013, pp. 1–7. DOI: 10.1109/CICC.2013.6658491.

[339] J. Schmitz, F. N. Cubaynes, R. J. Havens, R. De Kort, A. J. Scholten, and L. F. Tiemeijer, "RF capacitance-voltage characterization of MOSFETs with high leakage dielectrics," *IEEE electron device letters*, vol. 24, no. 1, pp. 37–39, 2003.

[340] A. Zaka, Q. Rafhay, M. Iellina, *et al.*, "On the accuracy of current TCAD hot carrier injection models in nanoscale devices," *Solid-State Electronics*, vol. 54, no. 12, pp. 1669–1674, Dec. 1, 2010, ISSN: 0038-1101. DOI: 10.1016/j.sse.2010.06.014. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0038110110002443 (visited on 11/16/2020).