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A 2TnC ferroelectric memory gain cell suitable for compute-in-memory and neuromorphic application

Stefan Slesazeck1, Taras Ravsher1, Viktor Havel1, Evelyn T. Breyer1, Halid Mulaosmanovic1, Thomas Mikolajick1,2
1NaMLab gGmbH, 01187 Dresden, Germany
2Technische Universität Dresden, Chair for Nano electronic Materials 01069 Dresden, Germany
stefan.slesazeck@namlab.com

Abstract—A 2TnC ferroelectric memory gain cell consisting of two transistors and two or more ferroelectric capacitors (FeCAP) is proposed. While a pre-charge transistor allows to access the single cell in an array, the read transistor amplifies the small read signals from small-scaled FeCAPs that can be operated either in FeRAM mode by sensing the polarization reversal current, or in ferroelectric tunnel junction (FTJ) mode by sensing the polarization dependent leakage current. The simultaneous read or write operation of multiple FeCAPs is used to realize compute-in-memory (CiM) algorithms that enable processing of data being represented by both, non-volatilely internally stored data and externally applied data. The internal gain of the cell mitigates the need for 3D integration of the FeCAPs, thus making the concept very attractive especially for embedded memories. Here we discuss design constraints of the 2TnC cell and present the proof-of-concept for realizing versatile (CiM) approaches by means of electrical characterization results.

I. INTRODUCTION
The vast amount of data processed in today’s electronic devices performing data search, classification and recognition, sensor signal processing and eventually machine learning facilitates a transition from the conventional compute centric to a more data centric paradigm. In contrast to the classical architectures where data is transferred between computing and memory units, giving rise to the well-known von-Neumann bottleneck [1], the CiM concepts target at repealing the approach of physical separation between computing and memory unit. Eventually, in neuro inspired architectures both logic and memory functionality become synergized together in one synaptic device. The ferroelectric materials based on HfO2 offer an attractive platform for the realization of non-volatile memory elements, being easily co-integrated together with state-of-the-art CMOS technologies, thus paving the way to collocate non-volatile memory and logic functionality in close vicinity on silicon. Two types of ferroelectric devices can be generally distinguished: two-terminal capacitors (FeCAP) and three-terminal transistors (i.e. ferroelectric field-effect transistors FeFETs). When the dielectric is very thin, the former can also be utilized as ferroelectric tunneling junctions (FTJ). However, while the integration of small-scaled FeFET devices was already demonstrated successfully [3][4], the comparatively low current density provided by FTJs [5][6][7] and limited amount of polarization switching charge offered by planar FeCAPs so far prevents their adoption in embedded memory arrays. Moreover, CiM operation based on FeFETs and FeCAPs has been demonstrated recently [8][9]. Though, utilization of FeCAP and FTJ devices for such approaches was not investigated so far in hardware. Recently a 2T1C ferroelectric memory cell was proposed, that enables the sensing of the small signals of scaled FeCAPs [10]. Building on these results, we present a 2TnC ferroelectric memory gain cell consisting of two transistors and two or more FeCAPs, offering the possibility for adoption of small-scaled planar ferroelectric 2-terminal devices and realization of versatile CiM concepts. Measurement were performed on test structures using FeFET-gates as FeCAP or FTJ, manufactured in the same technology as reported in [4][10].

II. BASIC OPERATION PRINCIPLE
Fig.1 depicts the schematic diagram and basic operation principle of the proposed 2TnC ferroelectric memory gain cell. Compared to a conventional FeRAM cell, that consists of a FeCAP and an access transistor TP, in the proposed cell the gate of an additional read transistor TR is connected to the internal storage node n1. In that way the effective capacitance of the sensing node (that is the BL in the conventional FeRAM architecture) can be greatly reduced and is mainly determined by the capacitance of the gate of TR, negligible drain capacitance of TP and the non-switching capacitance of the FeCAP itself. Thus, when TP is switched off during read operation, a small sized TR allows sensing tiny polarization dependent leakage currents flowing through the FeCAP in FTJ reading mode while applying a voltage between the plate line (PL) and the cell internal storage node n1, or sensing tiny polarization switching charges in conventional FeRAM mode by applying a read pulse to the respective PL. The polarization dependent voltage change \( \Delta V_{n1} \) at the internal node n1 can be sensed as drain current of TR by a sense amplifier (SA) being connected to the source line (SL). Thus, the original signal from the FeCAP is amplified via TR. The write operation is performed by turning on TP and applying the write voltage directly between BL and PL in either voltage polarity. Notably, in FeRAM mode the destructive readout requires a write-back operation to refresh the sensed data. That can be performed either by feeding back a writing voltage to the BL and switching on TP after a successful read operation or, by changing the cell structure as is depicted in Fig. 2 in a way, that read operation is performed directly using a SA connected to

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The rest of the text includes detailed analysis and discussion of the proposed 2TnC ferroelectric memory gain cell, including its performance, limitations, and potential applications in compute-in-memory and neuromorphic systems.
the BL. One drawback of the FeRAM operation mode is that the capacitive voltage divider ratio between $C_{\text{gate}_{\text{TR}}}$ and the FeCAP provokes a trade-off between read signal strength $\Delta V_{\text{NL}}$ and the required read pulse voltage amplitude $\Delta V_{\text{PL}}$ applied to PL and the voltage drop at the gate of TR during read operation, the latter one giving rise to a potential reliability issue (see Fig. 3). Those problems can be avoided in the FTJ operation mode, where increasing the ratio between $C_{\text{FTJ}}$ and $C_{\text{gate}_{\text{TR}}}$ increases the signal $\Delta V_{\text{NL}}$ without any other detrimental effect. Importantly, for large area FTJs the effective capacitance $C_{\text{NL}} = C_{\text{gate}_{\text{TR}}} + C_{\text{FTJ}} + C_{\text{drain}_{\text{TP}}}$ and the achievable read signal depend mainly on the non-switching capacitance $C_{\text{FTJ}}$ of the FTJ itself (see Fig. 4). Thus, assuming comparable current densities, the two-layer stack FTJ approach featuring a thin low-k tunneling oxide and a thicker high-k ferroelectric switching layer [7] yields a benefit due to lower capacitance when compared to the single-layer FTJ featuring only a very thin high-k ferroelectric switching layer [5]. In Table 1 we report the largest charging efficiency $\eta_{\text{FTJ}}$ defined as ratio of capacitance $C_{\text{FTJ}}$ and current density $j_{\text{FTJ}}$ for our FeFET-based FTJ compared to values extracted from literature.

### III. Compute in Memory Operation

As discussed above, it is evident that $\Delta V_{\text{NL}}$ is strongly influenced by the area of the active ferroelectric device. Thus, when two FeCAPs/FTJs are connected in parallel, one might expect the signal to change, depending on the polarization state of each individual device. Fig. 5a shows the result of such a measurement in a FeCAP mode. A clear separation between current levels corresponding to a different number of cells that were set into the programmed state is observed. This allows to realize either an AND or an OR logic gate, by setting a current threshold $I_{\text{th}}$ between the respective levels via the SA. Similar results are obtained when the cell is operated in FTJ mode (Fig. 5b). However, in this case, the signal level of the logic “1” state is located below the corresponding value for the logic “0” state. Furthermore, in FeRAM operation mode, the result of a logic operation can be directly stored inside a neighboring FeCAP (e.g. a third FeCAP as indicated in Fig. 6) during the logic operation itself. This is done by applying a negative bias to PL of FeCAP C that was set to “0” state before, such that the bias alone is not sufficient to switch its polarization. However, when the result of a logic operation is “1” the potential $V_{\text{NL}}$ is increased, thus increasing the voltage drop across the FeCAP device C and writing “1” into it only in this case. In addition to using internally stored values as operands for logic gates it is also possible to perform logic operations with external input. In case of a FeRAM operation mode, this is done by controlling the switching voltage applied to each PL as depicted in Fig. 7. It is clear that when $\Delta V_{\text{PL}}$ represents “0” than the output will always be “0”. On the other hand, if $\Delta V_{\text{PL}}$ represents a “1”, the value stored in the device will be outputted, thus performing the AND logic operation between external input and internally stored value.

### IV. Reconfigurable Operation Mode

The signal obtained during the read operation is highly dependent on the pre-charge voltage $V_{\text{PC}}$, which determines the operating point of TR. Hence, $V_{\text{PC}}$ can be used as an extra degree of freedom when implementing CiM operations. Suppose that the current threshold $I_{\text{th}}$ is set such that at a given $V_{\text{PC}}$ a logic AND operation is performed (Fig. 8a). Then, by increasing the value of $V_{\text{PC}}$ it is possible to shift all current levels upwards so that a logic OR gate is obtained. The same concept for the FTJ mode is demonstrated in Fig. 8b. However, because FTJ current levels are inverted with respect to the FeRAM mode, logic NAND and NOR operations are performed. This way, a reconfigurable AND/OR/NAND/NOR gate is realized, which can dynamically change the output of computation depending on the pulsing scheme applied, while keeping the peripheral circuitry unchanged ($I_{\text{th}}$ is the same for all cases). However, the realization of different pre-charge voltage levels might increase the complexity of external circuits. A better way to implement reconfigurable CiM operation is to store a control bit inside the memory cell, determining the operation to be performed. For example, in FeRAM mode by connecting all three devices during the read operation, if “1” is stored inside the control bit (device C) then the current levels will shift as compared to the case when control bit is “0”. This is analogous to the role of $V_{\text{PC}}$ change described above. Similar re-configurable CiM functionality can be achieved by the value of the control bit only, without the need to change $V_{\text{PC}}$, $\Delta V_{\text{PL}}$ or current threshold $I_{\text{th}}$ as is shown in Fig. 9a and 9b for FeRAM and FTJ mode, respectively. This, combined with the fact that the result of a logic operation can be directly stored in the neighboring cell (e.g. to be used as a control bit for the next operation) offers great flexibility in designing in-memory computing systems and novel dynamically reconfigurable computing architectures. The gradual [11] and accumulative [12] switching capability is revealed for both FTJ and FeRAM mode in Fig. 10. Those features are especially interesting for analog weight updates and inference in neuromorphic applications.

### V. Summary

A 2TnC ferroelectric memory gain cell and its adoption for ultra-low-power NVM, CiM and neuromorphic applications based on 2D integrated ferroelectric capacitors is demonstrated.

### ACKNOWLEDGMENT

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### REFERENCES

Figure 1: a) schematic diagram of a 2TnC ferroelectric memory cell with fixed source potential of the read transistor TR; TP is the access transistor allowing single cell access in an array; b) basic operation scheme in FTJ mode while sensing the polarization dependent leakage current.

Figure 2: a) schematic diagram of another 2TnC ferroelectric memory cell with shared BL connection; b) basic operation scheme in FeRAM mode including one possibility to realize the write back operation after readout.

Figure 3: a) measured SL current during sensing operation in FeRAM mode for different capacitor areas in programmed (red) or erased (blue) state and b) voltage drop across the FeCAP, Gate of TR and extracted voltage signal \( \Delta V_{n1} \) for a read pulse of 4V, 1\( \mu \)s.

Figure 4: a) measured SL current in FTJ readout mode and b) extracted \( \Delta V_{n1} \) after 100\( \mu \)s from (a) plotted over the area ratio between the gate area of TR and the FTJ area (red dots) and modeled \( \Delta V_{n1} \) (lines). Different FTJ devices from literature are compared.

Table 1. FTJ parameters used for calculation of the data shown in Fig.4b.

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Figure 5: a) measured SL current during sensing operation in FeRAM mode. AND / OR operation of two internally stored bits in CA and CB of Fig. 2 was performed. The corresponding ID-VG-characteristic of the read out transistor TR indicates the relation between SL current and voltage \( V_{n1} \) of internal storage node n1; b) measured SL current during sensing operation in FTJ mode while performing NAND / NOR operation of two internally stored bits in CA and CB of Fig. 2.
Figure. 8: Realization of reconfigurable logic gates using pre-charge voltage $V_{pc}$ to select the desired logic operation. When operated in FeCAP mode logic AND / OR operations and NAND / NOR in FTJ mode are demonstrated, controlled by the value of $V_{pc}$. The inset shows that when applying $V_{pc} = 0V$ no write operation to capacitor CC is performed.

Figure. 6: a) 2TnC ferroelectric memory gain cell with at least 3 FeCAPs. The result of the logic AND / OR operation of stored bits in capacitor CA and CB can be written directly into capacitor CC; b) measured SL current after AND / OR operation in FeRAM mode and c) resulting SL current when reading the capacitor CC in FeRAM mode after AND / OR operation of (b) while keeping the bias voltage $V_{bias}$ at -0.8V. The inset shows that when applying $V_{bias} = 0V$ no write operation to capacitor CC is performed.

Figure. 7: a) definition of logic values for performing logic operations between internally stored data bits (d1 and d3) that are represented by the polarization state of the two individual FeCAPs (logic ‘0’ for erased state and logic ‘1’ for programmed state) and externally applied data bits (d2 and d4) that are represented by the applied read pulse amplitude where $\Delta V_{PL} = 4V$ represents logic ‘1’ and $\Delta V_{PL} = 0V$ represents logic ‘0’; b) measurement results for compute-in-memory algorithm according to the equation: (d1 and d2) or (d3 and d4).

Figure. 8: Realization of reconfigurable logic gates using pre-charge voltage $V_{pc}$ to select the desired logic operation. When operated in FeCAP mode logic AND / OR operations and NAND / NOR in FTJ mode are demonstrated, controlled by the value of $V_{pc}$.

Figure. 9: Reconfigurable logic gates realized by controlling the operation to be performed by the value stored in the neighboring FeCAP device CC, referred to as the control bit. Depending on its state, the signals for each level will be either shifted or not, thus allowing to choose the logic operation.

Figure. 10: Measured voltage $V_{n1}$ for gradual polarization switching by applying program pulses of 10 µs duration for increasing program voltages $\Delta V_{PL}$ in a) FeRAM read mode and b) FTJ read mode.