Dieses Dokument ist eine Zweitveröffentlichung (Postprint) /

This is a self-archiving document (accepted version):

Stefan Slesazeck, Viktor Havel, Evelyn Breyer, Halid Mulaosmanovic, Michael Hoffmann, Benjamin Max, Stefan Duenkel, Thomas Mikolajick

Uniting The Trinity of Ferroelectric HfO₂ Memory Devices in a Single Memory Cell

Erstveröffentlichung in / First published in:

IEEE 11th International Memory Workshop (IMW). Monterey, 2019. IEEE. ISBN 978-1-7281-0981-7

DOI: <https://doi.org/10.1109/IMW.2019.8739742>

Diese Version ist verfügbar / This version is available on:

<https://nbn-resolving.org/urn:nbn:de:bsz:14-qucosa2-776856>

Uniting The Trinity of Ferroelectric HfO₂ Memory Devices in a Single Memory Cell

Stefan Slesazek¹, Viktor Havel¹, Evelyn Breyer¹, Halid Mulaosmanovic¹,
Michael Hoffmann¹, Benjamin Max², Stefan Duenkel³ and Thomas Mikolajick^{1,2}

¹NaMLab gGmbH, 01187 Dresden, Germany

²Technische Universität Dresden, Chair for Nanoelectronic Materials 01069 Dresden, Germany

³GLOBALFOUNDRIES Fab1 LLC & Co. KG, Dresden, Germany

stefan.slesazek@namlab.com

Abstract—The polarization reversal in ferroelectric HfO₂ is adopted to store information in three distinct device classes – ferroelectric field effect transistors (FeFET), ferroelectric capacitors (FeCAP) and ferroelectric tunnel junctions (FTJ). Common to all three concepts is the adoption of a ferroelectric layer stack that acts either as gate dielectric in the FeFET or as the capacitor dielectric and tunneling barrier in the FeCAP or FTJ, respectively. A composite structure including an inevitably or purposefully formed dielectric layer is frequently adopted. In this work we report on the co-existence of all three memory concepts within one device structure and propose a 2T1C ferroelectric memory cell that allows the operation and comparative characterization of the trinity of ferroelectric memory devices.

Keywords: *Ferroelectric Memory; FeRAM, FeFET; FTJ;*

I. INTRODUCTION

Ferroelectric (FE) materials based on HfO₂ offer an attractive platform for the realization of nonvolatile memory (NVM) elements. The electrically switchable ferroelectric polarization and its stability in time represent the main assets in this regard. Depending on the element structure, two types of devices can be generally distinguished: two-terminal capacitor and three-terminal transistor devices (i.e. ferroelectric field-effect transistors FeFETs). However, not only the structure, but also the effective device operation, which includes write and sensing functions, largely vary among and within the two types and are ground for further device subdivisions. For instance, the capacitor structures can be operated as capacitive elements - ferroelectric random access memory (FeRAM), but also as resistive elements - ferroelectric tunnel junctions (FTJs). The common feature of all of them is the stored polarization. This means that properties such as the polarization switching dynamics, switching reliability issues and polarization stability (retention), are shared to a large extent by the abovementioned devices. However, while the programming operation during the writing process is similar for all three device types – applying a positive or negative voltage pulse to induce polarization switching of the ferroelectric material, the read operation is unique for each memory concept and a main differentiator demanding different device optimization. In this work we review the three different ferroelectric memory devices and optimization targets, considering the fact that the transition between the three different devices is linked to the thickness of the dielectric layer in the metal-ferroelectric-insulator-semiconductor (metal) structures. Moreover, we will demonstrate, that all three different operation principles can be

observed within one ferroelectric device. Finally, we present a memory cell structure that can be reversibly reconfigured to operate as one of the three structures in order to conveniently study and benchmark the device properties thus enabling the comparative study of the different device operation schemes using the exact same ferroelectric film.

II. THE TRINITY OF FERROELECTRIC MEMORY DEVICES AND TYPICAL MEMORY CELL STRUCTURES

A. Ferroelectric capacitor FeCAP and FeRAM cell

Ferroelectric capacitors generally consist of a ferroelectric layer sandwiched between two conductive electrodes. By applying voltage pulses to the electrodes, the polarization is switched into one of the two states, which are supposed to be maintained in a nonvolatile manner. In the typical FeRAM memory cell that is depicted schematically in Fig. 1a) the polarization state of the ferroelectric layer is determined by sensing the displacement current of the ferroelectric capacitor C1 resulting from the polarization reversal during switching operation upon application of an electrical switching pulse at the plate line (PL). Such a destructive read operation not only means it might be necessary to re-write the sensed state, but also poses severe constraints for cycling endurance of the adopted ferroelectric material. The polarization switching charge is transferred via a select transistor T1 to the bit line (BL). The resulting voltage signal is determined by a voltage sense amplifier being connected to the respective bit line. Several memory cells share one sense amplifier. In order to yield a sufficient voltage signal the switched charge of every memory cell capacitor must be large enough to charge the bit line voltage to a level that can be reliably detected by the sense amp. Therefore, for highly scaled CMOS based technologies with a typical number of 128 or 256 cells that are connected to one bit line a 3D integration of the capacitor is mandatory to realize the large total switched charge, even though the area requirements might be relaxed compared to the DRAM case due to a higher charge density in the ferroelectric layer [1].

B. Ferroelectric Tunnel Junction - FTJ

The FTJ - when considered as a special case of the ferroelectric capacitor - could be operated in the FeRAM cell where write operation is performed in a similar way as for the ferroelectric capacitor. However, in contrast to the FeRAM concept FTJs

Figure 1. Ferroelectric memory cells: a) FeRAM cell, b) FeFET cell, and c) FeMFET cell

rely on the tunneling electroresistance ratio (TER), where the resistance of the FTJ strongly depends upon the orientation of the stored electric polarization within the structure. That is, instead of sensing the polarization switching charge upon polarization reversal the static current flowing through the FTJ might be directly transferred to the bit line to be sensed by a sense amplifier. However, while the sensing operation is tailored in a way not to disturb the stored state (nondestructive read), the resulting currents in the range of 10^{-13} to 10^{-10} A for scaled devices in the sub 100 nm regime [2]-[4] are very small and result in a very long sensing time at an unacceptable signal to noise ratio. Therefore, to operate the FTJ in a similar way as the FeRAM an increase of the current density by several orders of magnitude would be mandatory by optimization of the stack and/or adoption of additional sensing schemes. To enable sufficient tunneling current, the ferroelectric layer thickness would have to be somewhere in the range below 2nm [5]. However, for such small thicknesses the ferroelectric properties of the FE layer typically degrade and retention will be reduced [5][6]. Therefore, an additional dielectric layer can be introduced in the stack to decouple the ferroelectric thickness from the magnitude of the sensing current. In this concept the dielectric layer serves as the tunneling barrier while the ferroelectric layer serves as the memory layer [3].

C. Ferroelectric Field Effect Transistor - FeFET

FeFETs resemble conventional MOSFET transistors that have a ferroelectric material in the gate stack. In this way, the conductivity of the transistor channel can be readily modulated by the stored polarization charge, which is used to distinguish between two or more logic states. Moreover, the field-effect in FeFETs results in orders-of-magnitude separation between the conductivity states. The schematic diagram of the typical FeFET memory cell is depicted in Fig. 1b) where the circuit element T2 represents the FeFET device. The gate of the transistor T2 is directly connected to a word line (WL). In this concept the polarization state of the ferroelectric layer is determined by sensing the threshold voltage of the transistor by either charging or discharging a bit line that is connected to one S/D terminal of the FeFET and determining the voltage change after a certain sensing time using a voltage sense amplifier or by directly sensing the current flow through the FeFET by adoption of a current sense amplifier at either the source line (SL) or bit line (BL). The polarization state of the FeFET is maintained during read operation. Therefore, it is a non-destructive read operation that represents an important advantage for these devices. The benefit of the FeFET memory

device compared to the FeRAM memory cell is the nondestructive read, its easy integration into state-of-the-art CMOS processes [7] and no 3D capacitor structure has to be realized in the back-end-of-line (BEOL) process. However, FeFET memory devices have the disadvantage of lower cycling endurance compared to FeRAM capacitor devices that is typically limited to $10^5 - 10^7$ cycles [1]. The reason behind is the degradation of the interfacial silicon dioxide layer with a thickness in the range of 1nm that is sandwiched between the silicon channel and the ferroelectric high-k hafnium/zirconium oxide layer. This silicon oxide interface is formed during processing of the devices and preserves a sufficient electron mobility in the channel. The relatively high coercive field for polarization reversal of the HfO_2 -based ferroelectric layer in the range of 1 MV/cm and the relation between the relative permittivity of the silicon oxide interface (about 3.8 or up to 7 for nitrided interfaces) and the ferroelectric hafnium oxide (about 30) yields an electric field peak in the range of 10 MV/cm over the interfacial silicon oxide layer during polarization switching. That value is close to the break down field of the interfacial oxide layer. Therefore, repeatedly switching of the FeFET device results in a wear out of the interfacial silicon oxide layer, leading to an increase of charge trapping and eventually to the closure of the memory window.

D. Ferroelectric-Metal Field Effect Transistor (FeMFET)

In order to combine the benefits of high cycling endurance of a ferroelectric metal-insulator-metal capacitor that has no interfacial oxide and thus exhibits an improved reliability on the one hand, and the smaller cell size as well as lower manufacturing complexity of a FeFET device on the other hand, a planar metal-ferroelectric-metal capacitor C1 can be directly connected in between the gate electrode of a read transistor T3 and the word line terminal as is shown schematically in Fig. 1c). This concept is also referred to as the ferroelectric-metal field effect transistor (FeMFET) [8]. In that way a combined FeFET memory cell can be realized that is operated in a similar way as the conventional FeFET cell. However, the electrical node n1 is a floating node that has no direct connection to ground. Due to inevitable leakage currents that might flow through the gate dielectric of the transistor T3 and through the ferroelectric capacitor C1 the voltage at node n1 might change over time. Moreover, even under zero applied electric bias between the WL and SL/BL terminals of the memory cell, the polarization state of the ferroelectric capacitor C1 might lead to a non-zero electric potential at node n1 that results in an electrical field drop at the gate of the transistor T3 and at the ferroelectric capacitor C1. The electric field in turn induces a leakage current I_{LEAK} that eventually charges the floating node n1, thus resulting in a change of the effective gate potential of T3 and eventually leading to a loss of the stored information.

III. A 2T1C COMBINED FERROELECTRIC MEMORY CELL

The described limitations resulting from the inevitable leakage currents in the FeMFET could be circumvented by introducing an additional circuit element in the memory cell such as a transistor, resistor, diode or the like that allows the direct control of the potential of the otherwise floating node n1.

Here we propose a 2T1C ferroelectric memory cell where an additional select transistor T1 is connected to node n1 as is depicted in Fig. 2a). In that cell configuration node n1 can be directly connected to the bit line via T1. Write operation is performed like in the FeRAM cell by turning on T1 and applying the write voltage between BL and PL directly to the terminals of C1. In contrast to the FeMFET cell the write voltage becomes independent of the capacitive voltage divider ratio between the gate of read transistor T3 and the ferroelectric capacitor C1, thus being determined by the coercive voltage of the capacitor C1 only which leads to a lower write voltage. Moreover, prior to a destructive read operation to be performed in a similar way as in the FeRAM cell the potential of n1 can be set to a predefined value, thus eliminating the problem of data loss due to accumulated leakage current at node n1 during retention. Note, that the effective capacitance of node n1 is mainly determined by the sum of the gate capacitance of T3 and the dielectric background capacitance of C1, whereby the capacitance ratio between the gate of T3 and C1 determines the voltage change upon polarization reversal of C1. Thus, compared to the standard FeRAM cell array with typical BL capacitances in the range of several 10fF, in the proposed 2T1C cell with an effective capacitance in the sub-fF range at node n1 already a much smaller ferroelectric polarization charge will generate a suitable sensing signal in terms of the resulting drain current of read transistor T3 to be measured at the SL. The voltage of node n1 can be further adjusted via the BL and select transistor T1 by a pre-charge operation that is performed prior to the PL read pulse. In that way the operation point of T3 can be adjusted in a large range between sub-threshold and linear regime to adjust it according to the requirements of the interfacing sensing circuitry. Due to the high sensitivity of the 2T1C cell even a very small sensing current in the sub-nA range as is provided by a typical FTJ might be sufficient to alter the voltage of n1 in a sub- μ s time frame. In this operation scheme the polarization state of the ferroelectric capacitor C1 is determined by accumulating the charge that is flowing through C1 upon application of a suitable dc-bias between pre-charged n1 and PL on the gate capacitance of T3, thus giving rise to a polarization state dependent gate voltage change at T3. By connecting more than one storage capacitors to node n1 with each having an individual plate line PL connected to it the memory density might be increased. Such concept allows to access multiple capacitors simultaneously. Besides multi-bit operation also logic operation between the multiple stored bits could be performed already inside the memory cell.

Figure 2. 2T1C Ferroelectric memory cell: a) realization with ferroelectric capacitor and b) test structure realization using a FeFET

IV. EXPERIMENTAL

A. Test structure design and device fabrication

Fig. 2b) depicts the circuit schematic of the 2T1C ferroelectric memory cell where the capacitor C1 of Fig. 2a) is realized by the gate capacitor of a FeFET device. The gate of the FeFET T4 is connected to the node n1 while source / bulk terminal and drain terminal are connected to individual pads PL1 and PL2, together representing the PL of the 2T1C memory cell. Thus, the polarization state can be characterized by measuring the I_D - V_G characteristic of T4. For example, connecting the gate of T4 via T1 to the BL, the gate voltage can be swept while the drain /source current is measured between the terminals PL1 and PL2. Similarly, the I_D - V_G characteristic of T3 can be characterized while applying a suitable drain voltage to the SL terminal. The test structure of Fig. 2b) was manufactured in a 28 nm HKMG technology with the FeFET being realized by adopting an 8 nm thick Si-doped HfO_2 . The thickness of the interfacial silicon oxide is about 1.2 nm [7]. The size of the FeFET device T4 was chosen to be 450 nm/450 nm. T1 (W/L = 320 nm/590 nm) and T3 (W/L = 2700 nm/590 nm) are thick oxide I/O devices that allow the application of operation voltages up to 4V.

B. Electrical measurement results

Fig. 3a) schematically depicts the operation scheme of the 2T1C ferroelectric memory cell of Fig. 2b), where the gate of the FeFET transistor is connected to the BL via T1. Under that condition the FeFET T4 can be programmed/erased by applying write voltage pulses to the BL ($V_{PR} = [2V \dots 4V]$) or PL1/PL2 ($V_{ER} = 4V$), respectively, that exceed the coercive voltage of the FeFET being in the range of 3V. The measured I_D - V_G curves of the FeFET that are depicted in Fig. 3d) reveal a maximum memory window of 0.5V, which is defined as the threshold voltage difference between the erased (blue curves) and the programmed (red curves) state. By successively increasing the program pulse voltage (depicted as green arrow in Fig. 3a) the threshold voltage of the programmed state decreases successively. Upon a finer program voltage excitation, this behavior might be exploited for multi-level operation [9]. In Fig. 3b) the FeRAM-like operation scheme of the 2T1C ferroelectric memory cell is shown schematically. In this case PL1 and PL2 are always connected together as plate line and the FeFET device is used like a ferroelectric capacitor. Program and erase operation are performed in a similar way as is shown for the FeFET case. However, for the read operation in a first step the node n1 is pre-charged via the bit line and T1 to a potential that sets the read transistor T3 in a suitable operation point, for example in the sub-threshold region (in this case to 0V). After the pre-charge operation T1 is turned off by setting the WL voltage back to 0 V so that n1 is floating. Subsequently an erase pulse is applied to the PL1/PL2 terminals. In the case the FeFET was already erased no polarization reversal occurs and the potential at n1 stays roughly constant. Therefore the measured current post read pulse nearly equals the current at pre-charge state (blue curves). However, in the case the FeFET stores the programmed state, the read operation induces a polarization reversal. The resulting switching current increases the potential at n1. Thus, depending on the memorized

Figure 3. Operation scheme of the 2T1C ferroelectric memory cell using a FeFET as ferroelectric capacitor as shown in Fig. 2b and electrical characterization results for FeFET (T4) readout scheme in a) and d), FeRAM readout scheme in b) and e), and FTJ readout scheme in c) and g). The $I_D V_G$ characteristic of readout transistor T3 is shown in f), indicating the node n1 voltages that correspond to the measured source line currents. The measured curves for the erased state ($V_{ER}=4V$) are colored in blue, while the measured curves for the programmed state ($V_{PR}=[2.0V \dots 3.8V]$) are colored in red.

polarization state the gate voltage of T3 will change during read operation, which can be detected as a change in the S/D current of T3 that is measured at the SL. By successively increasing the program pulse voltage (depicted as green arrow in Fig. 3b) the read current corresponding to the programmed state increases gradually, indicating the possibility for multi-level operation (red curves). In Fig. 3c) the FTJ operation scheme is shown schematically. In this scheme the program / erase operation is performed again in a similar way as for the FeFET and FeRAM scheme. However, the pre-charge voltage of node n1 is increased such that a voltage difference of about 1.0 V is applied between n1 and PL1/PL2 terminals. This voltage difference leads to a polarization state-dependent leakage current that flows through the gate stack of the FeFET. In that way the FeFET gate stack is operated as an FTJ. In the case of a programmed low-VT state of the FeFET (red curves) the gate leakage is larger than for the case of a stored erased high-VT state and n1 discharges faster the stronger the previous programming pulse was performed. By successively increasing the program pulse voltage (depicted as green arrow in Fig. 3c) the measured read current at the SL shown in Fig. 3g) decreases gradually, again indicating the possibility for multi-level operation. Note, that the comparatively small read signal could be strongly increased by cell optimization for the FTJ operation. For example, the gate capacitance of T3 can be reduced strongly, since it must not be matched to the capacitance of T4 (C1) and the operation point of T3 might be optimized.

SUMMARY

In our work we propose a 2T1C ferroelectric memory cell that consists of a ferroelectric capacitor and a sense as well as an access transistor. We demonstrate the possibility to sense the polarization state of small FeCAPs and FTJs that eventually might be integrated as scaled planar capacitor structures either as MFIS-stacks in the FEOL or as MIM or MFIM stacks in the BEOL of a CMOS technology. The cell offers high flexibility

to be optimized for different applications, including multi-capacitor access for cell-internal logic-in-memory operations in dense memory arrays.

ACKNOWLEDGMENT

The authors gratefully acknowledge support by GLOBALFOUNDRIES Fab1 LLC & Co. KG, Dresden, Germany. This work was financially supported by the European Fund for regional Development EFRD and the Free State of Saxony, Europe supports Saxony.

REFERENCES

- [1] S. Slesazek, U. Schroeder and T. Mikolajick, "Embedding hafnium oxide based FeFETs in the memory landscape," 2018 International Conference on IC Design & Technology (ICIDT), Otranto, pp. 121-124, 2018.
- [2] S. Fujii et al., "First demonstration and performance improvement of ferroelectric HfO₂-based resistive switch with low operation current and intrinsic diode property," IEEE Symp. on VLSI Techn., pp. 148., 2016.
- [3] B. Max, M. Hoffmann, S. Slesazek, and T. Mikolajick, "Ferroelectric Tunnel Junctions based on Ferroelectric-Dielectric Hf_{0.5}Zr_{0.5}O₂/Al₂O₃ Capacitor Stacks", ESSDERC, 2018.
- [4] X. Tian and A. Toriumi, "New Opportunity of Ferroelectric Tunnel Junction Memory with Ultrathin HfO₂-based Oxides," 2017 IEEE Electron Devices Tech. and Manufact. Conference (2017) pp.63, 2017.
- [5] F. Mo et al., "Scalability Study on Ferroelectric-HfO₂ Tunnel Junction Memory Based on Non-equilibrium Green Function Method with Self-consistent Potential," IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2018, pp. 16.3.1-16.3.4., 2018.
- [6] C. Richter et al., "Si Doped Hafnium Oxide—A "Fragile" Ferroelectric System," Adv. Electron. Mater. 2017, 3, 1700131, 2017.
- [7] M. Trentzsch et al., "A 28nm HKMG super low power embedded NVM technology based on ferroelectric FETs," 2016 IEEE Internat. Electron Devices Meeting (IEDM), San Francisco, CA, 2016, pp. 11.5.1-11.5.4.
- [8] K. Ni et al., "SoC Logic Compatible Multi-Bit FeMFET Weight Cell for Neuromorphic Applications," 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, pp. 13.2.1-13.2.4, 2018.
- [9] H. Mulaosmanovic, J. Ocker, S. Müller, M. Noack, J. Müller, P. Polakowski, T. Mikolajick, and S. Slesazek, "Novel ferroelectric FET based synapse for neuromorphic systems," in Proc. Symposium on VLSI Technology (VLSIT), June 2017, pp. T176-T177.