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Erstveröffentlichung in / First published in:

International Integrated Reliability Workshop (IIRW). South Lake Tahoe, 07.-11. Okt.2018. IEEE. ISBN 978-1-5386-6039-3

DOI: [https://doi.org/ 10.1109/IIRW.2018.8727101](https://doi.org/10.1109/IIRW.2018.8727101)

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Off-state Impact on FDSOI Ring Oscillator Degradation under High Voltage Stress

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Abstract—The degradation predicted by classical DC reliability methods, such as bias temperature instability (BTI) and hot carrier injection (HCI), might not translate sufficiently to the AC conditions, which are relevant on the circuit level. The direct analysis of circuit level reliability is therefore an essential task for hardware qualification in the near future. Ring oscillators (RO) offer a good model system, where both BTI and HCI contribute to the degradation. In this work, it is qualitatively shown that the additional off-state stress plays a crucial role at very high stress voltages, beyond upper usage boundaries. To yield an accurate RO lifetime prediction a frequency measurement setup with high resolution is used, which can resolve small changes in frequency during stress near operation conditions. An ACDC conversion model is developed predicting the resulting frequency change based on DC input data. From the extrapolation to 10 years of circuit lifetime the model predicts a very low frequency degradation below 0.2% under nominal operation conditions, where the off-state has a minor influence.

Keywords—circuit reliability, ring oscillator, FD-SOI, off-state, bias temperature instability, hot carrier injection

I. INTRODUCTION

Fully-depleted silicon on insulator (FDSOI) technology featuring low substrate parasitics and good electrostatic control of short channel effects offers superior performance for low-power as well as emerging RF applications [1], [2]. Targeting high frequency applications degradation predicted by classical DC reliability methods, such as bias temperature instability (BTI) and hot carrier injection (HCI), might not translate sufficiently to the circuit level [3]. The direct analysis of circuit level reliability is therefore an important task for hardware qualification of the near future.

One type of circuit, which has gained particular interest in this respect, is the ring oscillator (RO). Due to the periodic nature of stress during operation, ring oscillators present a good model system, where both BTI and HCI contribute to the degradation (see Fig. 1). While, the amount of HCI can be varied by varying the number of stages due to self-heating effects at higher frequencies [4], the BTI portion of the resulting frequency degradation is largely independent on the operation frequency [5]. Also it has been shown on bulk-technology, that time-dependent dielectric breakdown (TDDB) has only a minor influence on RO degradation, and the circuit is operable also beyond the first gate oxide breakdown [6]. As a result, BTI degradation is still assumed to be the most important contributor to the aging of RO circuits with many stages [7].

This work was financially supported by the European Fund for regional Development EFRD and the Free State of Saxony, Europe supports Saxony.

Fig. 1. (a) Schematic of the used ring oscillator test structures. In this study the number of stages N is 101. A 1024x frequency divider is used at the output. (b) Schematic voltage evolution and stress modes during RO operation.

However, an often neglected contribution to the device degradation is the off-state, i.e. the operation state, where the drain voltage is high, but gate voltage is low. This state is inherently present in all devices of the RO for roughly 50% of the time. It was shown for 28 nm bulk devices, that the off-state has an impact on the dynamic threshold voltage relaxation of high-k metal gate devices after PBTI stress [8]. However, for ACDC analysis often the zero-voltage case ($V_D = V_G = 0$ V) is assumed, when BTI stress is removed. Thus, the off-state contribution to the actual circuit degradation is unexplored.

In this work, we will qualitatively show that off-state stress indeed plays a crucial role at very high stress voltages. Albeit those voltages are beyond the upper usage boundaries of the technology, the off-state might influence the degradation during voltages accelerated stress conditions used for the sake of model building. To yield an accurate RO lifetime prediction a frequency measurement setup with high resolution is used, which can resolve small changes in frequency after stress near operation conditions. Based on these measurement data an ACDC conversion model for the prediction of the RO degradation under use conditions is presented.

II. EXPERIMENTAL DETAILS

ROs with 101 stages composed of short-channel FDSOI transistors are stressed at various voltages and temperatures for up to 100,000 s. The RO were built of core devices with high-k metal gate and SOI thicknesses smaller than 7 nm [1]. SiGe channels were introduced for the pFET devices via a condensation anneal [9]. Dual in-situ doped epi processes and low-k spacer technology were used to ensure highly doped S/D regions as well as low gate-to-drain capacitances. Channel length varied from 20 nm to 40 nm, while the device width was kept constant at 170 nm. Stress phases are interrupted frequently to monitor the degradation of

oscillation frequency as well as the supply current at nominal operation conditions [10]. The RO output frequency was measured with a 500 MHz, 4 GS/s digital oscilloscope allowing for very high resolution down to the mHz range. The output signal of the RO test structure was sensed with one oscilloscope's channel set to 1 MΩ input impedance. The oscilloscope was remotely configured and controlled so that for a defined time interval (here 2 s) the waveforms were continuously acquired and the signal periods are detected and measured. After the defined time interval the oscilloscope returned a calculated averaged value of the individual frequency measurements. As a result the standard deviation of each measurement point is in a range of 500-800 Hz. As compared to a low resolution single point freq. measurement, a smooth degradation can be revealed even at low stress voltages near nominal operation conditions (Fig. 2).

In addition to the measurements of ring oscillator structures, DC characterization of individual pFETs and nFETs under BTI, HCI and off-state stress conditions were carried out. The results were used to extract model coefficients for the sake of building an ACDC conversion model and compare with the RO data, as described in the following sections.

III. MODELING RING OSCILLATOR DEGRADATION

The frequency degradation of a balanced RO, i.e. an oscillator with equal rise and fall times, can be modeled by the following equation [11]:

$$\frac{\Delta f}{f_0} = \frac{1}{2} \left(\frac{\Delta I_{D,n}}{I_{D,n}} + \frac{\Delta I_{D,p}}{I_{D,p}} \right) \quad (1)$$

Here f is the RO frequency and $I_{D,(np)}$ the drain saturation current of n-MOS and p-MOS device respectively. The current degradation of both devices can be split into a BTI and a HCI contribution:

$$\frac{\Delta I_{D,n}}{I_{D,n}} = \frac{\Delta I_{D,n}}{I_{D,n}}(BTI) + \frac{\Delta I_{D,n}}{I_{D,n}}(HCI) \quad (2)$$

and

$$\frac{\Delta I_{D,p}}{I_{D,p}} = \frac{\Delta I_{D,p}}{I_{D,p}}(BTI) + \frac{\Delta I_{D,p}}{I_{D,p}}(HCI). \quad (3)$$

Each contribution individually can be modeled by a DC to AC conversion formula, as introduced hereafter.

A. Modeling HCI contribution

The HCI contribution to the current degradation of an individual transistor within the ring oscillator can be given in the following functional form:

$$\frac{\Delta I_D}{I_{D,0}}(HCI) = \frac{A^* \cdot (t_{eq})^n}{1 + D \cdot A^* \cdot (t_{eq})^n}, \quad (4)$$

where D is a saturation factor and A^* can be given as:

$$A^* = A_{l,w,T}^{HCI} \cdot (s \cdot V_{DD})^m \cdot R_{\Delta} \quad (5)$$

where $A_{l,w,T}^{HCI}$ is a pre-factor, which is dependent on device length l , device width w , as well as operation temperature T . V_{DD} is the RO operation voltage, n and m are the DC

Fig. 2. Effect of measurement resolution on the detected freq. degradation. The dotted line marks the resolution limit of the standard low-resolution setup.

coefficients for time and voltage acceleration, respectively. The prefactor as well as the acceleration coefficients are determined by DC measurements under worst case HCI stress conditions. Within the RO, the strongest HCI present during the switching event is assumed at the crossing point where V_{DS} is equal to V_G . Thus, the applied supply voltage is reduced by a scaling factor s to yield the maximum effective stress voltage contributing to HCI during the switching event. In literature a typical cross point of 0.7 to 0.8 $\cdot V_{DD}$ is stated [12]. The equivalent DC stress time t_{eq} can be given by $t_{eq} = (t \cdot Z)$. Here a duty cycle factor Z of 0.005 was chosen. Both duty cycle factor Z and voltage scaling factor s are confirmed via cadence circuit simulations of the RO circuit. Finally, HCI waveform during switching was approximated with a triangular shape, reducing the effective stress by a factor of R_{Δ} :

$$R_{\Delta} = \frac{1}{(s \cdot V_{DD} - V_{min})} \frac{\int_{V_{min}}^{(s \cdot V_{DD})} |V_{ds}|^m dV_{ds}}{V^m} \quad (6)$$

B. Modeling BTI and off-state contribution

In DC characterization BTI degradation is typically monitored as a shift of the threshold voltage. Thus a factor C for converting the measured V_{TH} shift into $I_{D,sat}$ degradation is necessary. The resulting functional form of the BTI contribution to the current degradation of an individual transistor within the ring oscillator can be given as:

$$\begin{aligned} \frac{\Delta I_D}{I_{D,0}}(BTI) &= C \cdot \frac{\Delta V_{TH}}{V_{TH,0}} \\ &= C \cdot A_{l,w,T}^{BTI} \cdot (V_{DD})^p \cdot (t_{eq})^q \cdot R_{ACDC} \end{aligned} \quad (7)$$

where $A_{l,w,T}^{BTI}$ is a pre-factor, which is dependent on device length l , device width w , as well as operation temperature T . V_{DD} is the RO operation voltage, p and q are the DC BTI coefficients for time and voltage acceleration, respectively. A duty cycle factor Z of 0.5 was chosen for the BTI degradation under RO operation. R_{ACDC} is a factor accounting for the additional relaxation due to AC conditions and off-state. This is exemplarily shown in Fig. 3, where the normalized V_{TH} shifts during BTI stress under various waveforms are compared. It is evident that the absolute threshold voltage shift is lower during AC BTI than during DC BTI, albeit the effective BTI stress times are equal. This is reasoned in a significant amount of relaxation occurring during the zero

Fig. 3. Normalized V_{th} shift of an nFET after BTI stress with various waveforms. A distinct amount of relaxation is present for AC BTI stress with 100 kHz and 50% duty cycle (blue line) as compared to the DC stress data (green line). Even more relaxation is present, when an intermediate off-state voltage is introduced while the BTI stress is withdrawn (red lines).

volt state. If an additional off-state bias ($V_D = V_{STRESS}$; $V_G = 0$ V) is introduced while the BTI stress voltage is withdrawn, the permanent degradation is reduced even further, due to an accelerated de-trapping of charges in comparison to the zero volt case. A similar effect has already been observed by Kupke et al. in 28 nm bulk devices with high-k metal gate [8].

IV. RESULTS AND DISCUSSION

In this section the measured RO frequency degradation is compared with the calculations by the converted DC model proposed in section III. It will become evident, that two main regimes can be differentiated. At near usage case stress conditions, where the high resolution measurement setup is needed, the proposed ACDC conversion model fits the measured RO data very well. A further increase of the stress-voltage beyond upper usage boundaries for experimental purpose leads to a deviation from the proposed ACDC model prediction. It will be shown, that this deviation can be qualitatively explained by an increased impact of the off-state under high voltage stress conditions. However, the region where the off-state has only a minor influence will be discussed first.

A. Model Validation under Near Operation Conditions

Under near operation voltage stress conditions, the RO frequency decreases monotonically with increased stress time. The corresponding current at the supply line is decreasing over time, which is in accordance with the expectation set by the underlying model equations. If the stress voltage is increased during operation, both the RO frequency degradation as well as the reduction in current are more pronounced. In this region, the proposed equivalent DC model fits the measured frequency degradation quite well (compare Fig 4). The model was validated across several channel length, voltages and temperatures. After 100,000 s of stress the predicted degradation splits into roughly 80% BTI contribution and 20%

Fig. 4. Frequency degradation measurements (dots) and converted DC model data (lines) for RO's with various channel length L_{CH} all measured at 125°C. A good fit is achieved for low stress voltages and larger channel lengths, where the off-state has only a minor influence.

Fig. 5. Monitored drain current evolution during RO operation. At low voltages near operation condition the current degrades over time. In the intermediate region higher stress voltages lead to higher degradation. A reversal of the characteristics is seen at very high voltage stress due to off-state effects. The effect is more pronounced at shorter channel lengths.

HCI contribution. As opposed to results on 45 nm SiON technology, where PBTI has nearly no influence on the frequency degradation of a RO [11], both PBTI and NBTI contribute nearly equally in this high-k technology. From the extrapolation to 10 years of circuit lifetime the model predicts a very low frequency degradation of below 0.2% under nominal operation conditions.

B. Off-state Impact under high Voltage Stress

For experimental purpose, the stress conditions were increased beyond the upper usage boundaries of the technology. Beyond a certain limit (e.g. $V_{\text{STRESS}} > 1.8 \cdot V_{\text{MAX}}$ for $L_{\text{CH}} = 36 \text{ nm}$) a reversal of the monitored current characteristics is observed. Instead of a stronger decrease, which would be expected by a more pronounced BTI degradation, a saturation and even increase in current is evident (compare Fig. 5, half open symbols). Simultaneously, the measured frequency degradation starts to deviate from the proposed ACDC model prediction. This effect is more pronounced in devices with shorter channel lengths (compare Fig. 4 and 5, full symbols) and increases with higher stress voltage and operation temperature. Based on the RO operation modes, the additional off-state stress is the most likely root cause for this observation. Thus, individual devices were stressed under DC off-state conditions and the results were compared to the characteristics observed in the RO. Interestingly, if the individual devices are stressed in static off-state mode ($V_D = V_{\text{STRESS}}$; $V_S = V_G = 0 \text{ V}$) an increase in drain current, being similar to that seen in the RO, is observed (Fig. 6). This positive $I_{D,\text{sat}}$ shift is more pronounced in the pMOS devices, than in the nMOS devices. Further, the effect increases with temperature, stress voltage and reduced channel length (compare Fig. 6). Qualitatively, this matches well with the behaviour of the current evolution during RO operation under high voltage stress.

One explanation for the current increase that seems natural is a drain sided breakdown of the gate oxide under the elevated bias conditions. However, in the analysed devices no increase in gate current was monitored. Thus, another explanation of the physics behind the off-state stress has to be found. The origins of the current increase becomes evident, if the individual I_D - V_G characteristics prior and after stress are compared as shown exemplarily in Fig. 7. It can be seen, that the transfer characteristic after stress matches the unstressed characteristic exactly, if a V_{TH} correction into the opposite direction of a classical BTI shift is applied. The visible current increase is directly correlated to this off-state induced V_{TH} shift. TCAD simulations of an exemplary FDSOI device structure were carried out to visualize the field distribution under off-state stress conditions (Fig. 8). It becomes evident, that high electric fields are present at the drain-sided dielectric interface under off-state conditions. Under this conditions drain sided traps are filled. As a result a local V_{TH} shift is induced at the drain side of the channel, which qualitatively explain the electrical results shown in Fig. 7. During circuit operation this off-state induced V_{TH} shift counteracts the BTI degradation [8] leading to an effectively much higher BTI relaxation factor R_{ACDC} . This explains the differences in frequency degradation above usage boundaries, where the off-state is dominant. Simultaneously, the measured cross current increases. Thus, the additional off-state stress qualitatively explains the observed features of the RO degradation present under high voltage conditions. Near operation conditions the off-state effect is small over the product lifetime, but still influences relaxation.

Fig. 6. Normalized positive drain current change of various devices under pure off-state stress ($V_G = 0 \text{ V}$; $V_{\text{DS}} = V_{\text{STRESS}}$) at a temperature of 125°C . A similar trend is achieved for pFET and nFET for various voltages, device lengths. The lines are guides to the eye.

Fig. 7. I_D - V_G characteristics of a pFET after a reasonable time of pure off-state stress ($V_G = 0 \text{ V}$; $V_{\text{DS}} = V_{\text{STRESS}} > 1.8 \cdot V_{\text{MAX}}$) at 125°C . If the stress transfer characteristics (red line) are corrected by a V_{TH} shift of 30 mV (magenta triangles) the unstressed characteristic is matched (blue line).

Fig. 8. TCAD Simulation of field distribution under off-state stress conditions similar to the one used in Fig. 7 ($V_G = 0 \text{ V}$; $V_{\text{DS}} = V_{\text{STRESS}} > 1.8 \cdot V_{\text{MAX}}$) showing high electric fields in the drain sided interface (arrow).

V. CONCLUSION

To conclude, we have shown that at very high voltage stress, beyond typical operation limits, the degradation of a FDSOI ring oscillator is largely influenced by additional off-state effects. It has been shown, that the off-state induces a local V_{TH} shift in the opposite direction of a BTI degradation. Simultaneously the drain current during RO operation increases. As a result a high resolution setup for acquiring RO frequency is recommended to analyze the RO in a near operation regime, where the off-state has only a minor influence. Based on this experimental evidence an ACDC conversion model was proposed predicting the frequency degradation of 22 nm FDSOI ring oscillators under nominal operation conditions. An extrapolation to 10 years of circuit lifetime yields a frequency degradation below 0.2%.

ACKNOWLEDGMENT

The authors like to acknowledge the assistance and support of the GLOBALFOUNDRIES RF and reliability teams.

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