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Demonstration of versatile nonvolatile logic gates in 28nm HKMG FeFET technology

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Abstract—Logic-in-memory circuits promise to overcome the von-Neumann bottleneck, which constitutes one of the limiting factors to data throughput and power consumption of electronic devices. In the following we present four-input logic gates based on only two ferroelectric FETs (FeFETs) with hafnium oxide as the ferroelectric material. By utilizing two complementary inputs, a XOR and a XNOR gate are created. The use of only two FeFETs results in a compact and nonvolatile design. This realization, moreover, directly couples the memory and logic function of the FeFET. The feasibility of the proposed structures is revealed by electrical measurements of HKMG FeFET memory arrays manufactured in 28nm technology.

Keywords—FeFET; Logic-in-Memory; XOR; Logic Gates; nonvolatile

I. INTRODUCTION

One of the most critical issues for data processing and evaluation these days is the von-Neumann bottleneck, as it limits the data throughput, as well as the reduction of power consumption. Logic-in-memory (LiM) with its fine-grained structure is a promising candidate to overcome the existing bottleneck between logic and memory units. Different concepts, based on e.g. magnetic tunnel junctions [1], memristors [2], ferroelectric capacitors [3], floating gate FETs [4], ferroelectric field effect transistors (FeFETs) [5], and spin Hall effect-driven domain wall motion devices [6], were proposed previously. Several nonvolatile logic gates were developed based on two-terminal devices (e.g. FeCaps [3], domain-wall nanowires [7], and memristors [2]) resulting in either a larger area overhead, the necessity for separate reference voltage supplies, or several write/ read steps. Here, we report on nonvolatile logic circuits based upon logic AND and OR gates adopting only one FeFET [8], where one input state is stored internally and the second one is applied externally to the gate terminal of the FET. By connecting, for example, two single FeFET AND gates in parallel, the logic output is $(A \wedge B) \vee (C \wedge D)$, with the internal inputs A and C and external inputs B and D. Thus, three logic operations with four inputs are processed by only two FeFETs. By substituting C and D by NOT A (!A) and NOT B (!B), respectively, it is possible to create a XNOR logic gate between the inputs A and B. To show the functionality of the proposed

gates within existing memory structures, the FeFET logic gates are directly integrated in AND or NAND memory arrays manufactured in 28nm HKMG technology. Electrical characterization based on such arrays reveal the basic functionality of the proposed logic gates. Thus, the concept can be realized by a small number of transistors, and provides nonvolatility by storing one input in the polarization state of the FeFET. This is especially useful if one or more input states stay constant. Data centric digital filters are one example for such an application.

II. EXPERIMENTAL

The n-channel FeFET structure used in this work was realized in a 28 nm HKMG technology and is arranged in an AND as well as a NAND memory array [9]. The Metal-Ferroelectric-Insulator-Semiconductor gate structure (MFIS-FET) features a TiN/Si:HfO₂/SiO₂/Si gate stack. Channel length and width are $L = 90$ nm (AND array) or $L = 30$ nm (NAND array) and $W = 80$ nm, respectively. The FeFET is programmed or erased by applying positive or negative voltage pulses (± 5 V for 1 μ s) to the gate terminal (word line) of the FeFET to induce polarization switching in the ferroelectric layer. Thus, the FeFET is set in the low threshold voltage ($V_{T,L}$) or high threshold voltage ($V_{T,H}$) state (Fig. 1). The gates were characterized by transient output voltage (V_{out}) measurements using an oscilloscope. Output current (I_{out}) measurements were performed adopting Keithley pulse measurement units (PMUs).

Fig. 1: Schematic of the polarization states of an n-channel FeFET. The low V_T state and high V_T state are shown in a) and c), respectively. A corresponding program (Prg)/ erase (Ers) and logic read scheme is depicted in b) and d).

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III. FEFET LOGIC-IN-MEMORY CONCEPTS

A FeFET is a nonvolatile transistor device with a polarizable ferroelectric layer (Fig. 1a and 1c), causing a hysteretic drain current-gate voltage (I_d - V_g) characteristic. Consequently, the threshold voltage V_T likewise depends on the internal polarization state of the ferroelectric. In the following, the internal polarization state is utilized as one input (input A) of a logic gate, where the high threshold voltage I_d - V_g curve is equivalent to a logical zero, while the low threshold voltage I_d - V_g curve corresponds to a logical one (Fig. 2). By applying an external gate voltage $V_{g,ext}$, different output currents I_{out} can be measured for the high threshold voltage and the low threshold voltage I_d - V_g curve ($I_{out,highVT}$ and $I_{out,lowVT}$, respectively). Therefore, the externally applied gate voltage is used as the second input (input B). With a suitable choice of two gate voltages ($V_{g,ext1}$ and $V_{g,ext2}$), representing a logical zero and one state, a logic AND or OR operation between the consecutively applied inputs A and B can be implemented by one single FeFET. Details were described recently in [8]. These basic single FeFET logic gates are now used to create more complex cascaded logic as presented in the following sections.

A. Selected cascaded logic gates

To utilize the single FeFET AND and OR logic gate concepts as presented in [8] for more complex logic functions, the single logic gates are cascaded in parallel or in series (Fig. 3a and 3c). Serially connected AND gates or parallel connected OR gates constitute only multiple input AND or OR gates, respectively, and are thus not considered here. On the contrary, in case of a parallel arrangement of two logic AND gates, the logic equivalent of the output current I_{out} can be expressed by:

$$Z_1 = (A \wedge B) \vee (C \wedge D), \quad (1)$$

and, in case of a serial connection of two OR gates by:

$$Z_1 = (A \vee B) \wedge (C \vee D) = A \wedge C \vee A \wedge D \vee B \wedge C \vee B \wedge D, \quad (2)$$

where the logic inputs are A, B, C and D. When using an pull-up device, the logic equivalent of the output voltage V_{out} is $Z_V = !Z_1$ (NOT Z_1). $Z_1 = 0$ and $Z_1 = 1/Z_V = 0$ and $Z_V = 1$ correspond to a low and high output current/ output voltage level, respectively. These kind of device structures can be integrated

Fig. 2: I_d - V_g curve of a FeFET, where the dashed, red curve corresponds to the low threshold voltage state and the solid, blue curve represents the high threshold voltage state. Input A (internal polarization state) and B (externally applied gate voltage) are the possible inputs of a logic gate, where $I_{out} < I_{threshold}$ and $I_{out} > I_{threshold}$ can be interpreted as a logical 0 and 1 at the output, respectively [8]. I_{out} corresponds to I_d of a single FeFET.

Fig. 3: Two FeFET AND gates [8] connected in parallel (a), which can e.g. be implemented in an AND memory array (b). A series connection of two FeFET OR gates [8] (c) can for example be integrated into NAND memory arrays (d). WL mark word lines. BL and SL are bit and source lines, respectively. PU corresponds to the pull-up device.

in AND and NAND memory arrays as shown in Fig. 3b and 3d. Thus, a simple logic-in-memory structure consisting of cascaded single FeFET AND and OR logic gates is achieved.

B. $X(N)OR$, a special case of paragraph A ($C = !A$, $D = !B$)

A special case follows from the above in case $C = !A$ (NOT A) and $D = !B$ (NOT B). That is, the two FeFETs (FE1 and FE2, Fig. 4) exhibit the opposite internal polarization states A (FE1) and !A (FE2). Subsequently, the external input B as well as its complement, !B, are applied to the gates of the FeFETs FE1 and FE2, respectively. V_s is grounded, while $V_{dd} > 0$ V. In those cases, (1) results in:

$$Z_1 = (A \wedge B) \vee (!A \wedge !B) \quad (3)$$

and (2) rewrites to:

$$Z_1 = (A \wedge !B) \vee (!A \wedge B). \quad (4)$$

Fig. 4: Proposed XNOR logic gate (a) and XOR logic gate (b) (regarding I_{out}), consisting of only two FeFETs acting as logic AND or OR gates. To achieve this, two FeFET AND gates [8] are connected in parallel (a) or two FeFET OR gates [8] are connected in series (b). With a pull-up device PU in series, a XOR gate (a) and XNOR gate (b) regarding the output voltage V_{out} is created.

TABLE I: LOGIC TABLE OF THE PROPOSED X(N)OR LOGIC GATES, AS CONSTITUTED BY THE PARALLEL CONNECTION OF TWO LOGIC FEET AND GATES OR THE SERIES CONNECTION OF TWO LOGIC FEET OR GATES. $Z_I = 0$ AND $Z_I = 1 / Z_V = 0$ AND $Z_V = 1$ CORRESPOND TO A LOW AND HIGH OUTPUT CURRENT I_{out} / VOLTAGE V_{out} LEVEL, RESPECTIVELY.

Internal input		External input		Output (AND gates in parallel)		Output (OR gates in series)	
A	!A	B	!B	Z_I	Z_V	Z_I	Z_V
0	1	0	1	1	0	0	1
0	1	1	0	0	1	1	0
1	0	0	1	0	1	1	0
1	0	1	0	1	0	0	1

Regarding the current, a XNOR (3) and a XOR (4) logic gate is obtained (Fig. 4a and 4b, Table I).

The working principle of the X(N)OR logic gate of (3) with two parallel connected FeFETs is then as follows, assuming that each of the two FeFETs acts as a logic AND gate. In case that one of the inputs, A or B, is logical one and the other one is zero, none of the two FeFETs is in the conducting state, leading to a negligible current flow ($Z_I=0$). If both inputs, A and B, carry either a logical zero or one, one of the FeFETs would be conducting with a suitable current flow (i.e. $Z_I=1$). Thus, the two FeFETs constitute a XNOR logic gate regarding the output current and a XOR gate regarding the output voltage V_{out} (Table I). Similar structures can be used in TCAM cells (see [5]).

The X(N)OR logic gate of (4) with two serially connected FeFETs works as follows, assuming that each of the two FeFETs acts as an OR gate. In case both inputs, A and B, are in the logical zero or one state, one FeFET is in the conducting state while the other one is not. Due to the serial connection of both FeFETs no cross current is flowing ($Z_I=0$). As soon as either A or B carry a logical one, both FeFETs are in the conducting state, resulting in a high current flow ($Z_I=1$). Regarding the cross current I_{out} and the output voltage V_{out} the described logic gate acts as a XOR or XNOR logic gate, respectively (Table I).

If the proposed X(N)OR logic gate with parallel FeFETs is about to be implemented in a memory-array-like structure, the AND memory array is most favorable, because it mimics the parallel connection structure well by the shared bit and source lines. Furthermore, the cross talk between adjacent gates can be decreased by adjusting the potential of the unused word, bit and source lines. On the contrary, the NAND memory array mimics the X(N)OR logic gate with serially connected FeFETs best. However, suitable inhibit schemes during program and erase operation would require matching capacitance as in conventional NAND memory arrays.

IV. RESULTS AND DISCUSSION

In the following, measurement results for the cascaded FeFET AND and OR logic gates as well as the two-FeFET X(N)OR logic gates are presented. In all cases, the internally stored logical inputs A or C (!A) are first written into the FeFET by applying gate voltages of -5 V/+5 V (applied for 1 μ s) to erase

(logical "0") or program (logical "1") the FeFET. To circumvent a negative write voltage at the gate, a positive source/ drain write scheme might be applied for small channel devices [10]. Subsequently, the second logical inputs B or D (!B) are applied to the gate terminal of the FeFETs with a read scheme similar to the one depicted in Fig. 1b and 1d. For the demonstration of the concept, AND and NAND memory arrays were used as the test vehicles for the parallel connected FeFET AND gates and the serially connected FeFET OR gates, respectively (see also Fig. 3b and 3d). A 1 M Ω resistor was used as a pull-up device.

A. Selected cascaded logic gates

Fig. 5 shows the transient current and voltage plots of two FeFET AND gates connected in parallel (Fig. 5a) and two

a) Parallel cascaded AND gates ($Z_I = (A \wedge B) \vee (C \wedge D)$, $Z_V = !Z_I$)

b) Serially cascaded OR gates ($Z_I = (A \vee B) \wedge (C \vee D)$, $Z_V = !Z_I$)

Fig. 5: Cascaded logic gate of two single logic FeFET AND gates connected in parallel (a) and OR gates connected in series (b) with one pull-up resistor (1 M Ω) in series. The logic function and the logic inputs are given above. Z_I and Z_V are the logical levels of the corresponding output current and voltage, respectively.

FeFET OR gates connected in series (Fig. 5b). According to the I_d - V_g characteristics of the FeFETs used here, the externally applied gate voltages had to be adjusted to achieve AND or OR logic gate behavior of the single FeFETs [8]. To represent a logical "0" or "1", the gate voltages at inputs B/D were therefore chosen to be -0.5 V and 0.2 V in case of the parallel connected FeFETs and -0.4 V and 0.2 V in case of the serially connected FeFETs. The same gate input voltages for logic FeFET AND and OR gates are possible if an operation scheme as presented in [8] is used. The results demonstrate the successful operation of FeFETs as logical AND and OR gates in cascaded structures. As shown in Fig. 5, a low current ($I_{out} < 2 \cdot 10^{-7}$ A) was measured if the logic condition $Z_I = 1$ was not met. If the condition is fulfilled, a high current ($I_{out} > 6 \cdot 10^{-7}$ A) can be determined. Ideally, the output voltage corresponds to V_{dd} (if $Z_V = 1$) or to V_s (if $Z_V = 0$). Due to a residual voltage drop over the pull-up device, V_{dd} might not be reached. Moreover, in case of a NAND array (Fig. 5b), low channel resistance of the FeFETs is crucial as it determines the output voltage equivalent to $Z_V = 0$, which in the ideal case should reach V_s . Hence, to improve the electrical characteristic of the complex logic gates, both the FeFET design point as well as the characteristic of the pull-up device have to be optimized and well matched. In that way the rise and fall times of the output voltage can be adjusted as well. In the current setup, a high static power consumption resulting from the static current flow through the pull-up resistor is observed. Reductions of static power consumption may be achieved by introducing p-channel FeFETs as pull-up devices (similar to CMOS logic) or of clocked pull-up/ pull-down transistors.

B. X(N)OR gates

In Fig. 6 the recorded output current and voltage transients of the X(N)OR gate with two parallel connected logic FeFET AND gates (Fig. 6a) and two serially connected logic FeFET OR gates (Fig. 6b) are plotted. Adoption of complementary inputs (!A and !B) requires the input signals (A and B) to be logically inverted. The key figures of the proposed X(N)OR gates are:

- number of transistors: 2 FeFETs + 1 pull-up device in series
- amount of cycles for one operation: 2 (with write cycle), 1 (if input A is permanently written into the FeFETs)
- read gate voltage (input B): -0.5 V ("0") and +0.2 V ("1") (Fig. 6a), -0.3 V ("0") and +0.2 V ("1") (Fig. 6b)

As presented, one read voltage is chosen to be negative to obtain the desired logic functionality of the FeFET. In order to use only positive voltages, the I_d - V_g curves of the FeFETs may be shifted along the positive gate voltage axis as shown in [8]. The gate exhibits the expected X(N)OR behavior for the inputs A (internal polarization state of the FeFET) and B (external gate voltage) regarding the output current and voltage (Fig. 6).

V. CONCLUSION

We presented for the first time the application of only two FeFETs in compact, four-input nonvolatile logic gates. Starting from this and by applying complementary input signals, it is possible to construct compact two-FeFET logic X(N)OR gates. Electrical measurements confirmed the functionality of the

a) X(N)OR: parallel connected AND gates ($Z_I = (A \wedge B) \vee (!A \wedge !B)$, $Z_V = !Z_I$)

b) X(N)OR: serially connected OR gates ($Z_I = (A \wedge !B) \vee (!A \wedge B)$, $Z_V = !Z_I$)

Fig. 6: Transient diagrams of the output voltage V_{out} and the output current I_{out} of the proposed X(N)OR gates. Therefore two single logic FeFET AND gates are connected in parallel (a) and two single logic FeFET OR gates are connected in series (b). A pull-up resistor (1 MΩ) is used. Z_I and Z_V are the logical levels of the corresponding output current and voltage, respectively (see also Table I).

proposed structures and the possibility to implement such logic structures within AND or NAND memory arrays. Due to its simplicity and the capability to build basic logic gates, the construction of other logic structures is possible, e.g. half and full adders. The nonvolatility of the FeFET moreover directly connects logic (FeFET as a logic gate) with memory (internally stored input). Thus, the concept is especially of interest if one input is permanently saved and has to be configured only once, since the endurance of the FeFETs used here is limited to 10^5 cycles but the retention time is 10 years (extrapolated) [11]. Consequently, a low gate input voltage can be used during normal logic operation.

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