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Deconvoluting charge trapping and nucleation interplay in FeFETs: Kinetics and Reliability

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Abstract—Discovery of ferroelectric (FE) behavior in HfO₂ removed the compatibility roadblocks between the state-of-the-art CMOS and FE memories. Even though FE FETs (FeFETs) are scaled into 22 nm nodes and beyond, the limits of the technology as well as the physical mechanisms and reliability are still under research. In this paper we successfully developed a multiscale modeling platform to understand the interplay between the FE switching and charge trapping. Starting from the nucleation theory and rigorous charge transport modeling we present for the first time a self-consistent modeling framework we used for investigation of reliability and variability in FeFETs.

I. DEVICE AND MATERIAL CHARACTERIZATION

The Ferroelectric FETs (FeFETs) represent the core of both low-power non-volatile memory (NVM) solutions and the low-power negative capacitance (NC) logic. Despite the ferroelectricity (FE) in HfO₂ has triggered diverse research and enabled demonstration on 22nm technology nodes [1], the comprehensive understanding of both materials and devices is still under debate. Particularly, the interplay between charge trapping and ferroelectric switching, and its impact on the switching kinetics as well as on the reliability and variability of the device is not clear. Thus, the quantitative understanding of the charge trapping and nucleation interplay is crucial. In detail, the key questions to be answered are: (1) How does the interplay between ferroelectric switching and the charge trapping in HfO₂ influence the performance and scalability of FeFETs; (2) what are the boundary conditions for a reliable operation; (3) how can the material properties be tailored to achieve the maximum reliability for such devices?

Polarization reversal due to the application of the gate voltage sets the FeFET into high and low V_{TH} state (Fig.1). The characterization of FeFET (28nm bulk FET under test) considered for NVM applications shows that during endurance testing the closure of the memory window ($MW = V_{TH+} - V_{TH-}$) starts at the point when the charge trapping begins to dominate the FE switching process (Fig.2). To investigate the complexity of the switching process and find optimal operation conditions, we recorded the program/erase (PRG/ERS) matrices, Fig. 3. Within these maps, three regions can be identified: (1) a region of negative MW where charge trapping (CT) dominates; (2) a region of negligible MW (CT compensates the FE switching); (3) and a region of positive MW where the FE switching dominates. Fig. 4 shows the evolution of these regions with field cycling, exhibiting a drift of the switching region towards pulses with lower amplitude, stabilizing at amplitudes of

around -4 and -5 V and short pulses (1 μ s). After 10⁵ PRG/ERS cycles the CT completely compensates the MW of the FeFET resulting in negative or zero MW. Moreover, the evolution of density of interfacial states reported in [3] indicates that bipolar stress generated by PRG/ERS and the subsequent charging and discharging (carriers tunnel back and forth) degrade the interface properties. Consequently, the increased defect density and deteriorating interface properties may impact the switching kinetics of the FeFET.

II. MULTI-SCALE MODELING PLATFORM

To capture the aforementioned FE switching - CT interplay and reproduce the FE-device kinetics as well as to understand the physical mechanisms behind, we extended a multiscale modeling platform (Fig. 5). This modeling platform is comprised of two main parts, consistently connected, which address the charge transport and stress-induced material modifications, respectively. These are crucial to model device aging and reliability phenomena [4]. The capability to handle individual contributions of atomic species and defects (i.e. interstitial ions and vacancies) is included, along with their diffusion and generation processes. In parallel, the FE properties of the film responsible for switching processes and kinetics are also accounted for. The electric potential within the FE-device is calculated by solving the Poisson equation consistently with time dependent Ginzburg-Landau formalism enriched with the domain interaction and depolarization term. Parameters used in the study are listed in [5,6].

III. CHARGE TRAPPING AND NUCLEATION INTERPLAY

A. Charge trapping

Multiphonon charge transport mechanisms dominated by trap-assisted-tunneling are used to investigate the charge transport within the device whose geometry and doping is depicted in Fig. 6a. We investigated the FE-device behavior by simulating the I_D - V_G evolution during a PRG/ERS cycle. First a device under test was preconditioned and set in the low V_{TH} state to maintain the reference state. As shown in Fig.6b, charge trapping results in a clockwise I_D - V_G curve hysteresis (CW) and negative MW, whereas the FE switching exhibits a counter CW (CCW) hysteresis. The typical clockwise (CW) hysteresis of I_D - V_G curves upon the charge trapping is successfully reproduced by simulating a single pulse (V_{TH} -extracted on rising/falling edges). To investigate the defect distribution within the stack, we consistently model capacitance-voltage (C-V) and I_G - V_G curves of a multistructure- devices (large total gate area) together with parametrized charge trapping experiment (see

Fig. 7a-c) in turn extracting a defect map responsible for the CW hysteresis (Fig. 7d).

A high-operation field results in a high field drop across the low- k interface yielding a much higher generation of defect states within the interfacial layer (IL), see Fig. 8a-c. To investigate the impact of the PRG/ERS on the bulk defects in the HfO_2 layer, we monitored and simulated (using a TAT model) the leakage current [7], which allows extracting the defect density evolution with stress shown in Fig. 8b-c. This increase remains limited as the current transport is dominated by conduction band conduction. Evolving concentration is omitted deliberately due to the combined effect of defect concentration and switching state of the device (details in section B).

B. Interplay between charge trapping and nucleation

The impact of interfacial/bulk defect states on FeFET variability is assessed through Monte Carlo simulations, allowing to investigate the impact of the scaling and defects of the polycrystalline stack on the V_{TH} distribution (Fig. 9a). The impact of the defects and trapped charge on the potential within the gate stack is shown in Fig. 9b.

To assess the impact of the FE- HfO_2 material changes on FE-device performances (including variability and reliability), we show in Fig. 10 the simulation of the evolution of the FE domain orientation over time upon the application of the external excitation field. These domain maps represent a top view of the gate of the FE-transistor with source and drain on the left and right side, respectively. The 2D domain map shows a clear domain reorientation from the initial random condition to a common oriented state, which proves that the model captures nucleation occurring upon application of the electric field. The model accounts self-consistently for the potential changes due to the domain nucleation, as shown in the corresponding potential maps in Fig. 11a. Multiple PRG/ERS operations followed by I_d - V_g readout results in distributions of V_{TH}^+ , V_{TH}^- and MW (Fig. 11b), which is nicely captured by the simulations. Additionally, impact of the different grains (FE switching properties) along the width of device on single device performance was investigated (considering the average grain size of 20-30 nm, 30x80nm FeFET has in average 3 grain along the channel; see [8]). It can be seen that the worst domain (lowest MW when alone) determines the MW of the device (without trapping effects included). Still averaging effect is observable when portion of device is non-FE or pinned; in turn impacting the device to device variation of the FeFET.

In the next step we switched on previously calibrated charge trapping into the model. The band diagrams extracted from the grain 1 and grain 2 (Fig. 11a) are shown in Fig. 13a. Different field over the device changes the dynamics of the charge carrier injection (Fig. 13b-c) which in turn impacts the nucleation of domains along the width of the channel (Fig. 14). Same impact has a band bending and injection level change due to the variation of the program pulse amplitude. Using the developed model, we show that gate leakage is determined by the conduction band transport (similar to FE tunnel junction), thus

the polarized device is characterized with a higher leakage compared to the non-switched device (13b). To gain insight into the kinetics of the trapping, we set the device in different PRG states and simulated a charge trapping (Fig. 13c-d) and gate transients (V_g , I_g) upon application of a single pulse. The comparison of charge trapping kinetics simulated considering both conventional non-switching HfO_2 FET and programmed FeFET shows that the increased band-bending (induced by FE switching) impedes the charge trapping (for this scanning voltage and extracted defect distribution) within the stack, decreasing the trapped- ΔV_{TH} , but increases the gate leakage.

To gain insight into the kinetics of the device and competing processes of charge trapping and FE switching we simulated the FE-gate stack response upon application of the positive gate voltage pulse. Compared to the reference device (without defects and charge trapping), the device with CT effects included (Fig. 15a-b) shows that trapping pins the field at the interface, inducing a stronger change in the field across the FE: HfO_2 , which forces an earlier onset of FE switching (mono-domain) and ability to reach previously inactive "slow" domains (Fig. 14) in multi-domain case. However, with cycling this increased field and repeatedly charge tunneling back and forth through the IF layer results in a complete destruction of the interface and defect generation within the bulk. Finally, this degradation results in increased leakage current. The defect generation and consecutive trapping pins the domains and closes the MW of FeFET (Fig. 15c). The model of the competing processes and degradation is shown in Fig. 16.

IV. CONCLUSION

Within this paper we investigated the interplay between the ferroelectric switching and charge trapping in FeFET devices. We purposely extended a multiscale device modeling platform enabling the self-consistent assessment of this entanglement based on the nucleation FE theory and multiphonon mediated trap assisted transport. We show that the defect generation and subsequent charge trapping strongly impacts the switching kinetics within the FeFETs, thus influencing the distribution of the V_{TH} and directly impacting the MW. With the help of simulations we point out that the degradation of the dielectric and consequent charge trapping results in: 1) a slow-down of switching kinetics and 2) a reduction of the memory window of the FeFET. In summary we demonstrated that the proposed comprehensive model can capture the central physics of the FeFET and as such paves the path towards deeper understanding of the device and further improvement of its already excellent memory properties.

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Figure 1. Schematic representation of the FeFET gate stack comprised of Si/SiO₂/Fe:HfO₂/TiN upon application of a) negative and b) positive pulse on the gate. Resulting c) $\pm$ polarization state yields d) high ("0") and low ("1") V_{TH} of FeFET

Figure 2. Endurance characteristics of FeFET. The difference between V_{TH+} and V_{TH-} defines the MW of the device. At higher cycle count the MW closes because charge trapping becomes dominant compared to FE switching.

Figure 3. a) Reference pulse and parametrized erase pulse. b) Color intensity graph of erase matrix of woken up device with SiO₂ interface buffer layer. Three sub-regions can be seen: 1) charge trapping region 2) ferroelectric switching region 3) region without ferroelectric switching. The optimum operating conditions can be deduced from such graphs.

Figure 4. Evolution of the MW as a function of pulse width and pulse amplitude (erase matrix) with cycling. The different colors as shown on the right hand side denote the memory window in volts.

Figure 5. Flow chart of the multi-scale simulation framework accounting for the physical phenomena occurring in electron devices. The FE nucleation is selfconsistently coupled with charge trapping in discrete defects together with a Poisson solver.

Figure 6. a) Device structure geometry of the simulated bulk FET with the 9nm thick HfO₂ and 1nm thick interfacial SiO₂ buffer layer. b) Simulated semilogarithmic transfer characteristics. The opposing impact of the ferroelectric switching and charge trapping within the FeFET is illustrated here showing CW hysteresis behavior of the charge trapping (when going from negative to positive voltages and back) and CCW behavior of the FE switching

Figure 7. Measurements and corresponding simulations of a) CV, b) I_G-V_G [9] and c) ΔV_{TH} obtained from the single pulse measurements (see for inset I_D-V_G and $I_D(t)$) of a large gate area FeFET. d) Obtained defect map with sensitivity regions within band gap.

Figure 8. Band diagrams a) @ $\pm 5V$ stress; b) ERS and c) PRG state @ 0V and d) Measured [9] and simulated (solid) leakage evolution during PRG/ERS stressing of the device.

Figure 9. a) Simulated variability and impact of scaling on V_{TH} distribution of the control device with 9nm HfO_2 without FE properties. b) Local field distribution between two devices with high and low V_{TH} , respectively.

Figure 11. a) Local potential changes within the gate stack $SiO_2(IF)/HfO_2$ due to the nucleation of the domain. b) Statistical simulation of the V_{TH} distribution after PRG and ERS of the 30x80 nm FeFET device. Randomization of k-value; Landau parameters. 1 and 2 denote grain 1 and 2. Arrow indicates the shift with inclusion of trapping and degradation.

Figure 13. Simulated a) Band diagrams extracted from the grain 1 and grain 2 (Fig. 12) and b) leakage current in (1) completely (2) partially switched (3) non-switched and (4) non-switched degraded FeFET. PRG state of the FeFET is considered. Different field over the device changes the dynamics of the injection of electrons (and nucleation of domains) along the width of the channel; c) I_D -transient of the degrading FeFET (equivalent to (1)-(4)).

Figure 15. Kinetics of the switching. $I_G(t)$ simulated w/ and w/o presence of the a) CT b) FE switching upon application of the positive V_G . IF trapping (in fresh FeFET) and change the field over the FE: HfO_2 induces switching (1) earlier compared to device w/o trapping (2). Increase of the defect concentration and trapping alters the electric field over the device and pins the domain out (3) closing the MW of the FeFET. c) PRG V_{TH} degradation with time.

Figure 10. Simulated domain dynamic in 2D illustrating the nucleation processes within the device (top view) while setting it into the erase state. a) initial randomly distributed polarization (without applied electric field); b-c) initial coalescence of the domains and nucleation; d) whole device area set into erased-set (negative polarization state).

Figure 12. Impact of the FE properties variation along the channel. a) Geometry of the multigrain FeFET with different switching characteristics along the channel (with indicated 3 grains along the device W (30x80nm FeFET)) and c) MW dependence of the available domain configuration. The worst domain determines the V_{TH} causing the averaging effect.

Figure 14. Simulated switching kinetics of the 3-domain based FeFET depending on its interaction with interface and bulk defects.

Figure 16. Model of the (left) switching kinetics and trapping interplay and (right) degradation processes within the FeFET.