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A wired-AND transistor: Polarity controllable FET with multiple inputs

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Introduction: Reconfigurable field effect transistors (RFET) have the ability to toggle polarity between n- and p-conductance at runtime [1], [2]. The here presented multiple independent gate (MIG) RFET expands the device functionality by offering *additional logical inputs*, valuable for e.g. efficient XOR or majority gate implementations [3], [4] or the here originally presented *multiplexer circuit*. Moreover, for the first time with a top-down RFET approach *equal ON-currents* are obtained for every configuration while requiring *only one supply voltage* (V_{DD}).

Working principle: The presented RFET consists of an intrinsic silicon nanowire channel (**Fig. 1a**). At both ends NiSi₂ is intruded, which has a work function aligned near to the middle of the Si band gap. Each of the resulting Schottky junctions is gated individually (CG1, PG) and additional gates are introduced along the channel (CG2, CG3). The program gate (PG) determines the device's polarity and has the same potential as the corresponding drain (0 V for hole or V_{DD} for electron conductance). If all control gates (CG1-3) are biased equally, the RFET turns ON (**Fig. 3a, b, f, g**). Whenever any or all CGs are biased equally to the source's potential, a potential barrier is formed, switching the RFET OFF (**Fig. 3c-e, h-j**). Hence, the FET works as wired-AND logic gate (**Fig. 6a**).

The fabrication with CMOS compatible processes and materials is based on a 20 nm silicon-on-insulator (SOI) wafer and requires no doping. The nanowire is formed by a reactive ion etch process [5]. By repeated oxidation and HF etching the wire is further rounded and thinned to ca. 60 nm width and 4 nm height. An omega-shaped gate stack of 5 nm SiO₂, and conductive TiN, Ti and Pt surrounds and radially compresses the wire (**Fig. 1b**). Finally, nickel is deposited at both ends of the wire and atomically abrupt and flat NiSi₂ Schottky junctions are formed (**Fig. 1c**).

Performance: The transfer characteristics in **Fig. 4** reveal an ON/OFF ratio of five orders of magnitudes and ON-currents which are equal regardless of the programmed configuration. Additionally, only one supply voltage is needed for gates and drain. Despite its necessity for the use in complementary logic circuits, this symmetry was never achieved before for top-down fabricated RFETs. For NiSi₂ and Si, the Schottky barrier height is slightly lower for holes than for electrons leading to initially asymmetric ON-currents. However, by the influence of the omega gate stressor on the band structure the electron and hole injection through the Schottky barrier can be equalized as demonstrated in **Fig. 2** [6]. **Fig. 4** further shows that the minimum subthreshold swing SS and threshold voltage are lower for the switching with CG2 and CG3 than for all combinations including CG1. This is because CG1 directly controls the inlet at the Schottky junction whereas the other gates only build a conventional channel barrier. Having two efficiently switching gates (CG2+3), as demonstrated for the first time, thus improves the efficiency of RFETs. From **Fig. 5** it can be seen that the gates' voltage determines the shape of the output characteristics. Hole dominated currents rise with retard because the injecting Schottky barrier is still non-transparent for tunneling at $V_D = 0$ V.

Applications of the device reach from camouflage circuits for hardware secure authentication [7] and fine-grained FPGAs [8] over area and power-delay optimized circuits [3], [4] to novel logic synthesis based on majority-inverter graphs [9]. As a graspable and novel example, the presented device can serve as transmission gate (**Fig. 6b**) in a multiplexer (MUX) (**Fig. 6c, d**), which requires program gates at both in- and output. An n -bit MUX can be reduced by every second stage, thus only $(2^{n+2} - 2^i)/3$ transmission gates are required, with $i=1$ for odd and $i=2$ for even numbers of n (with classical CMOS: $2^{n+1} - 2$). For a 4-bit MUX this results in altogether 30% less transistors when considering also the select and program signal inverters and the reduced buffer needs (**Fig. 6e**). Eventually, more gates per transistor can further reduce the transistor count, e.g. for a 5-gate RFET in a 6-bit MUX by even 42%.

- [1] A. Heinzig *et al.*, *Nano Lett.*, vol. 12, no. 1, pp. 119–124, (2012).
- [2] M. D. Marchi *et al.*, in *Electron Devices Meeting (IEDM), 2012 IEEE International*, pp. 8.4.1–8.4.4, (2012).
- [3] P.-E. Gaillardon *et al.*, in *Test Symposium (LATS), 2016 17th Latin-American*, pp. 195–200, (2016).
- [4] J. Trommer *et al.*, in *2016 Design, Automation Test in Europe Conference Exhibition (DATE)*, pp. 169–174, (2016).
- [5] M. Simon *et al.*, *IEEE Trans. Nanotechnol.*, vol. 16, no. 5, pp. 812–819, (2017).
- [6] T. Baldauf *et al.*, *Solid-State Electron.*, vol. 128, pp. 148–154, (2017).
- [7] Y. Bi *et al.*, in *2014 IEEE 23rd Asian Test Symposium*, pp. 342–347, (2014).
- [8] P. E. Gaillardon *et al.*, *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 10, pp. 2187–2197, (2015).
- [9] L. Amaru *et al.*, *Proc. IEEE*, vol. 103, no. 11, pp. 2168–2195, (2015).

Fig. 1. Micrographs of transistors fabricated with the described technology. (a) Top view on 4-gate RFET with labeled gates and contacts. (b) Cross section TEM of an omega gated narrow channel. (c) Length cut (side view) through a nanowire reveals atomically sharp (see inset) and flat NiSi₂/Si Schottky junction at {111} crystal plane.

Fig. 2. (a) Current symmetry adjustment by radial stress as determined by process and device TCAD simulations. (b) Color map of vertical stress share in a simulated wire geometry in cross section view.

Fig. 3. (a, f) Device symbol with ON-state voltage setting and (b-e, g-j) band diagrams including the 4 gates (CG1-3, PG) for different settings. Depending on voltage of PG and the corresponding drain, n (a-e) or p (f-j) configurations are possible. (a, b, f, g) ON-state set for CG1=CG2=CG3=PG. OFF-state reached by switching (green double arrows) with C1 at Schottky junction (c, h) or a middle gate C2 or C3 (d, e, i, j) or a combination of those (not shown).

Fig. 4. Symmetric transfer characteristics for n- and p-configuration with low hysteresis and 5 orders of magnitude ON/OFF ratio. (a) Sweeping to OFF with a single gate C1, C2, or C3 or (b) with a combination of CGs. Smallest subthreshold slopes (SS) for sweeping with CG2 and/or CG3 (bright curves). SS rises when C1 is involved (dark curves).

Fig. 5. Output characteristics with all gates biased identically (some curves <0.1 nA). Retarded rising for 0 V gate bias due to hole-injection blocking Schottky junction for low V_D .

Fig. 6. Circuit application examples. (a) Look-up table of a multiple independent gate RFET as shown in Fig. 3a, f implementing a wired-AND function. For simplicity and the use in Fig. 6b the signal PG is also applied at CG1, here. (b) Schematic layout of a transmission gate with two select signals (S_0 , S_1) and a program signal (P). (c) Circuit symbol of a 2-bit multiplexer built from 4 transmission gates in parallel and (d) corresponding look-up-table. P can be used to switch the output configuration. (e) Number of transistors required for n -bit multiplexers can be reduced when RFETs with 4 or 5 gates instead of classical 1-gate CMOS transistors are used.