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Ferroelectric FETs With 20-nm-Thick HfO₂ Layer for Large Memory Window and High Performance

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Abstract—Hafnium oxide (HfO₂)-based ferroelectric field-effect transistor (FeFET) is an attractive device for nonvolatile memory. However, when compared to the well-established flash devices, the memory window (MW) of FeFETs reported so far is rather limited, which might be an obstacle to practical applications. In this article, we report on FeFETs fabricated in the 28-nm high-*k* metal gate (HKMG) bulk technology with 90 and 80 nm for the channel length and width, respectively, which show a large MW of nearly 3 V. This is achieved by adopting 20-nm-thick HfO₂ films in the gate stack instead of the usually employed 10-nm-thick films. We show that such a thickness increase leads to only a moderate increase of the switching voltages, and to a significantly improved resilience of the memory characteristics upon the parasitic charge trapping. The devices display a good retention at high temperatures and endure more than 10⁵ bipolar cycles, thus supporting this technology for a future generation of FeFET memories.

Index Terms—Ferroelectric field-effect transistor (FeFET), film thickness, hafnium oxide (HfO₂), large memory window (MW).

I. INTRODUCTION

FERROELECTRIC field-effect transistors (FeFETs) based on ferroelectric hafnium oxide (HfO₂) have been recently raising a strong interest for nonvolatile memory applications [1], [2]. This is mainly due to their proven CMOS compatibility, low-power operation, and a great potential for the lateral and vertical gate-stack scaling. In fact, ferroelectric properties in doped HfO₂ have been observed over a wide range of film thicknesses but are generally most pronounced

at a thickness of around 10 nm [3], [4]. For this reason, the recent research on FeFETs has mainly been adopting this film thickness within the gate stack for demonstrating the device functionality and its operation in large memory arrays. However, while the 10-nm-thick FeFETs prove to be fully functional even at ultrascaled nodes [5], they typically have a memory window (MW) ranging from 1 to 1.5 V. Due to parasitics, noise, and disturbs, this value might be further reduced within an active array environment, which, in turn, leads to a significantly degraded read margin [2].

To reduce the impact of parasitic effects on programmed distributions, the intrinsic MW of the FeFET device must be enlarged. In the past, several structural and compositional techniques in FeFETs using classical ferroelectrics have been proposed [6], [7]. Alternatively, theoretical studies [8] suggest that the MW can be approximately expressed as

$$MW = 2 \cdot \alpha \cdot E_C \cdot t_F \quad (1)$$

where E_C is the coercive field, t_F is the thickness of the ferroelectric layer, and α is a parameter that has a weak dependence on the polarization P and the dielectric constant of the ferroelectric ϵ_F . This parameter is generally lower than 1 and can also account for the second-order effects, which reduce the MW. Thus, it can be considered a measure of ideality for a given FeFET. It follows from (1) that the MW could be enlarged by increasing E_C and/or t_F . Since E_C appears to be relatively invariant in hafnia-(zirconia)-based ferroelectrics [9], the increase of t_F remains a viable option. Indeed, through simulations and experiments, past reports have already pointed out the benefits a thicker HfO₂ might have in terms of a larger MW and better performance of FeFETs [10]–[12].

This article presents a FeFET device adopting a 20-nm-thick silicon-doped HfO₂ layer and fabricated in the 28-nm high-*k* metal gate (HKMG) bulk technology. It shows a large MW of up to 3 V. Despite the thicker gate stack, we observe only a slight increase in switching voltage with respect to FeFETs having 10-nm-thick HfO₂, which is explained by a more favorable capacitive voltage divider for the ferroelectric. Moreover, we show a significantly reduced impact of the parasitic charge trapping, which makes the device operative immediately after the write operation, in contrast to the 10-nm-thick FeFETs. Finally, the good data retention at temperatures

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Fig. 1. (a) TEM image of a FeFET having a 20-nm-thick HfO₂ layer, channel length $L = 32$ nm, and channel width $W = 80$ nm. (b) Schematic of a FeFET indicating the composition of the gate stack and the thickness of the ferroelectric (t_F) and interfacial layer (t_{IL}). (c) Pulse scheme for write and read operations. A time delay of 1 s is introduced between write and read. (d) I_D - V_G curves of the programmed (PRG, +5 V, 1 μ s) and erased (ERS, -5 V, 1 μ s) state. The high- V_T and low- V_T values are extracted at the constant drain current $I_T = 0.1 \mu A$ W/L indicated by the dashed line.

as large as 300 °C and relatively high endurance support this device as a promising candidate for future embedded nonvolatile memory solutions.

II. EXPERIMENTAL METHODS

FeFETs considered here were fabricated in the 28-nm-bulk HKMG process flow in a gate-first approach by GlobalFoundries [5]. Fig. 1(a) and (b) shows the TEM cross section of a device having the channel length $L = 32$ nm and a schematic illustration of the FeFET, respectively. The gate stack consists of TiN/Si:HfO₂/SiON layers deposited on the top of the p-doped silicon substrate as follows: a 1.2-nm-thick interfacial nitrided SiO₂ layer (SiON, buffer layer) was grown on the active area. Then, a 20-nm silicon-doped HfO₂ layer was grown from HfCl₄ and SiCl₄ in a water-based atomic layer deposition (ALD) process at 300 °C. The silicon doping necessary to induce ferroelectricity was around 4%. TiN metal gate was formed by physical vapor deposition (PVD) and consequently contacted with polysilicon. The thermal budget for the complete gate-stack reached a maximum temperature of 1050 °C at a spike activation anneal resulting in a fully crystalline Si:HfO₂ ferroelectric layer.

Electrical characterization of the devices was performed with a Keithley 4200-SCS Semiconductor Analyzer with 4225-PMU pulse measurement units. A schematic of write and read operations is shown in Fig. 1(c). The write operation is carried out by applying pulses at the gate while grounding all other terminals. The read operation consisted of sensing the drain current (I_D) by a fast gate voltage (V_G) sweep with a total duration of 100 μ s. Drain voltage was kept at 100 mV. Such a fast read was adopted to avoid parasitic charge trapping during sensing and to avoid disturbs to the stored polarization, which might take place under long (quasi-dc) sweeps. As a consequence, the resolution of the drain current was limited to 10 nA, which, however, is sufficient to extract all the parameters of interest in this article. The read is performed with a delay of 1 s after the write, unless stated differently, which is done to capture the full MW of the device, as will be clear in Section IV. All electrical results in this article are relative to FeFETs having the channel length (L) and width (W) of 90 and 80 nm, respectively. The threshold

TABLE I
COMPARISON OF FEFETs HAVING DIFFERENT HfO₂ THICKNESSES

HfO ₂ thickness (t_F)	10 nm (ref. [5], [27])	20 nm (this work)
Memory window	1 V – 1.5 V	2.5 V – 3 V
PRG/ERS voltage	2.5 V – 5 V	4 V – 6 V
Write endurance	$10^4 - 10^5$ cycles	$10^5 - 10^6$ cycles
Retention (extrap.)	10 years	10 years

voltage (V_T) is extracted at the drain current level $I_T = 0.1 \mu A \cdot W/L$, as illustrated in Fig. 1(d).

III. SWITCHING CHARACTERISTICS

FeFETs undergo a program (PRG) transition from high- V_T to low- V_T state when the applied positive gate voltage V_P exceeds a certain threshold value, for which the voltage drop across the ferroelectric layer is larger than its coercive voltage. Similarly, an erase (ERS) transition from low- V_T to high- V_T state occurs when a sufficiently large negative pulse V_N is applied at the gate. Fig. 1(d) shows the transfer ($I_D - V_G$) curves for the programmed and erased state, which are obtained after applying a positive ($V_P = 5$ V, $t_P = 1 \mu$ s), and a negative ($V_N = -5$ V, $t_P = 1 \mu$ s) pulse, respectively. As a result, the separation between the so obtained low- V_T and high- V_T levels generally ranges between 2.5 and 3 V for these devices. We note that such values are indeed around twice those found for the FeFETs having 10-nm-thick HfO₂, as summarized in Table I. At the same time, these are the largest MW values reported for the HfO₂-based FeFETs so far and clearly confirm the benefit of increasing t_F . Nevertheless, it should be noticed that the ideal MW ≈ 4 V should be obtained from (1), when assuming that $E_C \approx 1$ MV/cm for HfO₂ films [3] and $\alpha = 1$. However, different nonidealities contribute to lower the value of α , including the polycrystalline nature of the ferroelectric film (each of the grains will have a slightly different polarization axis, with a consequently nonuniform influence on the transistor channel), depolarizing effects and charge trapping.

To study the switching performance of the device, the gate pulse excitations depicted in Fig. 2 are adopted. Here, only

Fig. 2. Gate voltage waveforms and the respective switching transitions. (a) ERS: from low- V_T to high- V_T state with reference $V_P = +5$ V. (b) PRG: from high- V_T to low- V_T state with reference $V_N = -5$ V. All pulse durations are $t_P = 1$ μ s. The read operation is performed after each pulse but for simplicity is omitted in the schematic waveform representation.

write pulses are illustrated, whereas the fast read sweeps are performed after each write pulse to assess the resulting V_T level, but for the sake of simplicity are omitted from the schematic waveform representation. Fig. 2(a) shows the switching from low- V_T to high- V_T state, which is explored by progressively increasing the amplitude of the V_N pulse, while keeping the pulse duration constant $t_P = 1$ μ s. It can be observed that the switching sets in starting from $V_N \approx -3.5$ V and is completed at around $V_N \approx -4$ V. Similarly, to reach the full PRG transition to the low- V_T state, it is necessary to apply at least $V_P \approx +5$ V [Fig. 2(b)]. Interestingly, these switching voltages are less than the double of those observed for the FeFETs with $t_F = 10$ nm (Table I). This can be understood by considering the capacitive voltage divider in the gate stack at an applied gate voltage V_G , where the voltage across the ferroelectric is given by [13]

$$V_F = \frac{C_{IS}}{C_{IS} + C_F} \cdot V_G - \frac{P}{C_{IS} + C_F} \quad (2)$$

where P is the polarization of the ferroelectric layer, and C_F and C_{IS} are the capacitances per unit area of the ferroelectric and of the series combination of the SiON interface layer and semiconductor capacitance, respectively. They can be expressed as, $C_F = \epsilon_0 \cdot \epsilon_F / t_F$ and $C_{IS} = \epsilon_0 \cdot \epsilon_{IS} / t_{IS}$, where ϵ_0 and ϵ_F are the vacuum permittivity and dielectric constant of the ferroelectric, respectively; ϵ_{IS} and t_{IS} are the equivalent (lumped) dielectric constant and thickness of C_{IS} . Considering that $V_F = E_F \cdot t_F$, it follows from (2)

$$E_F = \frac{1}{\epsilon_{IS} \cdot t_F + \epsilon_F \cdot t_{IS}} \cdot \left[\epsilon_{IS} \cdot V_G - P(t_F) \cdot \frac{t_{IS}}{\epsilon_0} \right]. \quad (3)$$

As t_F increases, the capacitance ratio C_F / C_{IS} decreases and the denominator in (3) tends to $\epsilon_{IS} \cdot t_F$. Thus, a larger fraction of V_G drops over the ferroelectric for thicker films, which is favorable for switching.

In addition, (3) shows that this trend might be even more pronounced when the concurrent decrease of P is considered. However, although a strong reduction of P at increasing t_F is reported for the HfO₂-based ferroelectrics [3], [14], it is still not clear to which extent this macroscopically observed phenomenon has an impact on nanoscale FeFETs and requires further studies.

It should be noted that the considerations made so far neglect the dependence of the coercive field on the ferroelectric layer thickness. This can be justified by several reports which indeed show that the coercive field in HfO₂-based ferroelectrics remains largely unchanged over a broad range of film thicknesses, as summarized by Migita *et al.* [9].

Fig. 2 also shows that there is an asymmetry between PRG and ERS switching voltages: while -4 V is sufficient to set the device in high- V_T state, $+5$ V is necessary to reach the low- V_T state. This originates from the asymmetric gate stack in FeFETs. In fact, contrarily to symmetric ferroelectric capacitors (e.g., TiN/HfO₂/TiN), which usually display symmetric switching, the ferroelectric layer in our FeFETs is confined between the heterogeneous top and bottom materials, which have different work functions. Besides this, the silicon substrate presents different surface potentials under negative and positive gate pulses (i.e., in accumulation and inversion regime, respectively). All these factors result in asymmetric PRG and ERS switching voltages.

IV. RELIABILITY STUDY

A. Charge Trapping and Retention

It is known that the parasitic charges trapped during the write operation severely reduce the effective MW of the FeFETs having $t_F = 10$ nm [15]. To explore this phenomenon for the devices with $t_F = 20$ nm, a test depicted in Fig. 3(a) is carried out. In contrast to measurements shown in Figs. 1 and 2, where the fast I_D - V_G sweeps were performed with a delay of 1 s after the write [Fig. 1(c)], here, the first I_D - V_G sweep was contiguous to PRG or ERS operation (no time delay). Then, additional reads at increasing delays over the following nine decades in time were performed. In this way, the time-resolved evolution of the transistor V_T can be monitored. Note that this test also corresponds to classical retention measurement. For a direct comparison, a device with $t_F = 10$ nm and having the same W and L was explored as well. The switching voltages of the FeFET with 10- and 20-nm-thick HfO₂ were $V_{SW} \approx 4$ V and $V_{SW} \approx 4.5$ V, respectively, whereas we used $V_P = 4.5$ V and $V_P = 5$ V to program them, respectively. Thus, the programming overdrive for both devices amounted $V_{OV} = 0.5$ V. Fig. 3(b) shows the evolution of the two states for the two device types. A striking difference is observed at the first read out: while the MW is initially absent for the FeFET with $t_F = 10$ nm, the device with $t_F = 20$ nm exhibits a large separation between the two V_T states (MW = 1.7 V). Then, low- V_T gradually decreases for both devices, widening in this way the MW. Once the full MW is reached, the two states remain stable in time. This behavior is well known for the FeFETs with $t_F = 10$ nm [15] and is explained by the trapped electrons, which get injected from the transistor channel during PRG operation and counteract the effect of the ferroelectric polarization charge on V_T .

Fig. 3. (a) Gate voltage waveform for assessing the retention and trapping characteristics. Here, the waveform for tracking the low- V_T state is shown. For tracking the high- V_T state, V_N and V_P are exchanged. “R” stands for read and corresponds to the fast I_D - V_G sweep described in Section II. In contrast to Fig. 1(c), note that the first read is contiguous to the PRG operation. (b) Evolution of the two states monitored over nine decades in time for FeFETs having 10- and 20-nm-thick ferroelectric layers. Since the single read takes 10^{-4} s, this will be the shortest time to be resolved on the x-axis.

Unless a detrapping pulse is applied, the MW is initially zero and is gradually recovered by the spontaneous detrapping of electrons, making the device nonoperative within the first few tens of milliseconds after PRG. On the other hand, although the device with $t_F = 20$ nm suffers from similar trapping mechanisms, its more favorable capacitive divider and large ferroelectric MW turn out to be particularly beneficial at this point. In fact, they prevent the functionality from being completely obstructed by the parasitic charge.

This behavior can be explained as follows: according to (2), the voltage drop over the series combination of the interfacial layer (IL) and the silicon is $V_{IS} = V_G - V_F$. As previously discussed, a thicker HfO_2 is more favorable for switching in that a larger fraction of the applied V_G drops over the ferroelectric, thus reducing V_{IS} . Since the two devices had the same programming overdrive V_{OV} , which largely contributes to charge trapping, a lower portion of V_{OV} will drop over the IL in the FeFET with $t_F = 20$ nm with respect to the one with $t_F = 10$ nm. Assuming that the injected charge is prevalently due to the direct tunneling from the silicon substrate through the IL and that the injection rate is exponentially dependent on the voltage drop over the IL [16], this will result in a significantly lower charge injection in FeFETs with $t_F = 20$ nm under the same V_{OV} .

Nevertheless, although it is desirable to reduce V_{OV} , a small overdrive is usually unavoidable for at least two reasons: first, the switching voltage of a single FeFET shows a cycle-to-cycle spread and a certain programming margin is necessary to ensure complete switching [17]. Second, FeFETs in arrays show distribution of switching voltages, and unless

Fig. 4. (a) Two V_T states as a function of annealing temperature T applied for 1 h. PRG/ERS and read operations are performed at room temperature. (b) ERS switching transition before and after the full sequence of annealing shown in (a).

dedicated programming schemes are adopted, a global programming voltage needs to reach the cell with the highest switching voltage. Therefore, all other cells will experience a certain amount of V_{OV} .

Moreover, this result testifies on the fact that the charge trapping in FeFETs is not a trivial issue and deserves a thorough investigation, including, e.g., transient and charge pumping experiments [18]. These are, namely, important to understand the structural origin of trapping sites, their energy levels as well as the spatial distribution within the gate stack, which is essential for the optimization of the programming conditions.

Nonetheless, Fig. 3(b) illustrates that the FeFET with $t_F = 20$ nm is fully operative immediately after the write operation. This is of great advantage not only for memory but also for other potential FeFET applications, such as artificial neurons [19], in-memory sensors [20], and oscillators [21], where the signal timing is essential and a fast, real-time response is required.

Fig. 3(b) also indicates that the FeFETs show good retention at room temperature once the two states reach their stable values. However, to be qualified for embedded nonvolatile memory, they also need to retain their states at high temperatures. In fact, embedded applications require that the stored states withstand the reflow soldering, for which the devices are subject to controlled heat, usually a few minutes at 260°C [22], [23]. To study the impact of high temperatures on data retention, we programmed/erased the cell and annealed it at a constant temperature $T = 100^\circ\text{C}$ for 1 h. Then, the read operation is performed to assess the resulting V_T value. Program/erase and read operations are carried out at room temperature to avoid the temperature-induced V_T shifts, which are solely related to the physics of the semiconductor [16] and not to the ferroelectric polarization. We repeated the annealing/read process five times, increasing each time the bake temperature by 50°C up to a value of 300°C .

Fig. 4(a) shows the obtained V_T values as a function of temperature. Both low- V_T and high- V_T states show a certain degradation, which results in a reduction of the MW. This can be explained by the thermal depolarization [24], which causes the spontaneous polarization of the ferroelectric to gradually decay as the temperature increases. Nevertheless, the FeFET exhibits an MW of more than 1.1 V even after the last anneal at 300°C , which reveals very strong retention.

Moreover, Fig. 4(b) shows the ERS switching transition, i.e., the V_T versus $|V_N|$ plot resulting from the measurement

Fig. 5. Endurance properties upon PRG/ERS cycling at +5 V/−5 V, with $t_P = 1 \mu\text{s}$. (a) Evolution of $I_D - V_G$ curves with increasing cycles indicated by arrows. Only curves before the collapse of the MW are shown (up to $N = 10^5$). (b) V_T versus cycles. (c) I_D versus cycles. Shaded area delimits the lower current resolution limit.

in Fig. 2(a), before and after the full annealing sequence of Fig. 4(a). It indicates that both the low- V_T and high- V_T states are preserved, confirming that the thermal depolarization effect is not permanent, and the polarization is restored after a new ERS or PRG operation at room temperature [24]. Moreover, Fig. 4(b) shows that the switching voltage is negligibly altered after the annealing. In fact, its slight change is within the switching variability range of these small-area devices, which is caused by the intrinsic stochastic switching of the ferroelectric domains [5], [17]. Furthermore, these observations are in line with the previous reports on the FeFETs having 10-nm-thick HfO_2 [25], which show that the annealing not only shows a negligible impact on switching but also can even have beneficial effects on the FeFET performance. Indeed, both off-chip heating (external heat source, e.g., oven) and on-chip heating (e.g., self-heating or microheaters) can be used to repair the cycling-induced damage and to fully recover the functionality of a degraded device [25].

B. Endurance

Fig. 5 shows the endurance characteristics of the device, which were studied by applying PRG and ERS cycling pulses of +5 and −5 V, respectively, with pulsewidth $t_P = 1 \mu\text{s}$. As evident in Fig. 5(b), low- V_T and high- V_T remain nearly constant within the first 10^3 cycles, after which a gradual degradation of both states sets in. Consequently, the $I_D - V_G$ curves approach each other [indicated by arrows in Fig. 5(a)], reducing in this way the MW. However, an MW of around 0.9 V still remains after 10^5 cycles, which represents a slight improvement with respect to devices with $t_F = 10$ nm (for comparison see [25, Fig. 1(c)]). The final collapse of the MW is attributed to the severe wear out of the SiON interface layer

and to the resulting excessive charge trapping, which hinders further ferroelectric switching [15], [25].

Finally, the distinguishing of the two logic states in large memory arrays is performed by sensing I_D at the bitline by means of a sense amplifier [2]. Thus, it is also important to monitor the endurance in terms of I_D , as shown in Fig. 5(c). By choosing an appropriate sensing voltage V_G [indicated by the dashed vertical line in Fig. 5(a)], a nearly stable $I_{ON}/I_{OFF} > 100$ is observed over the first 10^5 cycles.

V. DISCUSSION

Overall, the encouraging results presented in this article may indicate a new path for improving the memory characteristics of FeFETs. In particular, the FeFETs with a thicker ferroelectric layer may not only be appealing for planar devices but also for the recently proposed 3-D NAND FeFET devices [26]. In fact, such vertical structures are characterized by a serial architecture of densely packed FeFETs, which may, therefore, be additionally affected by the cell-to-cell interferences, as is the case for the corresponding Flash technology. Here, the large MW could be a way to mitigate the impact of variability and parasitics in such structures. Moreover, the increase of programming voltage is not only tolerable but also beneficial to achieve a large enough window for the write inhibit in the NAND string.

In addition, a large MW is particularly attractive for multi-level storage. Again, 3-D FeFETs with a thicker ferroelectric film could be perfect candidates in this regard. In contrast, the planar small-area device presented in this article might not be optimal for this purpose. In fact, Figs. 2 and 4(b) show that the switching transitions are relatively steep and that by repeating the ERS transition experiment with the same set of electrical parameters [Fig. 4(b)], the intermediate V_T states between the nominal low- V_T and high- V_T states are not completely matched. As previously mentioned, this is typical for the small-area devices. The situation is further worsened at higher temperatures, since the MW decreases [Fig. 4(a)]. A way to increase the reproducibility of the intermediate states, which is essential to multilevel storage, could be to increase the area of the planar device, as reported for the case of FeFET-based artificial synapses [28]. However, this would penalize the FeFET integration density. Consequently, 3-D FeFETs, which naturally have a larger area of the ferroelectric yet high integration density, appear to be suitable solutions.

Nevertheless, despite thicker ferroelectric films show promise to improve the performance of FeFETs, there are limitations to be considered as well. For instance, for films deposited with ALD process, a rapid degradation of the polarization hysteresis occurs for thicknesses $t_F > 20$ nm [29]. This was attributed to a large amount of the monoclinic non-ferroelectric phase with increasing t_F , which would, therefore, result in less performant FeFETs. This problem could be solved by interposing thin interlayers within the HfO_2 film (e.g., thin Al_2O_3 layers). Kim *et al.* [30] have shown that this suppresses the continuous grain growth and increases the amount of the orthorhombic ferroelectric phase in capacitor structures, preserving the good hysteresis up to $t_F = 40$ nm. However, this results in an increase of the total coercive voltage and would consequently result in an increase of

the switching voltage in FeFETs. Alternatively, deposition techniques different from ALD could be adopted. It has been recently shown that sputtering pure HfO_2 is an effective way to produce stable ferroelectric films over a wide thickness range [31]. Another limitation coming from thicker films might be an increased difficulty to etch them during the gate patterning. Finally, the dependence between the thickness and the switching voltage in (3) is also a crucial tradeoff in deciding which t_F to adopt.

VI. CONCLUSION

We have experimentally explored the memory characteristics of FeFETs fabricated in the 28-nm HKMG bulk technology, which had a 20-nm-thick ferroelectric HfO_2 layer and compared them to their 10-nm-thick counterparts. The devices display a large MW of up to 3 V and a switching voltage of around 5 V at a pulsewidth of 1 μs . The impact of the parasitic charge trapping on the memory characteristics is substantially reduced, making the device fully operative immediately after the write operation. Moreover, good data retention, which was confirmed up to a temperature of 300 $^\circ\text{C}$, and the cycling endurance of more than 10^5 cycles make these devices promising for future planar and 3-D nonvolatile memory applications.

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