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Multi-functional Hybrid Gating Silicon Nanowire Field-effect Transistors: From Optoelectronics to Neuromorphic Application

DISSERTATION
for obtaining the degree of
DOCTOR OF ENGINEERING (Dr.-Ing.)

submitted by

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Fakultät Maschinenwesen
Technische Universität Dresden

Multifunktionale Hybrid-Gating-Silizium-Nanodraht-Feldeffekttransistoren: Von der Optoelektronik zur neuromorphen Anwendung

Dissertation
Zur Erlangung des wissenschaftlichen Grades
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vorgelegt von

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Quest'opera è dedicata al sole splendente di Milazzo,
그리고 사랑하는 나의 가족들에게 바칩니다.

Abstract

Enormous demands for fast and low-power computing and memory building blocks for consumer electronics, such as smartphones or tablets, have led to the emergence of silicon nanowire transistors a decade ago. Along with the Si-based nanotechnology, the silicon compatible optical and chemical sensing applications have boosted the research on hybrid devices that combine the organic and inorganic materials. Apart from the revolution in the device dimensions, the rapid growth of artificial intelligence in the software industry brunch requires the next generation's computers with the revolutionized hybrid device architecture. Implementing such new devices can effectively perform machine learning tasks without the massive consumption of energy. The hybrid Si nanowire devices have an excellent capability to replace the conventional computing element by providing new functionalities of combined materials to the traditional transistor devices preserving the advantage of CMOS technology.

A goal of this thesis is **to develop functional hybrid Si nanowire-based transistors modulated by the stimuli-dependent gate** to go beyond the current digital building blocks. The hybrid devices converge semiconductor channel and various materials from organic molecules to silicate composite as a gate of the transistor. External stimuli change the electronic state of the gate materials which is transformed to the gate potential of the transistors.

First, this thesis studies the electronic characteristics of the Si nanowire FETs under the optical stimulus. Optical stimulus induces the strong conductance change on bare Si nanowire FETs. Under the light with low power intensity, the transistor shows an unconventional negative photoconductance (NPC) which is dependent on the doping concentration of the nanowire and the wavelength of the incident light. The dopants ions and surface states cause photo-generated hot electrons trapping which restricts conventional photoconductance in the semiconductor.

In the hybrid device, however, the gate material on the Si dioxide layer plays a significant role in the optoelectronic modulation of the FET device. This thesis demonstrates that an organic photochromic material, porphyrin, wrapping around the nanowire channel acts as an optical gate of the Si nanowire transistor. The diffusive property of electrons in the molecular film decides the optical switching dynamics and efficiency.

Further, this thesis introduces new functional gate material, *sol-gel derived ion-doped silicate film*, based on the availability of stimulus-dependent gate modulation. This amorphous and transparent silicate film shows memristive property due to the ionic redistribution in the film under bias condition. Interestingly, the sol-gel film-coated Si nanowire FETs the devices show a double gate effect cooperating with a back gate under light illumination which is due to the channel separation in the fin structure of the nanowire.

In addition, the sol-gel silicate film-coated Si nanowire transistor emulates the neuronal plasticity with pulsed gate stimulation, namely "*neurotransistor*." Because of the mobile ions in the silicate film, the transistor has a short-term memory and mimics membrane potential change of the neuron cell. The neurotransistor could be used as a computing node in the physical neural network for hardware machine learning.

This work demonstrates that the physical properties of the gate material decide the transfer characteristics and time-dependent dynamics of the hybrid Si nanowire transistors. The optical and neuromorphic gate features of the hybrid transistors would accelerate the advancement of an optical or brain-like computing machine.

Kurzfassung

Enorme Anforderungen an schnelle und stromsparende Rechen- und Speicherbausteine für die Unterhaltungselektronik, wie Smartphones oder Tablets, haben vor einem Jahrzehnt zur Entstehung von Silizium-Nanodraht-Transistoren geführt. Zusammen mit der Si-basierten Nanotechnologie haben die siliziumkompatiblen optischen und chemischen Sensoranwendungen die Forschung an hybriden Bauelementen, die organische und anorganische Materialien kombinieren, vorangetrieben. Neben der Revolution in den Geräteabmessungen erfordert das rasante Wachstum der künstlichen Intelligenz im Software-Branchenbrunch die Computer der nächsten Generation mit der revolutionierten hybriden Gerätearchitektur. Durch den Einsatz solcher neuen Geräte können maschinelle Lernaufgaben ohne massiven Energieverbrauch effektiv durchgeführt werden. Die hybriden Si-Nanodraht-Bauelemente haben eine ausgezeichnete Fähigkeit, das herkömmliche Rechenelement zu ersetzen, indem sie den traditionellen Transistorbauelementen neue Funktionalitäten aus kombinierten Materialien bieten und den Vorteil der CMOS-Technologie bewahren.

Ein Ziel dieser Arbeit ist es, funktionelle hybride Si-Nanodraht-basierte Transistoren zu entwickeln, die durch das stimuli-abhängige Gate moduliert werden, um über die aktuellen digitalen Bausteine hinauszugehen. Die hybriden Bauelemente konvergieren Halbleiterkanal und verschiedene Materialien von organischen Molekülen zu Silikatverbundwerkstoffen als Gate des Transistors. Externe Reize verändern den elektronischen Zustand der Gate-Materialien, der in das Gate-Potential der Transistoren umgewandelt wird.

Erstens, diese These untersucht die elektronischen Eigenschaften der Si-Nanodraht-FETs unter dem optischen Reiz. Der optische Reiz induziert die starke Leitwertänderung bei blanken Si-Nanodraht-FETs. Unter dem Licht mit geringer Leistungsintensität zeigt der Transistor eine unkonventionelle negative Photoleitfähigkeit (NPC), die von der Dotierungskonzentration des Nanodrahtes und der Wellenlänge des einfallenden Lichts abhängig ist. Die Dotierstoffe Ionen und Oberflächenzustände verursachen photogenerierte heiße Elektronen, die die konventionelle Photoleitfähigkeit im Halbleiter einschränken.

Im Hybridbauteil spielt jedoch das Gatematerial auf der Si-Dioxid-Schicht eine wesentliche Rolle bei der optoelektronischen Modulation des FET-Bauteils. Diese Arbeit zeigt, dass ein organisches photochromes Material, Porphyrin, das sich um den Nanodrahtkanal wickelt, als optisches Gate des Si-Nanodrahttransistors wirkt. Die Diffusionseigenschaft der Elektronen im Molekularfilm entscheidet über die optische Schaltdynamik und Effizienz.

In dieser Arbeit wird außerdem ein neues funktionelles Gate-Material vorgestellt, ein Sol-Gel-dotierter Silikatfilm, der auf der Verfügbarkeit von stimulierungsabhängiger Gate-Modulation

basiert. Diese amorphe und transparente Silikat-Film zeigt memristive Eigenschaft durch die ionische Umverteilung in den Film unter Bias-Bedingung. Interessanterweise zeigen die mit Sol-Gel beschichteten Si-Nanodraht-FETs einen Doppelgate-Effekt, der durch die Kanaltrennung in der Lamellenstruktur des Nanodrahtes mit einem Hintertor unter Beleuchtung zusammenwirkt.

Darüber hinaus emuliert der mit Sol-Gel-Silikat beschichtete Si-Nanodrahttransistor die neuronale Plastizität mit gepulster Gatestimulation, dem "Neurotransistor". Durch die beweglichen Ionen im Silikatfilm hat der Transistor ein Kurzzeitgedächtnis und imitiert die Membranpotentialänderung der Neuronenzelle. Der Neurotransistor könnte als Rechenknoten im physikalischen neuronalen Netz für das maschinelle Lernen eingesetzt werden.

Diese Arbeit zeigt, dass die physikalischen Eigenschaften des Gatematerials die Übertragungseigenschaften und die zeitabhängige Dynamik der hybriden Si-Nanodrahttransistoren bestimmen. Die optischen und neuromorphen Gate-Eigenschaften der Hybridtransistoren würden die Weiterentwicklung einer optischen oder hirnähnlichen Rechenmaschine beschleunigen.

CONTENTS

ACRONYMS

BOX	Buried Oxide
CMOS	Complementary Metal-oxide-semiconductor
CPU	Central Processing Unit
CVD	Chemical Vapor Deposition
DC	Direct Current
DG	Double Gate
FET	Field-effect Transistor
FinFET	Fin Field-effect Transistor
GNP	Gold Nanoparticle
HOMO	Highest Occupied Molecular Orbital
HR-TEM	High Resolution Transmission Electron Microscopy
ICP-RIE	Inductively Coupled Plasma Reactive Ion Etching
IPA	Isopropanol
ISFET	Ion-sensitive Field-effect Transistor
LCR	Inductance (L), Capacitance (C), Resistance (R)
LED	Light Emitting Diode
LUMO	Highest Unoccupied Molecular Orbital
MIGFET	Multiple Independent Gate Field-effect Transistor
MOS	Metal-oxide-semiconductor
MTMS	Trimethoxymethylsilane
NIR	Near-infrared
NPC	Negative Photoconductance (Photoconductivity)
OOS	Organic-oxide-semiconductor
PECVD	Plasma-enhanced Chemical Vapor Deposition
PPC	Positive Photoconductance
QD	Quantum Dot

SAM	Self-assembled Monolayer
SOI	Silicon on Insulator
SS	Subthreshold Slop
STD	Short-term Depression
STP	Short-term Potentiation
TEOS	Tetraethoxysilane
TLM	Transmission Line Method
TMOS	Tetramethyl Orthosilicate
TPPOH	5,10,15,20-Tetrakis(4-hydroxyphenyl)-21H,23H-porphine
UV	Ultraviolet
UV-Vis	Ultraviolet-visible
XPS	X-ray Photoelectron Spectroscopy
XRD	X-ray Diffraction

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CHAPTER 1
INTRODUCTION

Last 50 years, silicon industry has been dramatically grown based on the needs for metal-oxide-semiconductor (MOS) transistor which is a fundamental element of CPU and memory. Thanks to the development of nanotechnology including lithography and epitaxy, scaling down of the transistors opened the era of 10-nm processing (100 million of transistors per 1 mm^2 of a chip)[1]. The remarkably high integration density allows electronic devices to process a massive amount of data with high speed. The integration technology promoted the invention of *smart devices* (*e.g.*, smartphones or tablets) which can interact with users and other devices. The smart devices are changing our lifestyle and culture to more mobile and connecting. This trend has been expanded to smart system ems such as smart home, smart healthcare or smart grid.

In this circumstances, the Si-based transistors are not only used as a computing element but also operated as detecting elements interacting with the environment, for instance, chemical (bio[2,3] and gas[4]), light[5,6] or thermoelectric[7] sensors. The transistor-based sensors can be directly adaptable to electronic circuits with a wireless connection, so that detected signal could be processed ubiquitously. In the transistors, gate modulation "switches" (digital) or "amplifies" (analog) the channel current. This intrinsic property enables the various sensor applications requiring signal amplification combining with the digital process. A transistor can detect analytes using gate potential fluctuation induced by the charge of target elements. Sensor application was the evolution of transistors that converge various fields across the boundaries of biology, chemistry, and physics beyond the conventional transistor electronics.

Si nanowire, one-dimensional Si-based nanostructured material, is verified as an attractive detector which has high sensitivity based on the large surface area-to-volume ratio and compatible diameter with nanoscale sensing targets like proteins or molecules[8]. Therefore, the Si nanowire field-effect transistor (FET) has emerged as a powerful sensor platform where a small amount of external electrical stimuli like charged bio- or gas molecules around the nanowires causes meaningful conductance change in the nanowire channel. To increase the sensitivity, researchers have developed molecular immobilization technique on the nanowire surface as well.

Interestingly those sensor studies involving the surface technology encouraged the birth of *hybrid nanowire transistors* that combine nanowire with organic materials to carry out distinct functionality which depends on the stimuli (*e.g.*, photodetectors). While the Si nanowire sensors treat the external molecules as a passive material which should be detected, the hybrid transistors exploit the organic molecules as an active material by forming a heterojunction which controls the gate potential of the transistor device.

The transistors as computing elements have targeted extremely high integration density by continuous downscale by Moore's law. The integration technology using conventional transistor structure has successfully improved the computing performance such as speed or memory storage using. However, the smart computing processing various environmental input signals or complex human brain tasks require a new and different paradigm of device architecture. Thus, the *hybrid device* system has an excellent capability to go beyond the conventional computing based on a functional variety of the organic materials. By combining with various functional organic/inorganic materials on the gate of a transistor, it can modulate the transistors using environmental stimuli which generates particular electric reactivity in gate material, also preserving the technological advantage of Si-based transistors.

Another important aspect is that nature inspires the stimuli-dependent hybrid system. All living creatures in nature are analog machines that actively interact with their environment based on sensing and reacting which are controlled by ionic movement at a cellular level. Regarding computing, the binary calculation of the conventional computers is different with nature. Although it would be not simple to mimic the sophistication and elegance of nature, if we need robots or computers that can substitute advanced human

tasks in the near future, the machine that can emulate the natural computer, the brain, would be the best candidate which can understand our nature.

In this thesis, various gate materials from organic molecules, polymers to silicate composite and their systemic functions regarding field-effect affecting the Si nanowire transistor have been studied. In the following of introduction, **Chapter 2** discusses the basic theory of Si nanowire FET. In particular, this chapter describes how gate potential is modulating the channel conductivity using the energy band and potential diagrams, that would be the starting point to develop applications by gate engineering. **Chapter 3** covers the experimental method to fabricate the Si nanowire FETs. Also, film formation as a functional gate material is introduced. The electrical and optical characterization and spectroscopic procedure for the material analysis are followed.

Chapter 4 investigates the optoelectronic modulation of Si nanowire FETs including unconventional negative photoconductivity (NPC). This chapter shows that the light-induced trapped electron causes unconventional conductance change by threshold voltage change. Since photoconductance is the intrinsic effect of the nanowire channel and interface area, it is fundamental to understand the conductivity change of nanowire by external stimuli (cf. light) to take a step forward towards the external gate effect.

Chapter 5 to **Chapter 8** show various types of the external gate using the hybrid material system. In **Chapter 5**, the well-known organic material, porphyrin, is used as the outer shell of the nanowire transistor, acting as an optical gate. This chapter shows not only the optical current switching but also the possibility of optical gate modulation using pure field-effect.

Chapter 6 introduces the sol-gel derived composite materials for gate area. The sol-gel silicate film is used as a gate platform which can be doped with various small elements like ions or molecules. **Chapter 7** shows optical gate property of the sol-gel film-coated Si nanowire FETs under illumination. Interestingly, the devices show a double gate effect with a back gate which is typically shown in the FinFET. In **Chapter 8**, the sol-gel coated Si nanowire transistor shows new hardware opportunities that combine learning and memory functions within one unit cell, similar to a neuron. The device emulates the intrinsic neuronal plasticity and can perform as a computing node in a complex neural network.

Chapter 9 summarizes the thesis with the outlook for future applications.

References

1. Loughran, J. Moore's Law 2017: an uphill battle. *Engineering and Technology* (2017). Available at: https://eandt.theiet.org/content/articles/2017/05/moore-s-law-2017-an-uphill-battle/. (Accessed: 29th November 2017)

2. Shen, M. Y., Li, B. R. & Li, Y. K. Silicon nanowire field-effect-transistor based biosensors: From sensitive to ultra-sensitive. *Biosens. Bioelectron.* (2014). doi:10.1016/j.bios.2014.03.057

3. Baraban, L. *et al.* in *Nanowire Field Effect Transistors: Principles and Applications* 241–278 (Springer New York, 2014). doi:10.1007/978-1-4614-8124-9_10

4. Cao, A., Sudhölter, E. & de Smet, L. Silicon Nanowire-Based Devices for Gas-Phase Sensing. *Sensors* **14,** 245–271 (2013).

5. Miller, D. A. B. Are optical transistors the logical next step? *Nat. Photonics* **4,** 3–5 (2010).

6. Priolo, F., Gregorkiewicz, T., Galli, M. & Krauss, T. F. Silicon nanostructures for photonics and photovoltaics. *Nat. Nanotechnol.* **9,** 19–32 (2014).

7. Choi, J., Jeon, Y., Cho, K. & Kim, S. Field-effect modulation of the thermoelectric characteristics of silicon nanowires on plastic substrates. *Nanotechnology* **27,** 485401 (2016).

8. Cui, Y., Wei, Q., Park, H. & Lieber, C. M. Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species. *Science* **293,** 1289–92 (2001).

9. Yeonghwan Ahn, James Dunning, A. & Park*, J. Scanning Photocurrent Imaging and Electronic Band Studies in Silicon Nanowire Field Effect Transistors. *Nano Lett.* (2005). doi:10.1021/NL050631X

CHAPTER 2
THEORETICAL BACKGROUND: Hybrid gate Si nanowire field-effect transistors

Si nanowire field effect transistors (FETs) have been demonstrated as powerful building blocks for digital computing and sensing applications. Thus, the history and the current definition of Si nanowire FETs are introduced in this chapter. The analytical models of multiple gate transistors are fundamental to develop hybrid gate transistors. Therefore, the distribution of the potential in the Si nanowire, and threshold and subthreshold models in double gate transistor are presented. Finally, the physical concept of a hybrid gate induced by external stimuli is sketched for actual applications in next chapters.

2.1 Si nanowire field-effect transistors

To understand the birth and current state of Si nanowire field-effect transistors (FETs), it is worth noting the history of CMOS technology, since MOSFET (*metal-oxide-semiconductor* FET) is a building block of the CMOS, the backbone of the semiconductor industry. In 1965 Gordon Moore predicted the evolution of the transistor density in a chip, which is known as *Moore's law*. Remarkably, the semiconductor industry has faithfully followed the law for the last 40 years, that the number of transistors on integrated circuits has doubled every two years (Figure 2.1). The semiconductor devices have been evolved to achieve a fast circuit operation by reducing clock speed and parallel processing which can be obtained by reduced gate oxide capacitance and increased number of transistors

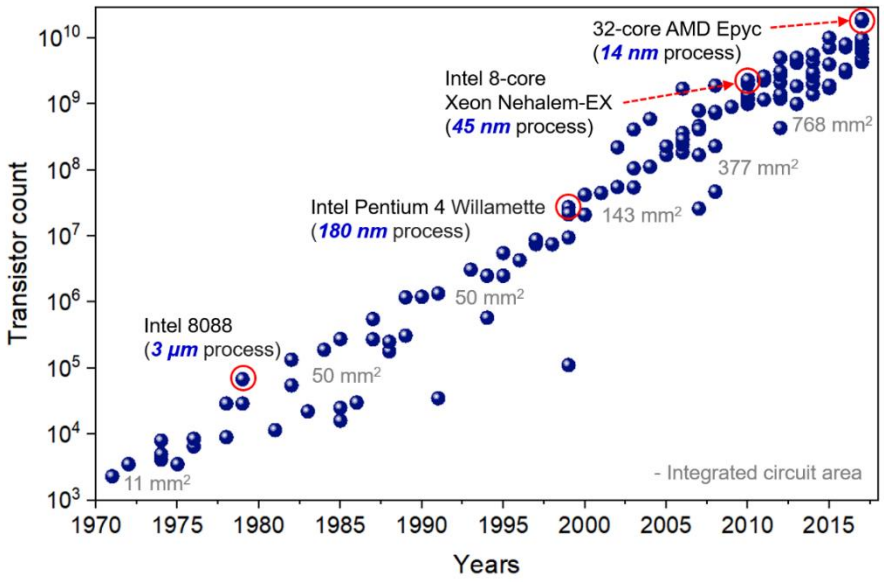


Figure 2.1 Moore's law: The number of transistors on integrated circuit chips. (Data source: http://en.wikipedia.org/wiki/transistor_count)

on a chip. In addition, smaller transistors guarantee lower leakage current by reducing the space charge region in bulk and lower power consumption. These advantages have leaded aggressive scaling down of semiconductor device components.

The integrated circuits in the initial period were built on a Si wafer. At the end of 1990, the invention of SOI (silicon-on-insulator) wafers boosted circuit performance by reducing the parasitic capacitances and enhancing charge transport. Major semiconductor companies like IBM or AMD have manufactured the memory and processor using SOI wafer. In 2010, semiconductor companies began to produce 20 nm gate length transistors, and 10 nm CMOS technology is established in 2017[1].

As the dimension of the devices is reduced to sub-100nm gate length scale, the close distance between the source and the drain generates a number of parasitic effects such as short channel effects[2] that reduce the ability of the gate to control the channel current or random dopants fluctuation[3] from the enhanced atomistic effect in nanoscale devices. To overcome the short channel effect and recover the gate controllability, MOSFETs have evolved from a single planar gate to the multiple-gate structure on the SOI substrate (Figure 2.2). In 1984 the first theoretical paper of double gate (DG) MOSFET was published and showed that SCE is significantly reduced by fully depleted condition obtained by two gate electrodes[4]. The advantage of DG MOSFET was experimentally proven in 1989 using *Delta* (fully depleted lean-channel transistor) structure[5] which was

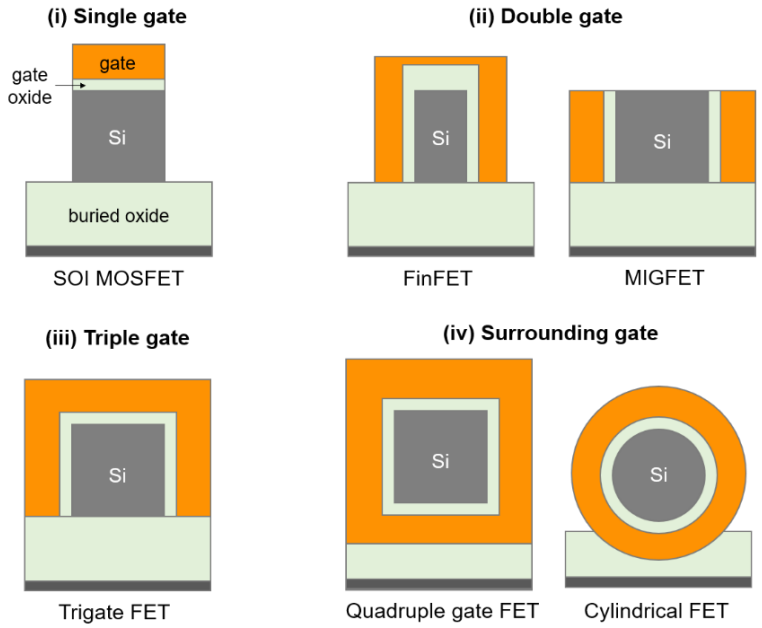


Figure 2.2 Various gate structures.

an initial model of fin-based FET (FinFET) which became main interest in transistor industry after 2000[6]. Further, an advanced structure like multiple independent gate FETs (MIGFET) with non-connected gates were developed[7]. Triple gate MOSFET has an island-like Si channel which is modulated by three sides[8,9]. The theoretically ideal structure is surrounding gate or gate-all-around MOSFET where the gate electrode wraps around all side of the nanowire so that dramatically suppresses short channel effect and its unit channel area is controlled by large gate electrode surface that extensively enhances gate controllability[10]. In the silicon industrial sector, surrounded cylindrical structure, in which diameter of Si channel is below 10 nm, is called *Si nanowire MOSFET*. The downscaling of the transistor enables to fabricate a MOSFET without forming *p-n* junctions at source/drain and the channel region, so-called 'junctionless' nanowire transistor that is turned off by full depletion of nanowire originating from the work function difference between the channel material and the gate electrode[11]. The main purpose of the Si nanowire FET in the industry is to suppress the parasitic effect induced by downscaling, and to enhance the functionality and convenience in the manufacturing of integrated circuits.

In most fields, however, it is called Si nanowire FETs, when the nanowire diameter is in the nanoscale (< 100 or 1000 nm). Bottom-up synthesized nanostructures have been separately studied in the field of physics and material science. Their interest is to

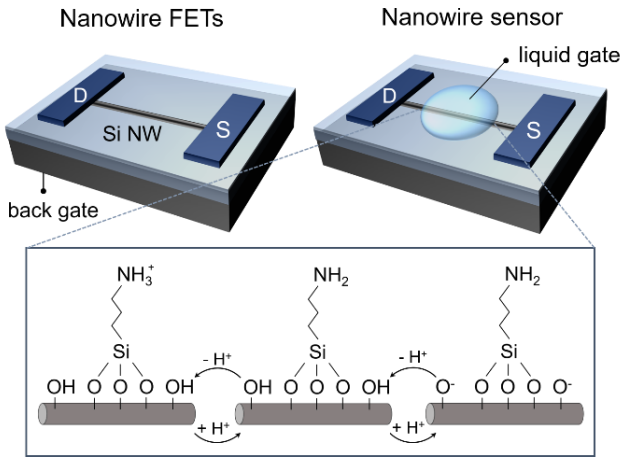


Figure 2.3 The conversion of the Si nanowire FETs to Si nanowire sensor. Figure is adopted from the ref.[14].

understand the physics in the nano-sized materials and to search for novel functionalities using the distinct low dimensional characteristics like quantum effects or ballistic transport. In 2000, Charles M. Lieber published the transistor characteristics of the synthesized *p*- and *n*-type Si nanowire using chemical vapor deposition (CVD) method with 70-150 nm-thick diameter[12]. Further, his group fabricated n^+-*p*-*n* bipolar transistor and CMOS inverter which is modulated by back gate[13]. The nanowire diameter was reduced to 20-50 nm range. In 2001, his group presented a historic result, the first Si nanowire biosensor detecting pH and protein[14] (Figure 2.3). This study has brought up explosive stream of the Si nanowire-based *ion-sensitive* sensor researches[15] which are still ongoing process[16–18]. For ion detection, the solid metal back gate can be substituted with a liquid gate connected to the metal reference electrode, namely ion sensitive FET (ISFET). Most of Si nanowire FET sensors follow the universal principle that channel current is fluctuated by dielectric capacitance change induced from electric charge of detection targets.

It is notable that there are several essential aspects of previous studies about Si nanowire FETs;

(i) Although *bottom-up* transistors have the potential to reduce the cost of fabrication, *top-down* devices are more reliable in electrical performance based on the well-established CMOS process steps on an SOI substrate. However, bottom-up grown nanowires are easily printable on any substrate from SiO_2 to flexible organic films or grids, which is not easy to be performed using the top-down way. Therefore, both regimes are used these days depending on the target application and spec.

(ii) The surface effect becomes critical in the nanowire FETs. The nano-sized material has more surface per unit volume that generate parasitic effects like interfacial trapping or scattering which should be overcome to obtain the best transistor

operation. On the other hand, people exploit the surface effect to enhance the performance of the transistor, for instance, gate all around structure or surface functionalization for sensing applications.

2.2 *The field-effect – gate-induced potential distribution*

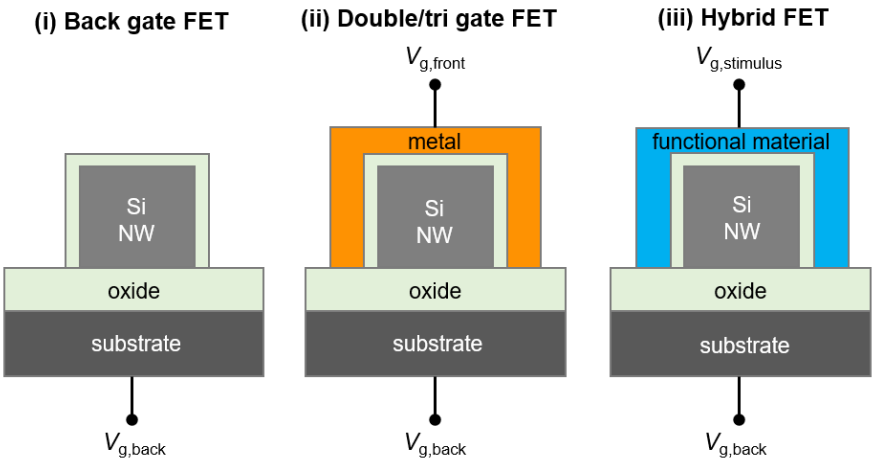


Figure 2.4 Structural evolution of functional gate field-effect transistors.

In the field effect transistor, the variable voltage applied to the *gate* controls the effective cross-sectional area (*e.g.*, depletion or inversion region) of the conducting channel in the nanowire. Because of junctions between channel and source/drain, the current flow is generally blocked in an equilibrium state ($V_g = 0$). However, gate potential (V_g) changes conduction- and valence band bending which modulate the charge carrier distribution on each band. Enough voltage induces the mobile charge carriers which can flow between *source* and *drain*. Therefore, the surface potential modulation of the Si channel determines the current flows and the switching functionality (strong inversion) decided by the threshold voltage (V_{th}).

In the CMOS industry, the back (substrate) gate is not used as a primary gate controller. However, using back gate has an advantage when one creates a 'manual' front gate to obtain complex gate controllability keeping the typical transistor behavior. Figure 2.4 shows several variations of the back-gate FETs. Opened front channel area can be combined with any material from the metal, organic to liquid. For instance, the ISFET for ion sensing is the liquid gate combination and double or tri-gate FinFET structure is one of the combined structure. If functional materials which have particular characteristics

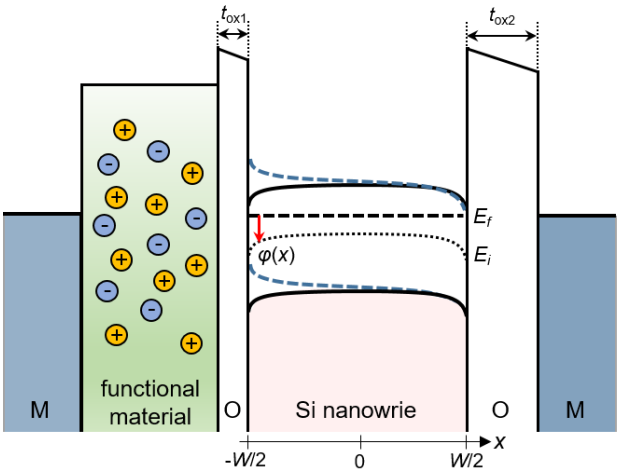


Figure 2.5 Energy band diagram of hybrid Si nanowire FETs with double gate (left: front gate, right: back gate). (M: metal, O: oxide layer, t_{ox}: thickness of the oxide layer, W: thickness of the Si nanowire, E_f: Fermi energy, E_i: intrinsic Fermi energy)

with additional stimuli, are combined with the nanowire, functional hybrid FET can be created for tailored applications. Figure 2.5 shows the band bending of Si nanowire can be modulated by the internal electrical dynamics of the functional material which is a result of the external stimuli like voltage, temperature, light or chemical reactions etc.

Although the gate materials could be varied, the surface potential on the oxide interfacing the nanowire determines the transistor behavior in the devices using the field-effect scheme. The surface potential is induced from Poisson's equation:

$$\frac{d^2\varphi}{dx^2} = \frac{q}{\varepsilon_{si}} n_i e^{q\varphi/kT} \tag{2.1}$$

where q is electric charge, ε_{si} is permittivity of silicon, n_i is intrinsic carrier density and φ is the potential at any point x in the Si nanowire relative to E_i. The boundary condition at $-W/2$ and $W/2$ are different;

$$\varepsilon_{ox} \frac{V_g - \Phi_{ms1} - \varphi_{s1}}{t_{ox1}} = \varepsilon_{Si} \frac{d\varphi}{dx} \Big|_{x=W/2} = -\varepsilon_{Si} \vec{E}_1 \tag{2.2}$$

$$\varepsilon_{ox} \frac{V_g - \Phi_{ms2} - \varphi_{s2}}{t_{ox2}} = \varepsilon_{Si} \frac{d\varphi}{dx} \Big|_{x=-W/2} = -\varepsilon_{Si} \vec{E}_2 \tag{2.3}$$

where Φ_{ms1} and Φ_{ms2} are work function difference between the gates and Si nanowire (here the functional material is not considered), φ_{s1} and φ_{s2} are left and right oxide

interfacial potential respectively, $\vec{E}_1$ and $\vec{E}_2$ are the electric field at the left and the right boundary.

By integrating eqs. (2.1) with the symmetry boundary condition $\frac{d\varphi}{dx}|_{x=0} = 0$, we can obtain

$$\frac{d\varphi}{dx} = -\sqrt{\frac{2kTn_i}{\varepsilon_{si}}\left(e^{\frac{q\varphi}{kT}} - e^{\frac{q\varphi_0}{kT}}\right)} \tag{2.4}$$

where φ_0 is potential when $d\varphi/dx = 0$.

Integrating (2.4) we can obtain the potential distribution as a function of x[19]

$$\varphi(x) - \varphi_0 = -\frac{2kT}{q} \cdot ln\left[cos\left(\sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT}e^{\frac{q\varphi_0}{2kT}}} \cdot x\right)\right]. \tag{2.5}$$

Similarly, in asymmetric boundary condition the symmetry point is moved to x_0 (cf. $\frac{d\varphi}{dx}|_{x=x_0} = 0$). The potential can be obtained from eqs. (2.5)

$$\varphi(x) - \varphi_0 = -\frac{2kT}{q} \cdot ln\left[cos\left(\sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT}e^{\frac{q\varphi_0}{2kT}}} \cdot (x - x_0)\right)\right] \tag{2.6}$$

where $\varphi_0 \equiv \varphi(x = x_0)$.

With very low gate voltages are applied, then it can be approximated as $\frac{d\varphi}{dx} \approx -\vec{E}_0$ which is constant field when the charge inversion ($e^{\frac{q\varphi}{kT}}$) is negligibly small. In this case the internal field is directly calculated by $\varphi_{s1} - \varphi_{s2} \approx -W\vec{E}_0$. Appling these into eqs (2.2) and (2.3), one obtains

$$\vec{E}_0 = \frac{\Phi_{ms1} - \Phi_{ms2}}{W + \frac{\varepsilon_{si}}{\varepsilon_{ox}}(t_{ox1} + t_{ox2})} \tag{2.7}$$

and

$$\varphi(x) = \frac{2kT}{q} \cdot ln\left[\frac{\sqrt{\frac{\varepsilon_{si}}{2kT \cdot n_i}}\vec{E}_0}{sinh\left(\frac{q\vec{E}_0(x - x_0)}{2kT}\right)}\right]. \tag{2.8}$$

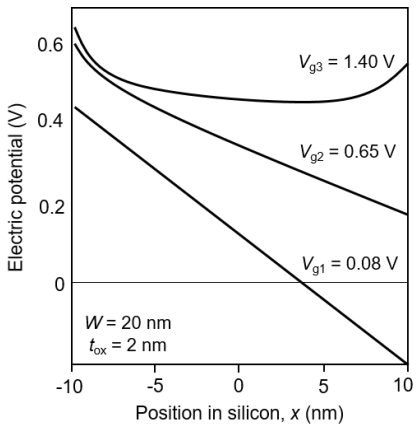


Figure 2.6 Electric potential φ as a function of position in silicon. V_{g1}-V_{g3} are equally applied on each gate. Left and right gates are n^+ and p^+ polysilicon respectively.[20]

Based on the equations above, the potential distribution of the nanowire with the same V_g applied on two different gate electrodes, is shown in Figure 2.6 which is adapted from the analytic study of double gate MOSFET[20]. When the gate bias is big enough, the potential in nanowire has distinct distribution and comparably uniform potential is applied overall nanowire channel which is not shown in the planar MOSFETs. If the gate bias is small, the potential is more affected by work function differences between the gate and the Si channel that makes a linear distribution. This information gives a hint of understanding the charge distribution in the nanowire which is dependent on potential, when multiple gate structure is formed.

One of the important parameters that characterize a switching performance of the transistors is the threshold voltage (V_{th}). The threshold voltage is classically defined by

$$V_{th} = \Phi_{ms} + 2\varphi_f - \frac{Q_d}{C_{ox}} - \frac{Q_i}{C_{ox}} \tag{2.9}$$

where φ_f is the difference between the Fermi level and the intrinsic Fermi level of Si, Q_d is the depletion region charge, Q_i is the oxide and interfacial charge and C_{ox} is gate capacitance. In nanowire devices. However, with low doped ultra-thin nanowire structure, inversion in the channel could be limited when the surface potential is at $2\varphi_f$. Therefore, eqs (2.9) should be modified to

$$V_{th} = \Phi_{ms} + 2\varphi_f - \frac{Q_d}{C_{ox}} - \frac{Q_i}{C_{ox}} + V_{inv} \tag{2.10}$$

where V_{inv} is the additional surface potential needed to induce the inversion charge in the nanowire channel. V_{inv} increases with narrower channel width and lower doping concentration[21]. Similarly, the surface charge in the hybrid devices strongly affects the threshold voltage. Any surface charge change, *e.g.* surface functionalization or stimuli-

induced charge generation in the hybrid gate materials, enhance or suppress V_{th} depending on the sign of the charge. Therefore, eqs (2.9) could be modified with surface charge Q_s:

$$V_{th} = \Phi_{ms} + 2\varphi_f - \frac{Q_d}{C_{ox}} - \frac{Q_i}{C_{ox}} - \frac{Q_s}{C_{ox}}. \tag{2.11}$$

Most of the sensor applications using the Si nanowire transistor use V_{th} shift by ionic charge change on the Si nanowire surface. The dynamics of charge formulation on the Si nanowire surface is directly applied as the surface potential of the nanowire, which must be considered to design hybrid gate devices. In addition, distinct fin-nanostructure and multiple gate modulation are able to generate a channel separation that two separated inversion charge is formed in a nanowire, which will be discussed in **Chapter 7**.

2.3 Subthreshold region: a fingerprint of the gate signal change

Many studies have demonstrated the important role of the subthreshold region of the transfer characteristic, specifically for the detection of the surface charge fluctuation with the highest percentage of conductance change[22,23]. The reason is the subthreshold region current changed exponentially by gate potential change. The exponential increase of current allows the transistor to have (i) switching functionality from off to on current with low power consumption and (ii) amplification of current in this range. Therefore, this sensitive region shows the various information of electric properties of gate area through the slop, the shape (*e.g.* hump), or the off current level etc.

In the classical MOSFET, the subthreshold slop (SS) is represented by

$$\mathrm{SS} = \ln 10 \cdot \frac{\partial V_g}{\partial \ln I_d} \cong \frac{kT}{q} \cdot \ln 10 \cdot \left(1 + \frac{C_d + C_{it}}{C_{ox}}\right) \tag{2.12}$$

where C_d is depletion capacitance and C_{it} is interface trap capacitance. With normal MOSFET with fully depleted thin channel structure with a top gate, the variation of depletion charge by voltage fluctuation is zero, so that $C_d = 0$. If the interfacial trapped charge is zero with a perfect process step,

$$\mathrm{SS} \rightarrow \frac{kT}{q} \cdot \ln 10 = 60\ \mathrm{mV/dec}. \tag{2.13}$$

However, with multiple gate modulation, the back interfacial trap density is not negligible and all capacitance values at front and back should be considered. Figure 2.7 shows a

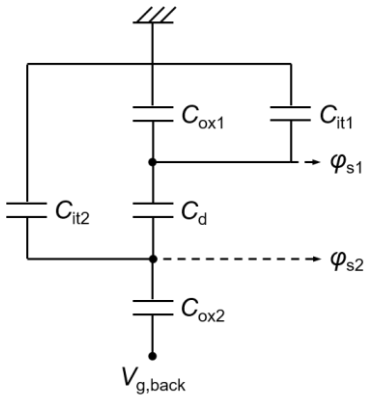


Figure 2.7 Capacitance model of MOSFET structure with back gate control.

capacitance model of back gate control with fixed front gate potential. In this case, SS is induced from the eqs. (2.14) [24]:

$$\frac{\partial \ln I_d}{\partial V_{g,back}} = \frac{1}{I_d} \cdot \frac{\partial I_d}{\partial \varphi_{s2}} \cdot \frac{\partial \varphi_{s2}}{\partial V_{g,back}} \tag{2.14}$$

$$\frac{\partial \varphi_{s2}}{\partial V_{g,back}} = \frac{C_{ox}}{C_{ox2} + C_{it2} + \frac{C_d \cdot (C_{it1} + C_{ox1})}{C_{it,front} + C_{ox1} + C_d}} \tag{2.15}$$

$$\frac{1}{I_d} \cdot \frac{\partial I_d}{\partial \varphi_{s2}} = \frac{kT}{q} - \frac{\frac{1}{t_{si}}\left[1 - \frac{C_d}{C_d + C_{it1} + C_{ox1}}\right]}{\left(\frac{\varphi_{s2} - \varphi_{s1}}{W} + \frac{qN_dW}{2\varepsilon_{si}}\right)} \tag{2.16}$$

where φ_{s1} and φ_{s2} are front and back surface potential of the nanowire channel, W is the thickness of the nanowire channel ε_{si} is the dielectric constanct of the Si and N_d is the doping concentration. Eqs. (2.16) shows that SS is related to the back and front gate potential difference ($\varphi_{s2} - \varphi_{s1}$). The simplest front and back gate potential distribution is shown in Figure 2.8 which is redrawn from the previous study[24]. For back gate modulated devices, the subthreshold current is strongly affected by front gate potential. As front gate potential increases, SS and off current level also increases because high

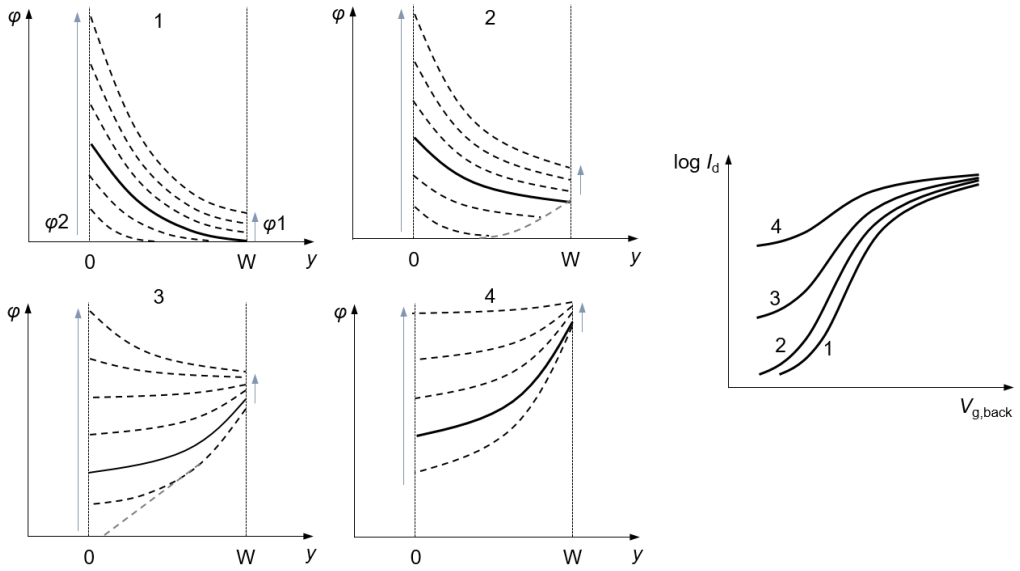


Figure 2.8 Variation of front and back gate potential distribution (1-4, left) and their corresponding transfer characteristics (right).

front gate potential can generate weak inversion in all over the nanowire channel. Therefore, from the subthreshold characteristics, an unknown surface potential could be estimated. This technique is very useful especially for stimulus-induced potential variation in hybrid gate.

2.4 *Hybrid electronic elements with the stimuli-induced gate*

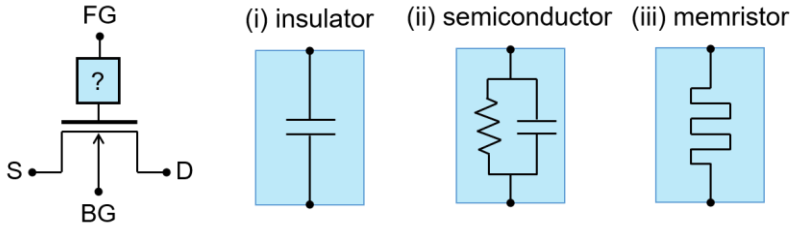


Figure 2.9 Various circuit elements for the hybrid gate.

Previous sections show how the surface potential applied from multiple(double) gates affects the potential distribution in the nanowire, threshold voltage and subthreshold slope. Metal gate without any potential loss was a good starting point to understand the double or multiple gate system in previous sections. The purpose of hybrid electronic devices study is to generate distinct functionality which is induced by both internal electronic property and external stimuli, keeping the transistor characteristics. Since a lot of functional materials are available for the hybrid gate, it is convenient to classify the functional materials as circuit elements. Figure 2.9 shows the simplified transistor circuit with various hybrid gates. Insulators have been used to form a high-κ stack on a transistor to guarantee enough capacitance level even in the strong downscaling. However, using semiconducting or memristive materials for gate modulation would be a new approach to build a single electronic circuit element. Apart from the work function difference between the gate material and the Si nanowire, external stimuli like light or voltage pulses would generate front gate potential and unique dynamics with specific time span in the functional materials. Many existing memory devices are using additional material (*e.g.* high-κ to ferroelectric) on the top of the MOSFET performing 0 or 1 states. However, unique dynamics of various functional materials have the capability to be applied for analog circuits or unconventional application beyond CMOS. In this system, Si nanowire is modulated by physics in the gate materials whether the front gate bias is applied or not.

References

1. Auth, C. *et al.* A 10nm high performance and low-power CMOS technology featuring 3 rd generation FinFET transistors, Self-Aligned Quad Patterning, contact over active gate and cobalt local interconnects. in *2017 IEEE International Electron Devices Meeting (IEDM)* 29.1.1-29.1.4 (IEEE, 2017). doi:10.1109/IEDM.2017.8268472
2. Chaudhry, A. & Kumar, M. J. Controlling Short-Channel Effects in Deep-Submicron SOI MOSFETs for Improved Reliability: A Review. *IEEE Trans. Device Mater. Reliab.* **4,** 99–109 (2004).
3. Asenov, A., Brown, A. R., Davies, J. H., Kaya, S. & Slavcheva, G. Simulation of intrinsic parameter fluctuations in decananometer and nanometer-scale MOSFETs. *IEEE Trans. Electron Devices* **50,** 1837–1852 (2003).
4. Sekigawa, T. & Hayashi, Y. Calculated threshold-voltage characteristics of an XMOS transistor having an additional bottom gate. *Solid. State. Electron.* **27,** 827–828 (1984).
5. Hisamoto, D., Kaga, T., Kawamoto, Y. & Takeda, E. A fully depleted lean-channel transistor (DELTA)-a novel vertical ultra thin SOI MOSFET. in *International Technical Digest on Electron Devices Meeting* 833–836 (IEEE, 1989). doi:10.1109/IEDM.1989.74182
6. Chenming Hu *et al.* FinFET-a self-aligned double-gate MOSFET scalable to 20 nm. *IEEE Trans. Electron Devices* **47,** 2320–2325 (2000).
7. Mathew, L. *et al.* CMOS Vertical Multiple Independent Gate Field Effect Transistor (MIGFET). in *2004 IEEE International SOI Conference (IEEE Cat. No.04CH37573)* 187–189 (IEEE, 2004). doi:10.1109/SOI.2004.1391610
8. Jong-Tae Park & Colinge, J.-P. Multiple-gate SOI MOSFETs: device design guidelines. *IEEE Trans. Electron Devices* **49,** 2222–2229 (2002).
9. Colinge, J.-P. Multiple-gate SOI MOSFETs. *Solid. State. Electron.* **48,** 897–905 (2004).
10. Iwai, H. *et al.* Si nanowire FET and its modeling. *Sci. China Inf. Sci.* **54,** 1004–1011 (2011).
11. Colinge, J.-P. *et al.* Nanowire transistors without junctions. *Nat. Nanotechnol.* **5,** 225–229 (2010).
12. Yi Cui, Xiangfeng Duan, Jiangtao Hu, and & Lieber*, C. M. Doping and Electrical Transport in Silicon Nanowires. (2000). doi:10.1021/JP0009305
13. Cui, Y., Lieber, C. M. & Bawendi, M. G. Functional nanoscale electronic devices assembled using silicon nanowire building blocks. *Science* **291,** 851–3 (2001).
14. Cui, Y., Wei, Q., Park, H. & Lieber, C. M. Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species. *Science* **293,** 1289–92 (2001).
15. Patolsky, F. & Lieber, C. M. Nanowire nanosensors. *Mater. Today* **8,** 20–28 (2005).
16. Zhang, G.-J. & Ning, Y. Silicon nanowire biosensor and its applications in disease

diagnostics: A review. *Anal. Chim. Acta* **749,** 1–15 (2012).

17. Zhang, A., Zheng, G. & Lieber, C. M. Nanowire Field-Effect Transistor Sensors. in 255–275 (Springer, Cham, 2016). doi:10.1007/978-3-319-41981-7_10
18. Dai, X., Zhou, W., Gao, T., Liu, J. & Lieber, C. M. Three-dimensional mapping and regulation of action potential propagation in nanoelectronics-innervated tissues. *Nat. Nanotechnol.* **11,** 776–782 (2016).
19. Yuan Taur. An analytical solution to a double-gate MOSFET with undoped body. *IEEE Electron Device Lett.* **21,** 245–247 (2000).
20. Taur, Y. Analytic solutions of charge and capacitance in symmetric and asymmetric double-gate MOSFETs. *IEEE Trans. Electron Devices* **48,** 2861–2869 (2001).
21. Tahara, Y. & Omura, Y. Empirical Quantitative Modeling of Threshold Voltage of Sub-50-nm Double-Gate Silicon-on-Insulator Metal–Oxide–Semiconductor Field-Effect Transistor. *Jpn. J. Appl. Phys.* **45,** 3074–3078 (2006).
22. Gao, X. P. A., Zheng, G. & Lieber, C. M. Subthreshold regime has the optimal sensitivity for nanowire FET biosensors. *Nano Lett.* **10,** 547–52 (2010).
23. Zörgiebel, F. M. *et al.* Schottky barrier-based silicon nanowire pH sensor with live sensitivity control. *Nano Res.* **7,** 263–271 (2014).
24. Wouters, D. J., Colinge, J.-P. & Maes, H. E. Subthreshold slope in thin-film SOI MOSFETs. *IEEE Trans. Electron Devices* **37,** 2022–2033 (1990).

CHAPTER 3
EXPERIMENTAL METHODS

In this chapter, the experimental methods will be discussed. Two main device fabrication scheme, bottom-up and top-down, will be introduced with details. Also, the hybrid gate formation by various film coating method depending on the device functionality and the material characteristics will be shown. Finally, procedure of electrical and film analysis will be described.

3.1 Fabrication of Si nanowire field-effect transistors

3.1.1 Bottom-up scheme: Schottky-junction Si nanowire FETs

The content of this part is mainly based upon my published article[1].

(i) Si wafer preparation with gold catalysts: A clean Si (100) wafer was prepared using piranha and organic cleaning using acetone and isopropanol, and hydroxyl groups on the surface were activated using air plasma for 20 sec. Poly (diallyl dimethylammonium) chloride (PDDA) was used as stabilizing agent of gold nanoparticles (GNPs) that acts as a catalyst of nanowire growth. PDDA solution (0.5 vol% PDDA and 5 mM NaCl in distilled water) was treated on the Si wafer and 19 nm GNPs were attached to PDDA. O_2 plasma removed PDDA linking that makes equivalent distribution of Au NPs and prevents aggregation of Au NPs.

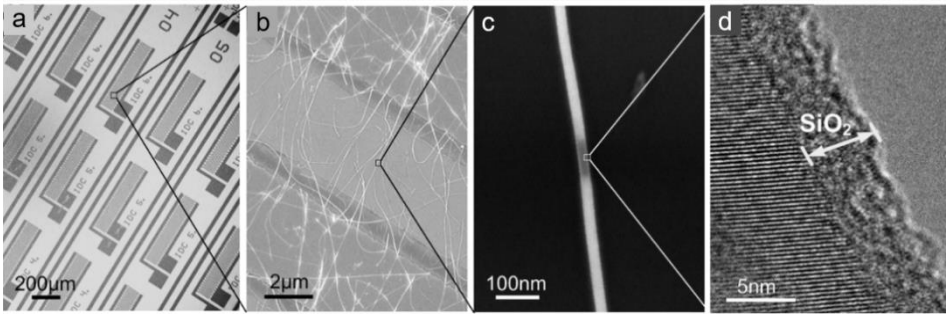


Figure 3.1 Microscopic images of Schottky-barrier Si nanowire FETs. (a) The conformation of the Ni electrode on high density nanowires. (b) Inter- electrode spacing of devices are varied from 6 to 12 µm. (c) $NiSi_2$ formation as Schottky barrier of a nanowire. The brighter part indicates N–Si phases and the dark part of the nanowire is the Si channel. (d) The thickness of the thermally grown oxide wrapping nanowires is around 5 nm.

(ii) Growth of Si nanowire: Si nanowires were synthesized in chemical vapor deposition (CVD) chamber heated at 400°C using silane (SiH_4) gas and hydrogen (H_2) gas as precursors with an inner pressure of 65 mbar for 45 min[2]. The length of grown Si nanowires was around 20-40 µm and the diameter was around 20 nm depending on the size of Au nanoparticles.

(iii) Fabrication of the transistor chip: The contact printing method was used to align the synthesized nanowires in a common direction[3]. The nanowire-growth wafer was put on a SiO_2 wafer for Schottky-barrier FETs with vertical pressure of 100-200 N/cm^2 and moved with constant velocity that provides friction force between nanowires and the SiO_2 wafer. Nanowires are covalently bonded on the interface (Figure 3.1(b)). Dry thermal oxidation was employed to form a thermal oxide layer of 5 nm (Figure 3.1(d)). For the fabrication of Schottky barrier FETs, metal source and drain pads were patterned on the Si nanowires embedded SiO_2 wafer using photolithography process (Figure 3.1(a)). Finally, the sample was annealed at 450 °C in a H_2/N_2 atmosphere for 1 min. Thus nickel diffused along Si nanowires and nickel silicide was formed. Figure 3.1(c) shows well-defined phases of nickel silicide fractions within the single nanowire produced by means of axial diffusion of nickel into the nanowire body[4,5]. The FET devices, consisting of arrays of parallel nanowires, provide reduced device-to-device variability and high source-drain current level as well as high transconductance[5].

This work was conducted by Dr. S. Pregl at NamLab, Dresden. This scheme is used for the organic molecular coated Si nanowire FETs described in **Chapter 5**.

3.1.2 Top-down scheme: n- and p-doped Si nanowire FETs

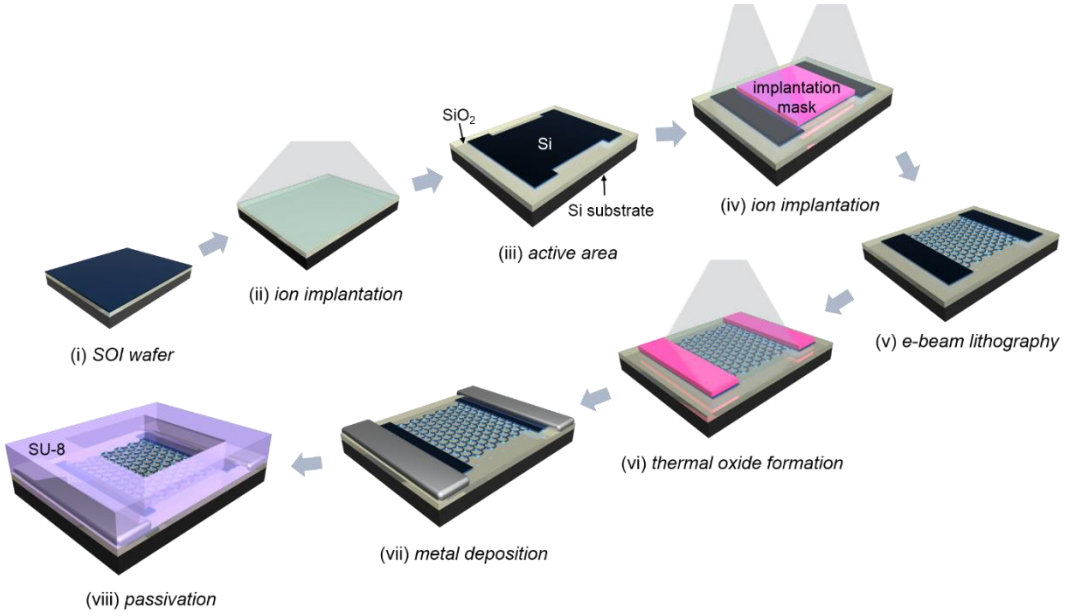


Figure 3.2 The steps of the top-down nanowire device fabrication. A doped SOI wafer (i, ii and iv) is patterned using (iii) photolithography and (v) electron beam lithography depending on the pattern size. After (vi) thermal oxide formation and (vii) metal deposition for the electrodes, (viii)the devices are passivated except nanowire and electrode contact area.

The content of this part is mainly based upon my published article[6].

Si nanowire FETs were fabricated on three 8-inch SOI wafers that consist of a 40 nm-thick top-Si layer (Boron, 10^{16} cm^{-3}), a 400 nm-thick buried oxide layer and the 725 μm-thick p-type Si substrate (Figure 3.2(i)). To implant phosphorus ions in the top Si layer, the 20 nm SiO_2 buffer layer was deposited using plasma enhanced CVD (PECVD) at 300 ℃. After that, phosphorus ions are implanted with an energy of 15 kEV and the concentrations of dopants were 10^{13} cm^{-2} for 10^{18} cm^{-3} and 10^{14} cm^{-2} for 10^{19} cm^{-3} samples (Figure 3.2(ii)). Rapid thermal annealing followed, at 1,000 ℃ for 20s in N_2 atmosphere to activate dopants. Finally, the buffer oxide layer was stripped in 1:100 dHF for 2~3 min. Consequently, one of the wafers has a boron concentration of 10^{16} cm^{-3} and the other two wafers have phosphorus concentration of 10^{18} cm^{-3} and 10^{19} cm^{-3}, respectively.

An active area including the channel, the source and the drain region was defined for electrical isolation of devices using photolithography and inductively coupled plasma reactive ion etching (ICP-RIE) (Figure 3.2(iii)). The source and the drain region were

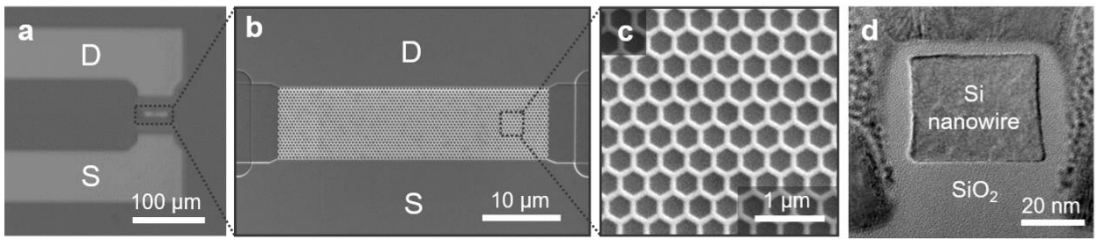


Figure 3.3 Structure of honeycomb Si nanowire FETs. (b) Microscopic image of Si nanowire devices with source and drain transmission line. Scanning electron microscopy (SEM) image of (c) Si nanowire channel area and (d) honeycomb structure of nanowires. (e) Transmission electron microscopy (TEM) image of cross-section of nanowire and thermal SiO_2 layer.

formed using phosphorus ion implantation with a concentration of 5×10^{20} cm^{-3}, and dopant activation followed, using the same recipe above (Figure 3.2(iv)).)). The source and drain area was heavily doped to form ohmic contact (See **Appendix I**). A honeycomb nanowire was patterned on the channel region using electron beam lithography and etched with ICP-RIE (Figure 3.2(v)). The pattern width of the nanowire was 50 nm and the length of the nanowire was 8 μm. (Figure 3.3 (b) and (c)) The final height of nanowire was 30 nm. (Figure 3.3(d)) A 5-nm thick gate oxide layer was grown on the nanowire using a wet oxidation furnace at 850 °C for passivation and post-processing (Figure 3.2(vi) and 3.3(d)). To form the source and the drain electrodes, a 500 nm Ag layer on 50 nm Ti adhesion layer was deposited using an electron-beam evaporator, and liftoff process has followed the deposition steps (Figure 3.2(vii), 3.3(a) and (b)). Finally, the whole wafer area except the nanowire channel region and metal contact pad was passivated with 2 μm thick SU-8 epoxy-based photoresist to protect the long transmission line from undesired contamination (Figure 3.2(viii)).

Figure 3.3 shows the fabricated honeycomb Si nanowire FETs. The Si channel area was heavily doped (10^{18} and 10^{19} cm^{-3}) with phosphorus to modify the channel conduction properties from normal inversion mode *n*-type FETs to accumulation mode *n*-type FETs. Therefore, device is normally in an on-state at gate bias $V_g = 0$ V, which is advantageous for low power sensor applications. As a nanowire channel region, a honeycomb structure was designed (see Figure 3.3(c)) in order to obtain higher signal to noise ratio and higher current stability at the subthreshold voltage regime [7,8]. The source and drain area was heavily doped (10^{20} cm^{-3}) to form ohmic contact with the metal transmission line (Figure 3.3(a)).

The fabrication process of honeycomb structured Si nanowire FET is done by Dr. T. Rim and Dr. K.Kim at NINT of POSTECH in Republic of Korea. This scheme is used for the photoconductance of Si nanowire FETs in **Chapter 4** and for the ion-doped sol-gel film coated Si nanowire FETs in **Chapter 7 and 8**.

3.1.3 Top-down scheme: Top gate fabrication

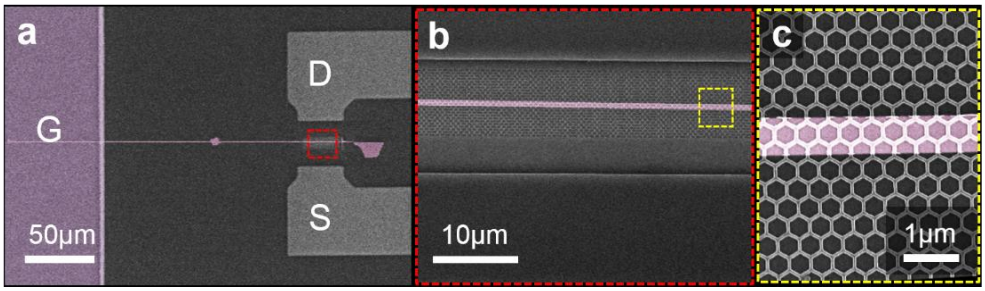


Figure 3.4 SEM images of the top electrode configuration on a honeycomb nanowire device. (a) Top view of the gate electrode on the nanowire FET device with source and drain electrodes. (b) Top gate electrode covers the part of nanowire area. (c) The transparent gate electrode on the honeycomb nanowire structure.

The content of this part is mainly based upon my published article[6].

Top gate electrodes were fabricated by patterning Poly(methyl methacrylate) (PMMA) 950k using electron beam lithography, followed by a lift-off process with sputtered platinum (Figure 3.4). The resist was spin-coated on the honeycomb nanowire devices at a speed of 1000 rpm for 60 s, resulting in a 120 nm thick PMMA film. The top electrode pattern was written by electron beam. Then, the samples were immersed into the H_2O:IPA(isopropanol) (1:3) development solution for 3 min and cleaned in isopropanol. After, a thin chromium adhesion layer (3 nm) was thermally evaporated and a 30 nm platinum layer was sputtered on it. The chip was immersed into acetone for 3 min and treated in ultrasonication for 1-2 min to remove the residual PMMA layer. This protocol allowed connection of the gate electrode to the honeycomb nanowires with a thin Pt electrode with a width of 650 nm which covers approx. 8% of the nanowire area (Figure 3.4(b)). Finally, the sample was annealed in 200 ℃ to reduce the contact resistance.

This scheme is used for the photoconductance of Si nanowire FETs in **Chapter 4**.

3.2 Functional hybrid gate film formation

3.2.1 Organic film formation

Photochromic molecular film

The content of this part is mainly based upon my published article[1].

Nanowire FET chip (in the **section 3.1.1**) is cleaned first with acetone, and then with isopropanol for 5 min respectively to remove organic contaminant. As a final cleaning step, ethanol is used for 5 min. This step helps to regularly spread the ethanol based solution over the chip.

45 µl of 5,10,15,20-Tetrakis(4-hydroxyphenyl)-21H,23H-porphine (Sigma Aldrich) solution based on ethanol and distilled water (95:5) was dropped on a chip with constant area with 1x2 cm^2. The concentration is changed from 10 to 500 µM. Solvent was evaporated overnight (~12 hrs) with high humidity that promotes the formation of a conformal porphyrin layer on all over the surface. Therefore, the porphyrin layer is formed on the 5 nm of thermal oxide on the Si nanowire. Depending on the concentration, the thickness of the porphyrin layer is varied from 2 nm to 12 nm that is discussed in **Chapter 5**.

Organic semiconductor film

The nanowire chips (in the **section 3.1.2**) was cleaned with acetone, isopropanol and ethanol around 5 minutes respectively to remove the organic contaminations on the chips. After this process, the sample was rinsed with the deionized water. The chip was dried using nitrogen gas and baked in vacuum oven at 100°C for 15 minutes to remove the water completely.

Electron transporting copolymer, Poly-{[N,N′-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis-(dicarboximide)-2,6-diyl]-alt-5,5′-(2,2′-bithiophene)} (P(NDI2OD-T2), synthesized by IPF Dresden) was dissolved in trichloroethylene (TCE) solvent with a concentration of 7g/L. The mixture was stirred using magnetic hot plate stirrer at 50°C for 1 hour, then the solution was kept in ultrasonic bath for 15 minutes and shaken by vortex mixer for 15 minutes. Well mixed solution was filtered using 400 nm pore size filter. The resulting solution was spin-coated with an angular speed of 2000 rpm during 60 seconds. The polymer coated sample was annealed using 110 °C hot plate for 1 hour

to eliminate any remaining solvent and to produce a uniform film.

The film formation method in this section is used for the organic molecular coated Si nanowire FETs described in **Chapter 5** and **Appendix A.3.**

3.2.2 Hybrid silicate sol-gel film formation

Firstly, 2.0 x 2.0 cm^2-size nanowire FET chip (in the **section 3.1.2**) was cleaned with acetone, isopropanol and deionized water for 3 minutes to remove existing organic contaminants. Air plasma cleansing was applied to the cleaned chip for 5 seconds to form ultra-hydrophilic surface which guarantees a better adhesion with sol-gel derived film.

1.7 mg of Nikel(II) choloride hexahydrate ($Cl_2Ni{\cdot}6H_2O$) (Sigma Aldrich) and 2.4 mg of Copper(II) chloride dehydrate ($Cl_2Cu{\cdot}2H_2O$) (Sigma Aldrich) were mixed in 467 µl deionized water. 900 µl of Tetramethyl orthosilicate (TMOS) (Sigma Aldrich), 600 µl of Trimethoxymethylsilane (MTMS) (Sigma Aldrich) and 33 µl of 0.1 M HCl were added to metal salt solution. The total concentration of metal ions ($[M]_{tot}$) indicates the sum of equal concentration of two metal salts in the final mixed solvent. ($[M]_{tot} = [Cu^{2+}] + [Ni^{2+}]$ = 10 mM, $[Cu^{2+}] = [Ni^{2+}]$ = 5 mM). Final solvent is filtered by 200 nm pore-size filter to remove unwanted huge particles. 400 µl of the metal ion-sol was spin-coated on the cleaned FET chip with 7000 rpm in 60 sec. The sol-coated chip was dried in a vacuum oven under various temperature from 25℃ to 100℃ (depending on applications) for 24 hours to get a uniform gel-formation.

This scheme is used for the ion-doped sol-gel film coated Si nanowire FETs described in **Chapter 6, 7 and 8**.

3.3 Electrical characterization of FETs

3.3.1 Photocurrent measurement

A 4-channel light emitting diode (LED) driver (DC-4100, Thorlabs) which includes 4 visible LEDs (λ = 405 nm, 470 nm, 530 nm and 625 nm) was used as a visible light source. The controller of DC-4100 controlled the power intensity of light illumination and selected the wavelength. The LED driver was connected to the collimator through liquid waveguide to illuminate the target device area with equivalent light power. The collimator was installed on the hand-made metal dark box with 5 cm-height. Therefore,

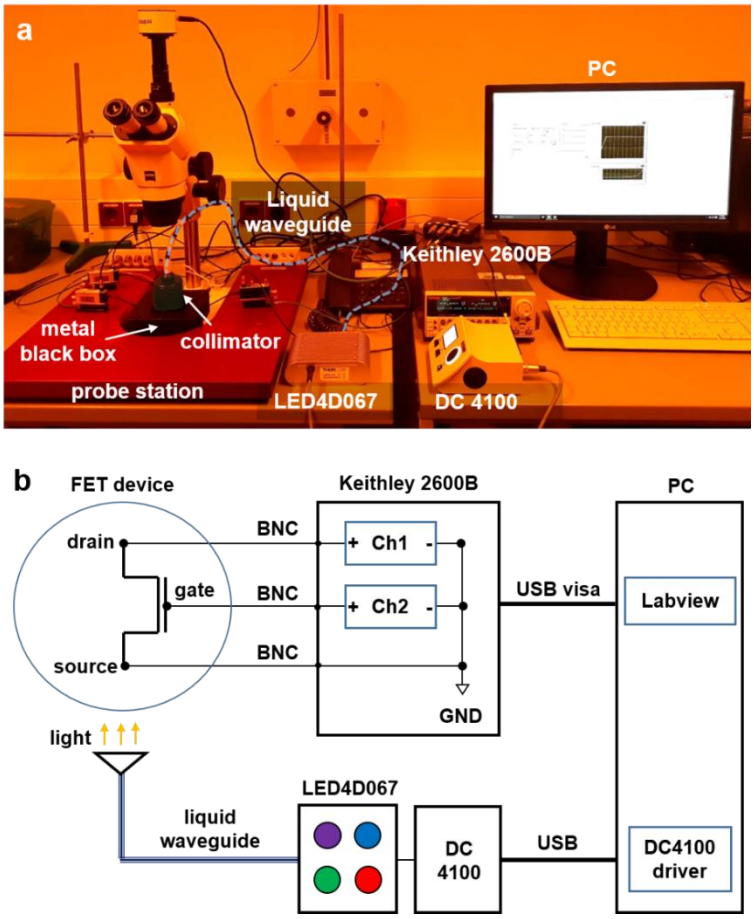


Figure 3.5 (a) Photocurrent measurement setup. (b) block diagram of the measurement setup.

the distance between the light source and the FET sample was fixed as 5 cm. (see Figure 3.5) The bias generation and current measurement of FET devices were performed using Keithley 2600B (source meter in Figure 3.5) at room temperature. The source meter was controlled by manually programed LabView program. This measurement setup is used in **Chapter 4, 5 and 7**.

3.3.2 Electrical measurement

***I-V* measurement**

The electrodes of the devices including field effect transistors or any patterned film are connected to tungsten needles of the micro-manipulators. The voltage and current supply and the current flowing through the devices were measured with Keithley 2604B controlled by Labview program (see the Keithely 2600B connection setup of Figure 3.5(b)). This measurement scheme is used for **Chapter 4, 5, 7 and 8**.

Pulse measurement

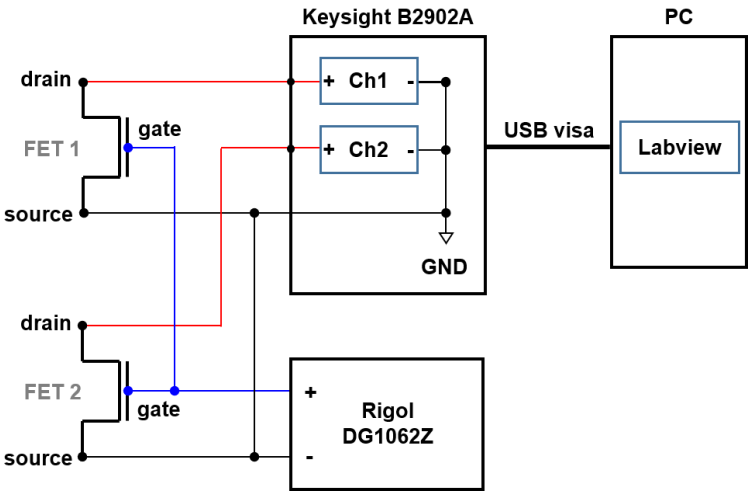


Figure 3.6 Block diagram of pulse measurement setup.

In order to characterize the plasticity behavior of the devices, Keysight B2902A was used as source meter to read the output currents under the modulation of the input pulses generated by the pulse generator, Rigol DG1062Z (Figure 3.6). The current from multiple devices was measured using Labview program. Square pulses are used as input signal with various pulse width and period. This pulse measurement is used in **Chapter 8**.

3.4 Film analysis

In this section, the methods used for the analysis of hybrid sol-gel derived film (described in **section 3.2.2**) and film preparation steps for analysis will be introduced. The tailored modulation of hybrid functional devices relies on the physical and chemical properties of the film. Since the sol-gel film doped with metal ions is an uncommon material for present electronic applications, the careful analysis from various angles were essential to verify the quality of film formation on the surface and to determine the functional purpose of the hybrid devices. The result of the analysis in this section will be discussed in **Chapter 6**.

3.4.1 Capacitance analysis

To measure the capacitance of the sol-gel film, the gold electrode was formed using thermal evaporation. Using a metal shadow mask, patterns with large area (0.5×1.0 mm^2)

of electrodes were deposited on the cleaned SiO_2 wafer with 50 nm thickness (Figure 3.7). The large electrodes are necessary to increase the capacitive signal which has to be measurable by commercial LCR meters. The patterned wafer is cleaned with isopropanol and activated with ozone generator. Then, the sol-gel derived film was coated on the wafer in accordance with the **section 3.2.2**. Second one, top electrode was deposited on the film following same method above.

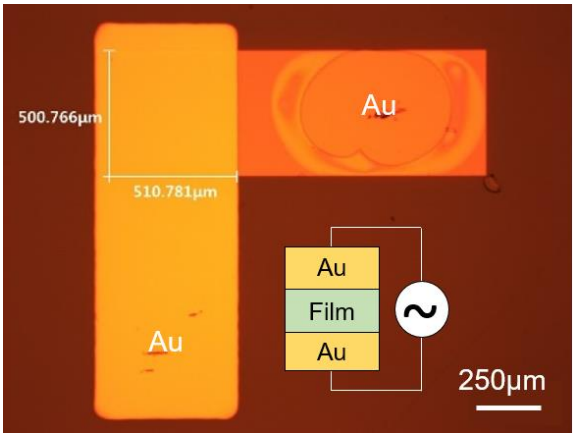


Figure 3.7 Microscopic image of the patterned gold electrodes for capacitance measurement. Overlapped area is used to extract capacitance.

The bottom and top electrode were connected to LCR meter (Agilent E4980A) which is shown in the schematic diagram in Figure 3.6 and the capacitance of the film between two electrodes was measured at various frequencies.

3.4.2 Spectroscopic analysis

To verify the chemical structure including crystallinity and composition of the hybrid sol-gel film in the **section 3.2.2**, X-ray diffraction (XRD) and X-ray photoelectron spectroscopy (XPS) analysis were performed. The film is formed on the SiO_2 wafer surface (see the **section 3.2.2**) dried in different temperature such as 25 °C and 100 °C with and without the present of metal salts. To obtain the absorption spectra of the film, UV-Vis spectroscopy was used. The absorption spectra of the film is distinct from the solution state, because the degree of freedom of molecules is reduced by interference from neighboring molecules in solid state. For UV-vis spectroscopy which exploits transmission of the light through the sample, the transparent glass substrate is used instead of the SiO_2 wafer. The film formation was following the **section 3.2.2**. The sol-gel film samples with and without metal salts were compared.

XRD and UV-Vis spectroscopy were performed in POSTECH, Korea and XPS is analyzed at IFW Dresden, Germany.

References

1. Baek, E. *et al.* Optoelectronic switching of nanowire-based hybrid organic/oxide/ semiconductor field-effect transistors. *Nano Res.* **8,** 1229–1240 (2015).
2. Weber, W. M. *et al.* Silicon nanowires: catalytic growth and electrical characterization. *Phys. status solidi* **243,** 3340–3345 (2006).
3. Weber, W. M. *et al.* Silicon-Nanowire Transistors with Intruded Nickel-Silicide Contacts. *Nano Lett.* **6,** 2660–2666 (2006).
4. Léonard, F. & Talin, A. A. Electrical contacts to one- and two-dimensional nanomaterials. *Nat. Nanotechnol.* **6,** 773–783 (2011).
5. Pregl, S. *et al.* Parallel arrays of Schottky barrier nanowire field effect transistors: Nanoscopic effects for macroscopic current output. *Nano Res.* **6,** 381–388 (2013).
6. Baek, E. *et al.* Negative Photoconductance in Heavily Doped Si Nanowire Field-Effect Transistors. *Nano Lett.* **17,** 6727–6734 (2017).
7. Rim, T. *et al.* Improved Electrical Characteristics of Honeycomb Nanowire ISFETs. *IEEE Electron Device Lett.* **34,** 1059–1061 (2013).
8. Kim, K. *et al.* Suspended honeycomb nanowire ISFETs for improved stiction-free performance. *Nanotechnology* **25,** 345501 (2014).

CHAPTER 4
INTRINSIC OPTICAL GATE: Negative Photoconductance in Si nanowire FETs

In this chapter, negative photoconductance (NPC) in n- and p-doped Si nanowire field-effect transistors (FETs) will be described. In particular, the strong influence of doping concentrations and the energy of visible light are major sources of NPC in the nanowire FETs. The photo-generated hot electrons trapping by dopants ions and interfacial states induces threshold voltage change in the nanowire devices. The transition between negative and positive conventional photoconductance regimes in the nanowire FETs is caused by the competition between the light-induced interfacial trapping and the recombination of carriers. The contents of this chapter is largely based upon my published article[1].

4.1 Photoconductance of Si nanowire

Investigations of the photoconductivity in silicon have a long history[2,3] since optical characteristics of the material is adequate for practical optical and optoelectronic applications. For example, the band gap energy of silicon (1.1 eV) allows Si to be a good photoconductive material under visible to UV illumination. During the last decade, Si and Si nanostructures, especially nanowires, have been studied for various optical applications such as photodetectors[4,5], photovoltaics[6,7] and solar cells[8-9], using advantages from 1-dimensinal structure and relying mostly on the phonon-assisted photoexcitation

due to its indirect bandgap and therefore generating the conventional "*positive*" photocurrent. Also, stable electrical performance of Si (*e.g.*, high speed and efficient signal processing) causes numerous industrial realizations[10] with mature integration technique.

In 2005, photocurrent in an individual Si nanowire field effect transistor (FET) was investigated using optical scanning measurements[11] thanks to the development of nanowire synthesis technique with controllable diameter[12]. This study shows that photocurrent of FETs is depending on *gate bias* as well as light power intensity. The number of photo-excited mobile carriers in the Si nanowire is varied by the local energy band bending which is modulated by gate bias. Currently, in 2016, the highly doped junctionless Si nanowire phototransistor has been investigated[13]. This study shows that the highly doped Si nanowire has high sensitivity of infrared light, which is dependent on the light power. The observed area is mainly *off-current region* in the transfer curve of the transistors where the effect of the gate bias is minimum.

Photoconductive characteristics of Si nanowire FETs

For our investigations, Si nanowire FETs doped with 10^{15} cm^3 of boron (fabrication method is shown in the **Section 3.1.2**) shows conventional positive photoconductivity (Figure 4.1). Light illumination with the light of 405 nm wavelength induces not only the strong transfer curve shift (threshold voltage (V_{th}) shift) towards the direction of current increasing at the same gate bias, but also increase of subthreshold slope (Figure 4.1(a)). The off current ($I_{d,OFF}$) in the dark condition is set as 100 nA with fixed drain and gate bias, which is highly sensitive subthreshold area in various sensing applications[14–16]. Under illumination, drain current (I_d) increases in highly sensitive way to reach a new stable level, $I_{d,ON}$, depending on the light power intensity which is growing from 12.4 to 142 $\mu W/cm^2$ in Figure 4.1(c). The photocurrent of the nanowire device is, in turn, enhanced by the increase of light power intensity (Figure 4.1(d)). Figure 4.1(b) illustrates the photocurrent generation in the nanowire transistors: (1) The light illumination leads the photoexcitation of electrons (2) which leaves electron/hole pairs and (3) the electrons are transferred to electrodes and holes are recombined with other excited electrons in the middle of the nanowire. It has been shown that the strong photocurrent generation in the junction area near electrode due to the energy band bending near electrode[11].

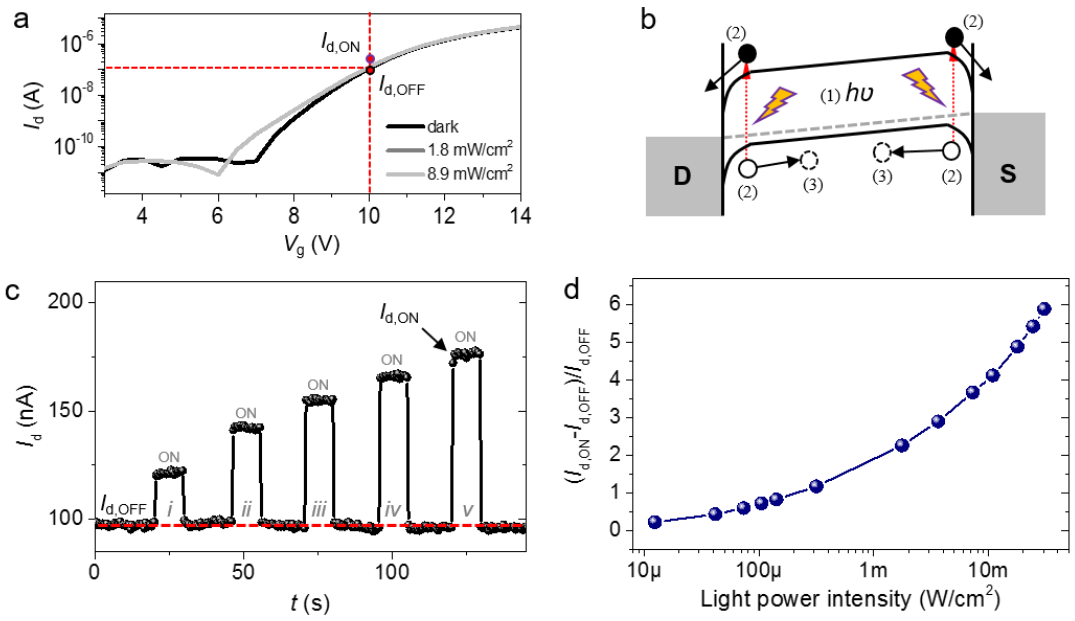


Figure 4.1 Photoconductance of a boron-doped (p-type) Si nanowire FET. (a) Transfer characteristics (Id-Vg curve) of device under LED illumination. (V_d = 0.5 V) (b) Illustration of photo-dinduced electron transition and transfer in the band diagram of Si nanowire device with applied drain potential. (c) Light-induced current switching. The stage *i*-*v* indicates the increasing light power density ((*i*) 12.4, (*ii*) 41.6, (iii) 73.5, (iv) 105, (v) 142 μW/cm^2 respectively). (d) Enhancement of photocurrent switching ratio by increasing light power intensity. (V_d = 0.5 V, V_g = 10 V for (c) and (d). The wavelength of applied LED source is 405 nm.)

In general, nanowires show light-induced current growing. However, the nanowire transistors show the additional featured characteristics which is the light induced degradation (increase) of subthreshold slop (SS). Since the visible light photons has much higher energy (1.9 eV < E_{ph} < 3.06 eV) than the band gap energy of Si (E_g = 1.1 eV), photoexcited electrons become hot electrons in the Si nanowires. In general, hot electrons can create trap states in the oxide layer[17] and these additional trap states increase SS by the following equation,

$$\Delta N_{it} = \left(\frac{C_{ox}}{q}\right)\left[\frac{q\log(e)\Delta SS}{KT} - 1\right] \tag{4.1}$$

where C_{ox} is oxide capacitance, q is elementary charge, K is Boltzmann constant, T is temperature(℃), ΔN_{it} is density change of interface state by light illumination and ΔSS is subthreshold slope change[18]. The subthreshold slope degradation is observed in FET devices by the interface trap creation under light stress[18,19]. This property must be considered in photodetector development using transistors.

4.2 Negative photoconductance in nanostructures

Negative photoconductance (NPC) is a unusual phenomenon since the photoexcitation of charge carriers in materials normally enhances channel conductivity.[29] In order to reach the opposite situation (NPC), one requires a cooperation with additional electrical states that can compensate a generation of photoelectrons. Recently, some of the members in the family of the low dimensional materials (*e.g.*, nanoparticles, nanowires and thin film *etc*.) revealed a reduced photoconductance, due to the surface effects originating from the high surface-to-volume ratio[20,26]. Thus, the large surface area in the nanostructured materials can potentially generate high density of localized energy states acting as traps for the charge carriers, sufficient to reverse the mode of channel conductivity. For instance, conductive array of metal nanoparticles, which is capable of surface plasmon excitations upon light illumination, can reveal NPC, due to the present interfacial charges[20]. On the other hand, NPC in semiconductors has different nature, linked to energy band gap structure. In many cases, the NPC has been observed in large band gap semiconductors such as AlN,[21] *p*-ZnSe[22] or Ga_2O_3[23], with sub-band gap excitation where photoexcited electrons can be captured by extrinsic (*e.g.* surface oxygen) and intrinsic (*e.g.* defects) trap states in the middle of the band gap. Moreover, since super-band gap excitation mostly generates the photoexcited electrons, it requires additional phenomena

Table 4.1 Negative photoconductance observed in different systems and its mechanism

material		dim.	excitation	NPC mechanism	year	ref.
metal	Au nanoparticle	0D	-	plasmonic change by charged SAMs	2009	20
direct semicond.	AlN nanowire	1D	sub-bandgap	hole trapping by surface oxygen	2010	21
	ZnSe nanowire	1D			2011	22
	Ga_2O_3 nanobelt	1D			2011	23
	InN thin film	2D	super-bandgap	scattering by recombination centers	2010	24
	MoS_2 monolayer	2D		increasing effective mass by trion	2014	25
	InAs nanowire	1D		hot-carrier trapping by surface states	2015	26
indirect semicond.	Au-doped Ge	Bulk	sub-bandgap	recombination by positive donor ions	1960	27
	Co-doped Si	Bulk			1966 1971	2 28
	P-doped Si nanowire	1D	super-bandgap	gating effect by hot electron trapping in dopants and interface states	2016	this work

like scattering by recombination center in InN[24] or hot carrier trapping by surface states in InAs[26] to induce the NPC and its optoelectronic nature should be discussed for clear understanding. NPC of bulk Si was observed for the first time from cobalt doped Si under infrared light illumination[2,28]. The localized energy states of dopants in the band gap of Si act as a powerful recombination center, which is typical sub-band gap NPC phenomena. The NPC of various materials in terms of band-gap is listed on Table 4.1.

The well-developed Si photodetectors present at the market and the enormous research and industrial demands of Si nanowires for various optical applications. In particular, modern Si nanowire field effect transistors (FETs) need proper doping in the conduction channel for effective gate modulation and should include insulating layers in contact with the channel area for field effect or surface functionalization for bio-[30-31] or optical[32,33] sensor application. In this situation, the devices are working in more complex electrical systems including the charge transfer via defects and the interfaces. Therefore, NPC studies of Si nanowire devices would be a critical issue, not only for a deeper understanding of the optoelectronic properties of 1-dimensional Si systems, but also for realizing Si-based optical processors which have bilateral switching functionality, preserving the speed of Si in the CMOS technology.

4.3 Negative photoconductance in Si nanowire FETs

Si nanowire FETs with a honeycomb nanowire network were fabricated on an 8-inch SOI wafer using conventional CMOS fabrication technique described in the **Section 3.1.2** (Figure 4.2(a)). The Si channel area was heavily doped with phosphorus to modify the channel conduction properties from normal inversion mode *n*-type FETs to accumulation mode *n*-type FETs. Therefore, device is normally in an on-state at gate bias V_g = 0 V, which is advantageous for low power sensor applications. As a result, the variations of doping concentration were 10^{18} cm^{-3} and 10^{19} cm^{-3} of phosphorus and 10^{16} cm^{-3} of boron respectively. Hereafter, I will use the terms of 'n^+', 'n^{++}' and 'p'-doped device, to designate the abovementioned doping concentrations, respectively. For light illumination, 4 visible light-emitting diodes (LEDs) (wavelengths, λ = 405 nm, 470 nm, 530 nm and 625 nm) were used. By transmission line method (TLM) measurement, it was verified that there is no plasmonic effect by Ag contact under-illumination.

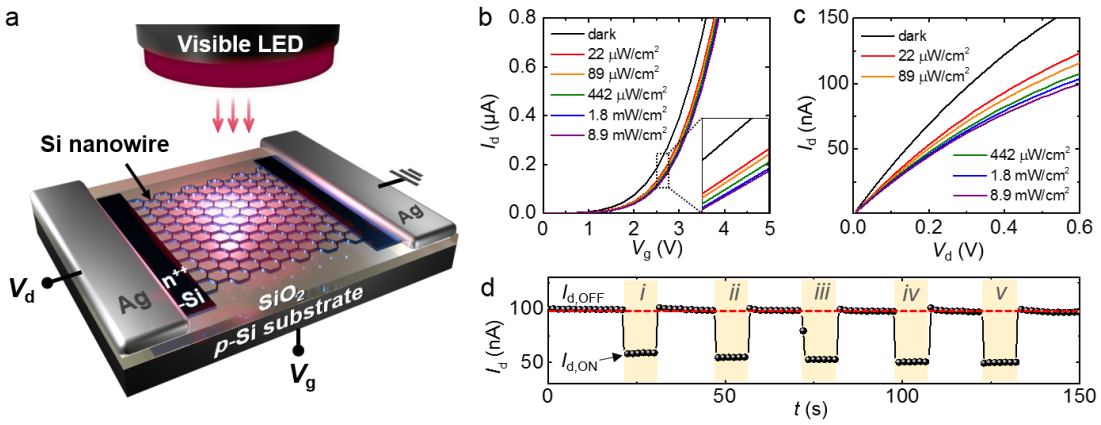


Figure 4.2 Structure and electrical characteristics of honeycomb Si nanowire FETs under illumination. (a) Schematic diagram of the Si nanowire FETs under light illumination. (b) Transfer (I_d-V_g) and (c) output (I_d-V_d) characteristics of an n+-doped nanowire device under illumination ((b) V_d = 0.5 V, (c) V_g = 2.3 V) (d) Photo-induced current switching characteristics on the time domain with increasing light intensity, (i) 0.022, (ii) 0.089, (iii) 0.442, (iv) 1.8, (v) 8.9 mW/cm^2 respectively. (V_d = 0.5 V, V_g = 2 V) λ = 625 nm for (b)-(d).

In the following, the influence of the light illumination on the conductivity of Si nanowire FET devices is demonstrated. Figure 4.2(b) and (c) show the transfer and output characteristics of the n^+-doped ($N_d = 10^{18}$ cm^{-3}) device under illumination of λ = 625 nm with various light power intensities. Interestingly, V_{th} of the device increases under illumination condition which causes a distinct decrease of photocurrent as the illuminated light intensity increases (see inset, Figure 4.2(b)). The output characteristics of the device also supports the clear NPC behavior of Si nanowire FETs (Figure 4.2(c)). Figure 4.2(d) shows reverse switching of I_d under light illumination. The magnitude of light-induced reversed current switching increases (see stages *i*-*v*) as the light intensity increases in the time domain, which also shows the dependence of light intensity in reversed way. Contrary to intuitive expectations that the current should increase due to increasing number of mobile channel carriers by photoexcitation[11], I_d is decreasing when the gate bias and light intensity satisfy certain conditions.

The condition of gate potential that leads to NPC in Si nanowire FETs is shown in Figure 4.3. Figure 4.3(a) shows that the subthreshold slope of devices increases as the light intensity increases. The reason of SS degradation is described in the **Section 4.1**. Therefore, NPC is not able to be observed at very low V_g close to off current level, because

the increased SS by photo-induced hot electrons raises the current at low V_g. For this reason, the NPC is only observed at high enough V_g to cause channel depletion.

In order to determine the dependence between the NPC and the gate bias, current change ratio (ΔI_d (%)) in the light condition from I_d in the dark is extracted from the transfer curve (see Figure 4.3(b)). Under light illumination with very low power intensity (< 400 μW/cm^2), the overall subthreshold area shows strong reduction of current. After the nanowire channel is fully formed ($V_g >> V_{th}$), the NPC is still observed but weaker. As the light power intensity is increasing (> 400 μW/cm^2), the effect of off current increasing in the transfer curve become stronger due to photoexcitation. This raises ΔI_d (%) at low V_g (below V_{th}) and NPC is switched to conventional positive photoconductance (PPC). Therefore, the best area to observe the NPC in FET devices covering wide range of light intensities is the subthreshold area near $V_g = V_{th,dark}$.

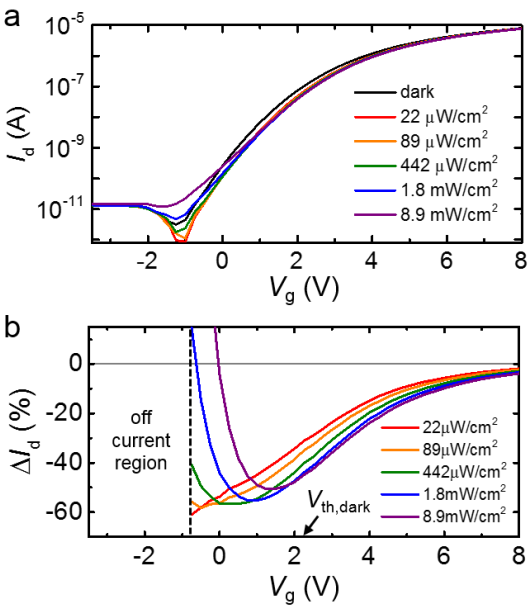


Figure 4.3 The current change depending on gate bias under light illumination (a) Transfer characteristics (log scale) of the n^+-doped Si nanowire FETs upon illumination. (b) The current change ($\Delta I_d(\%) = \frac{I_d(V_g) - I_{d,dark}(V_g)}{I_{d,dark}(V_g)}$) in light condition (λ = 625nm) as a function of V_g.

4.4 Light-induced threshold voltage shift and substrate effect

Since strong NPC was observed near V_{th}, the light-induced threshold voltage shift ($\Delta V_{th} = V_{th,light} - V_{th,dark}$) from the I_d-V_g curve for various doping concentration of nanowires is analyzed (Figure 4.4(a)). Using the constant current method, V_g at I_d = 200 nA was defined as V_{th}. Since V_{th} was changed by illumination, the photoconductance in the FET devices are mainly leaded by V_{th} shift. In Figure 4.4 (b), under low intensity light (< 200 μW/cm^2), all devices show positive ΔV_{th} leading NPC regardless of the doping types. However, the variation of ΔV_{th} with light intensity change is totally different with doping type and concentration. The heavily *n*-doped devices behave with much stronger

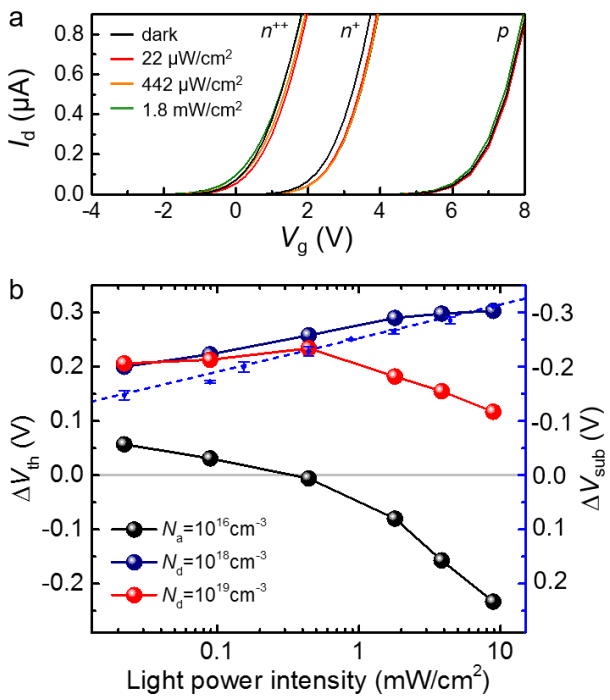


Figure 4.4 (a) Transfer curve shift under illumination of the Si nanowire devices with various doping concentration. (b) Threshold voltage shift (ΔV_{th}) of the devices depending on the light power intensity, which is compared with the substrate potential change (ΔV_{sub}) by illumination (blue dashed line).

NPC than the lightly *p*-doped devices do. For n^+-doped devices, V_{th} increases depending on light intensity, which is a standard NPC behavior. Contrarily, although the n^{++}-doped device shows similar amplitude of NPC with the n^+-doped device at the beginning at lower light intensities illuminating devices, the amplitude of ΔV_{th} decreases with higher light intensities. Finally, weakly *p*-doped devices reveal relatively weak NPC effect at lower intensities of illumination. As light intensity increases, however, PPC behavior, such as the fast decrease of V_{th}, was observed.

In order to demonstrate the main source to lead NPC and PPC by V_{th} shift, a simple equation of V_{th} in FET devices is derived as

$$V_{th} = \Phi_{const.} - \frac{Q_i}{C_{ox}} - \frac{Q_d}{C_{ox}} \quad (4.2)$$

where $\Phi_{const.}$, Q_i, Q_d and C_{ox} imply required potential compensating the working function difference and the channel formation, oxide and interface charge, channel charge in the depletion region and the oxide capacitance respectively. Eq. 2 can be modified to include electrical changes induced by light illumination:

$$V_{th} = \Phi_{const.} - \Delta V_{sub} - \frac{(Q_i+Q_{it})}{C_{ox}} - \frac{(Q_d+Q_{dt})}{C_{ox}} \quad (4.3)$$

where ΔV_{sub} is *substrate potential change* by illumination, Q_{it} is light-induced interfacial trapped charge and Q_{dt} is light-induced dopant-trapped charge. Since the substrate is *p*-type Si, the photogenerated mobile charge can change the interfacial potential. Therefore,

the substrate potential change is measured, which is shown in Figure 4.4 (blue dot line) and the detailed data and method are shown in **Appendix A.3**. Since the amount of ΔV_{sub} is comparable with the amount of ΔV_{th}, the shift of V_{th} in the devices can be leaded by ΔV_{sub} when the light intensity is low. However, still extra ΔV_{th} that is exceeding ΔV_{sub} in the heavily *n*-doped devices could be induced by Q_{it} and Q_{dt}.

For NPC analysis, ΔV_{th} with very low light intensity (< 500 μW/cm^2) that exceeds ΔV_{sub} is considered to be discussed in this section. In order to induce the positive change of V_{th}, (Q_{it} + Q_{dt}) should be negative value. Firstly, Q_{dt} can compensate or strengthen depletion charge (cf. $Q_d < 0$ in the *n*-type devices) depending on the dopants type. In *n*-doped devices, positive donor ions capture electrons ($Q_{dt} < 0$) to increase V_{th}. On the other hand, *p*-doped devices have negative acceptor ions, which capture holes ($Q_{dt} > 0$) to decrease V_{th}. Therefore, *n*-doped devices show an extra increase in V_{th}. Also, Q_{it} would be a negative value since the photoexcited electrons are filled in the defect states, thereby raising the V_{th}. As light intensity gradually increases, Q_{it} and Q_{dt} are strongly affected by recombination rate (discussed later). Therefore, the photoexcited electrons captured by interfacial states and donor ions are the main driving force of NPC in heavily *n*-doped nanowires.

4.5 Doping concentration and light intensity dependence

Figure 4.5 shows the light intensity dependence of the light-induced current change with fixed $I_{d,OFF} \approx 100$ nA, which is chosen to be near to the V_{th} of devices based on the result of Figure 4.3(b). The photocurrent switching with respect to doping concentration and extraction of ΔI_d are shown in Figure 4.5(a). I_d near V_{th} decreases upon the illumination, so that $\Delta I_d < 0$, *i.e.*, NPC, where $\Delta I_d = \frac{I_{d,ON} - I_{d,OFF}}{I_{d,OFF}}$ x 100 (%). It is notable that the heavily *n*-doped devices show reverse change of the photocurrent, mainly from the V_{th} change as discussed before. In Figure 4.5(b), ΔI_d gradually increases with increasing light intensity because of the photoexcitation of electrons in the nanowires. With equal change of light intensity, however, the lightly *p*-doped devices show strong PPC behavior. This figure clearly shows the main differences between doping types. The PPC is strongly disturbed in the heavily *n*-doped devices. The inset of Figure 4.5(b) shows a detail variation of the current with light intensity in a logarithmic scale. In the heavily *n*-doped devices, ΔI_d

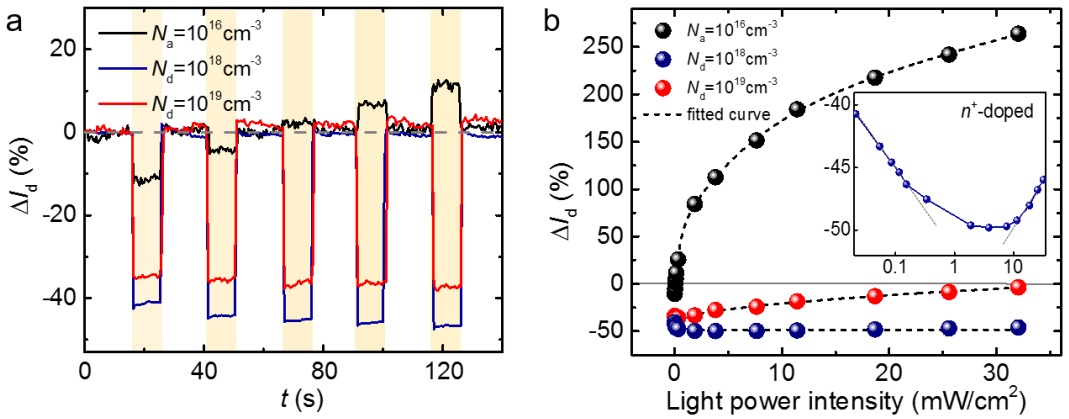


Figure 4.5 Photocurrent change of the devices with various doping concentration. (a) Current change (ΔI_d) upon illumination for various doping concentration. The illuminated light power density in the shaded area was increasing with time with the order of 21, 54, 86, 116, 153 μW/cm^2 respectively. The current drift factor was removed by current normalization. (b) Photocurrent change depending on light power intensity. The data points of (b) is extracted from the average current level in the light and dark condition of (a). The inset graph is photocurrent change vs. light power intensity in a logarithmic scale, which shows exponential reduction of current at low light intensity (< 1 mW/cm^2). The grey lines are fitted curves. (λ = 625 nm)

decreases exponentially with light intensity and at some point, ΔI_d begins to increase, even though ΔI_d is still a negative value. It implies that net ΔI_d is a sum of exponential decay and growth of current with light intensity change.

NPC without substrate effect

In order to verify the NPC in the nanowires *without substrate effect*, a top gate electrode is fabricated on the nanowires, shown in Figure 4.6 (a). The thin platinum electrode was formed on the middle of the honeycomb nanowire array covered with oxide gate dielectric. Pt is chosen to protect the nanowire from any additional optical effects like surface plasmonic effects in the range of visible light. The back gate was floating in order to electrically isolate the nanowire from the substrate. The fabrication steps are shown in Method.

Figure 4.6(b) shows the photo-induced current change with various light intensities. Even when the substrate effect is eliminated, the photocurrent is reduced with low light intensity. The current change ratio in the top-gate device is much smaller than that in the back gate devices due to the absence of the strong potential drop. Like the inset of Figure

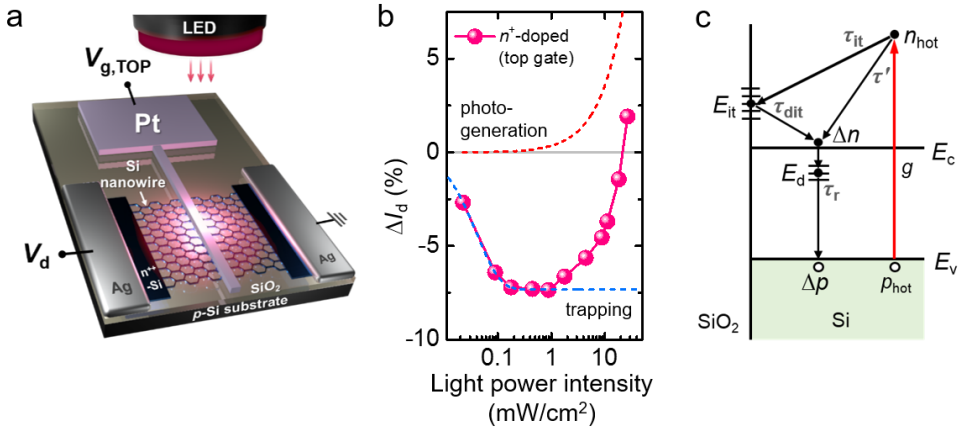


Figure 4.6 Negative photoconductivity of the Si nanowire device without substrate effect. (a) Schematic diagram of Si nanowire FETs with top platinum electrode. (b) Photocurrent change of the n^+-doped top gate devices depending on light power intensity. The dark current level was 100 nA. ($\lambda = 625$ nm) The dashed lines are fitted curves. (c) The schematic energy band diagram of Si and SiO_2 interface explaining the hot carrier generation by light illumination, interfacial trapping and release of excess electrons and recombination process via defect states.

4.5(b), ΔI_d of the top-gate device also decreases in low intensity light and increases as the light intensity increases. ΔI_d is attributed to the combination of two major phenomena such as carrier trapping and photogeneration that are inducing NPC and PPC respectively.

Figure 4.6(c) shows the energy band diagram of Si and SiO_2 interface that describes the physical origin of the NPC and PPC. When photons are absorbed by Si, electron-hole pairs are created with optical generation rate g. Due to the high energy of visible photons, hot electrons are generated in the conduction band with a density of n_{hot}, remaining hot holes, p_{hot} in the valence band. Mobile hot electrons can thermally transit to interface states, E_{it} and conduction band edge with transit time constant τ_{it} and τ' respectively. The density change of electrons at the conduction band edge, Δn, is combining the thermally relaxed hot electrons and the detrapped electrons from interface states with the detrapping time constant, τ_{dit}. The electrons in the conduction band edge are recombined with the holes in the valence band edge, Δp. Since Si is an indirect band gap semiconductor, the recombination process must involve the defect states transition in the band gap with the recombination time constant τ_r.

In order to understand the effect of interfacial trapping on the photoconductance change of the devices, the differential equations of dynamics of the photoexcited carrier density change is developed:

$$\frac{dn_{hot}}{dt} = g - \frac{n_{hot}}{\tau_{it}}\left[1 - \frac{n_{it}}{N_{it}}\right] - \frac{n_{hot}}{\tau'} \tag{4.4}$$

$$\frac{dn_{it}}{dt} = \frac{n_{hot}}{\tau_{it}}\left[1 - \frac{n_{it}}{N_{it}}\right] - \frac{n_{it}}{\tau_{dit}} \tag{4.5}$$

$$\frac{d\Delta n}{dt} = \frac{n_{hot}}{\tau_{it}} + \frac{n_{it}}{\tau_{dit}} - \frac{\Delta p}{\tau_r} \tag{4.6}$$

$$\frac{d\Delta p}{dt} = \frac{p_{hot}}{\tau'} - \frac{\Delta p}{\tau_r} \tag{4.7}$$

$$\frac{dp_{hot}}{dt} = g - \frac{p_{hot}}{\tau'} \tag{4.8}$$

where n_{it} is interface trapped electrons and N_{it} is interface state density. The photoconductivity change can be expressed with excess mobile carriers under illumination:

$$\Delta\sigma = q\mu_{\mathrm{n}}(n_{\mathrm{hot}} + \Delta n) + q\mu_{\mathrm{p}}(p_{\mathrm{hot}} + \Delta p) \tag{4.9}$$

where μ_{n} and μ_{p} are the mobility of electrons and holes respectively[26].

In the steady state, the solutions of the Eqs (4)-(8) depending on the interface trapped electrons are obtained and applied to eqs (9). If light intensity is very low, then most interface trap states are empty ($n_{\mathrm{it}} << N_{\mathrm{it}}$). Therefore, $\Delta\sigma$ is expressed as,

$$\Delta\sigma \approx q\mu_{\mathrm{n}}g\left[\tau_{\mathrm{r}} - \frac{\tau'\tau_{\mathrm{dit}}}{\tau_{\mathrm{it}}}\right] = q\mu_{\mathrm{n}}g[\tau_{\mathrm{r}} - \tau_{\mathrm{b}}] \tag{4.10}$$

where $\tau_{\mathrm{b}} = \frac{\tau'\tau_{\mathrm{dit}}}{\tau_{\mathrm{it}}}$ [26]. Since electrons are majority carriers in *n*-type FETs and the mobility of electrons is much higher than that of holes, the excess electron density in the conduction band is the critical component contributing to the light-induced conductivity change in the nanowire.

If $\tau_{\mathrm{r}} < \tau_{\mathrm{b}}$, then $\Delta\sigma < 0$ under illumination, which implies the NPC. From Table 4.2, estimated τ_{b} is in a range of 10 μs to 10 ms. Therefore, τ_{r} of each heavily *n*-doped devices (both n^{+} and n^{++}) (≤ 1 μs) is much less than τ_{b}, which agrees with the NPC behavior of heavily *n*-doped devices in our results in

Table 4.2 Experimental values of carrier life time in doped Si

parameter		life time	ref.
τ_{dit}		0.01 - 1 s	34
τ_{it}		0.1 - 1 ns	
τ'		1 ps (at R.T.)	35
τ_r	$N_{\mathrm{d}} = 10^{19}\,\mathrm{cm}^{-3}$	0.1 μs	36
	$N_{\mathrm{d}} = 10^{18}\,\mathrm{cm}^{-3}$	1 μs	
	$N_{\mathrm{a}} = 10^{16}\,\mathrm{cm}^{-3}$	100 μs	37

Figure 4.5(b) and 4.6(b). It implies that the electron trapping by the oxide interfacial layer is more preferable than electrons staying at the conduction band edge, and that it limits the mobile carrier density. On the other hand, $\Delta\sigma$ of the *p*-doped device could be a weak negative or a positive value depending on the interface trapping and detrapping time constants, which could possibly induce the weak NPC or the PPC in the nanowire device. This estimation agrees with the strong increase of ΔI_{d} and opposite trend of ΔV_{th} of the *p*-doped device under weak light illumination in Figure 4.5.

On the other hand, if the light intensity is increasing, then the interface states are fully filled with photoexcited electrons, *i.e.*, $n_{\mathrm{it}} \approx N_{\mathrm{it}}$. From this, the channel conductivity is approximated as,

$$\Delta\sigma \approx q\mu_{\mathrm{n}}(g\tau_{\mathrm{r}} - N_{\mathrm{it}}) \tag{4.11}$$

The derivation of all formulas is described in the previous study for hot carrier trapping induced NPC[26]. Firstly, $\Delta\sigma$ could positively increase proportional to g and τ_{r} when the product overcomes the constant negative component, N_{it}, inducing PPC component. As a result, NPC is limited and the current is growing with high light intensity, which agrees with the tendency of current growth as increasing intensity. Secondly, there is a competition between g and τ_{r} depending on doping concentration. As doping concentration increases, g increases and τ_{r} decreases. Therefore, the strong PPC in the *p*-doped device is obvious because of the large τ_{r}. Meanwhile, the PPC of in the heavily *n*-doped devices is not straightforward with doping concentration, due to the larger generation rate of heavier n^{++}-doped device in spite of shorter τ_{r}. Consequently, the n^{++}-doped device shows stronger PPC component than the n^{+}-doped device does in Figure 4.5(b).

4.6 Wavelength dependence

Figure 4.7(a) shows wavelength dependence of NPC in the n^{+}-doped device upon visible light illumination. With low light intensity (0.1 mW/cm^2), the NPC is linearly dependent on the wavelength. It follows the generation rate, which is an inverse function of the energy of a photon ($g = \alpha I_{\mathrm{ph}}/E_{\mathrm{ph}}$, where I_{ph} and E_{ph} are light intensity and photon energy respectively). However, with strong light intensity (10 mW/cm^2), only red light (λ = 625 nm) keeps ΔI_{d} decreasing, whereas the other spectra cause ΔI_{d} to increase. It implies that

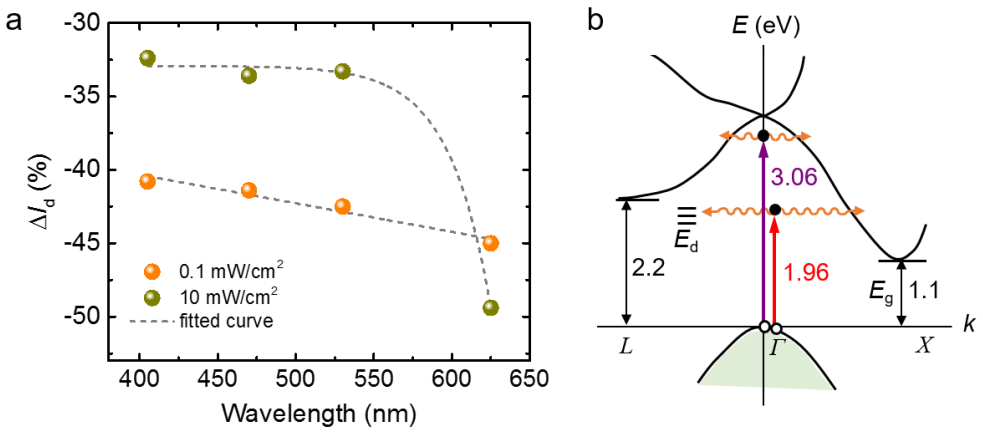


Figure 4.7 (a) Wavelength dependence of photocurrent change of the n^+-doped back gate device with weak and strong light power intensity. (b) The schematic energy band diagram of Si under visible light illumination. The energy band gap of Γ- and L- valley of Si and the energy of red (λ = 625 nm) and violet (λ = 405 nm) light are shown in the diagram.

the interface states are seldom filled with red light absorption. That is because the excitation probability is comparably small due to the low photon energy of red light as shown in Figure 4.7(b). Since the photon energy of the red light (1.96 eV) is lower than the energy band gap on the L-valley in the Si, the excited electrons are directly injected into the Γ-X band. However, hot electrons generated by the photon energy above the 2.2 eV can enter both X- or L-valleys with phonon assisted transition[38,39]. The absorption of the red light leads two effects; (i) no photoconduction in the L-band and (ii) quasi sub-bandgap excitation. By (i), excess mobile carriers are generated only in the X-valley, strongly limiting carrier generation, unlike other visible light-induced excitation, which allows both valleys conduction. For (ii), though the visible light absorption induces super-bandgap excitation (*i.e.*, $E_{ph} > E_g$), excited electrons could be captured by defect states (E_d) in the band gap between the L-band minimum and the X-band minimum during the momentum change by phonon absorption or emission, like sub-bandgap trapping in previous studies[21–23]. This phenomenon is expected only in the indirect band gap semiconductor. Thus, quasi sub-bandgap trapping would be highly probable with the red light absorption, which could normally enhance the NPC.

4.7 Conclusion

Negative photoconductance of Si nanowire FETs with different doping concentrations and light wavelengths and intensities is demonstrated in this chapter. This is the first observation of the NPC, induced by the hot trapped carriers in the nano-scaled semiconductors with indirect gap. The main sources of the NPC are the light induced V_{th} shift by photoexcited electrons trapping in the interface (outside of nanowire) and dopants ions (inside of nanowire). This characteristic behavior is considered as the intrinsic field effect induced by light. The interfacial trap state explains the doping concentration dependence, but the dopants ion trapping becomes important for the doping types (*n*- or *p*-type). Since the NPC of nanowire devices depends on doping concentration, heavily n-doped devices show strong NPC behavior due to its longer interfacial trapping time. Also, the NPC and PPC occurs by means of light intensity which decides the carrier generation rate competing with the carrier recombination life time. NPC appears differently with wavelength in visible light area due to the phonon assisted excitation to multi-conduction bands in the indirect band gap Si.

Finally, analysis of the obtained results for heavily doped Si nanowires and comparison with NPC in various nano-structures from available literatures, allows us to make an interesting observation that the NPC could be considered as a universal phenomenon for low-dimensional systems, due to the stronger influence of the surface/interface states. This work could provide fascinating insight into the photoconductivity in nano-systems influenced by unavoidable defects. The controllable bipolar optical current switching may open novel possibilities in Si nanostructure-based electronic applications like optical integrated logic circuits or photonic function generators.

References

1. Baek, E. *et al.* Negative Photoconductance in Heavily Doped Si Nanowire Field-Effect Transistors. *Nano Lett.* **17,** 6727–6734 (2017).
2. Penchina, C. M., Moore, J. S. & Holonyak, N. Energy levels and negative photoconductivity in cobalt-doped silicon. *Phys. Rev.* **143,** 634–636 (1966).
3. Aberle, A. G., Glunz, S. & Warta, W. Impact of illumination level and oxide parameters on Shockley-Read-Hall recombination at the Si-SiO2 interface. *J. Appl. Phys.* **71,** 4422–4431 (1992).
4. Bae, J. *et al.* Si nanowire metal–insulator–semiconductor photodetectors as efficient light harvesters. *Nanotechnology* **21,** 95502 (2010).
5. Yang, C., Barrelet, C. J., Capasso, F. & Lieber, C. M. Single p-Type/Intrinsic/n-Type Silicon Nanowires as Nanoscale Avalanche Photodetectors. *Nano Lett.* **6,** 2929–2934 (2006).
6. Hu, L. & Chen, G. Analysis of Optical Absorption in Silicon Nanowire Arrays for Photovoltaic Applications. *Nano Lett.* **7,** 3249–3252 (2007).
7. Kelzenberg, M. D. *et al.* Photovoltaic Measurements in Single-Nanowire Silicon Solar Cells. *Nano Lett.* **8,** 710–714 (2008).
8. Tian, B. *et al.* Coaxial silicon nanowires as solar cells and nanoelectronic power sources. *Nature* **449,** 885–889 (2007).
9. Garnett, E. & Yang, P. Light Trapping in Silicon Nanowire Solar Cells. *Nano Lett.* **10,** 1082–1087 (2010).
10. Casalino, M., Sirleto, L., Iodice, M. & Coppol, G. Silicon Photodetectors Based on Internal Photoemission Effect: The Challenge of Detecting Near-Infrared Light. in *Photodetectors* (InTech, 2012). doi:10.5772/36014
11. Ahn, Y., Dunning, J. & Park, J. Scanning photocurrent imaging and electronic band studies in silicon nanowire field effect transistors. *Nano Lett.* **5,** 1367–70 (2005).
12. Cui, Y., Lauhon, L. J., Gudiksen, M. S., Wang, J. & Lieber, C. M. Diameter-controlled synthesis of single-crystal silicon nanowires. *Appl. Phys. Lett.* **78,** 2214–2216 (2001).
13. Das, S., Dhyani, V., Georgiev, Y. M. & Williams, D. A. High sensitivity silicon single nanowire junctionless phototransistor. *Appl. Phys. Lett.* **108,** 1–6 (2016).
14. Gao, X. P. a, Zheng, G. & Lieber, C. M. Subthreshold regime has the optimal sensitivity for nanowire FET biosensors. *Nano Lett.* **10,** 547–52 (2010).
15. Gao, A. *et al.* Enhanced Sensing of Nucleic Acids with Silicon Nanowire Field Effect Transistor Biosensors. *Nano Lett.* **12,** 5262–5268 (2012).
16. Zörgiebel, F. M. *et al.* Schottky barrier-based silicon nanowire pH sensor with live sensitivity control. *Nano Res.* **7,** 263–271 (2014).

17. DiMaria, D. J. & Stasiak, J. W. Trap creation in silicon dioxide produced by hot electrons. *J. Appl. Phys.* **65,** 2342 (1989).
18. Ghaffarzadeh, K. *et al.* Instability in threshold voltage and subthreshold behavior in Hf–In–Zn–O thin film transistors induced by bias-and light-stress. *Appl. Phys. Lett.* **97,** 113504 (2010).
19. Hamilton, M. C., Martin, S. & Kanicki, J. Thin-Film Organic Polymer Phototransistors. *IEEE Trans. Electron Devices* **51,** 877–885 (2004).
20. Nakanishi, H. *et al.* Photoconductance and inverse photoconductance in films of functionalized metal nanoparticles. *Nature* **460,** 371–375 (2009).
21. Huang, H. M. *et al.* Photoconductivity in single AlN nanowires by subband gap excitation. *Appl. Phys. Lett.* **96,** (2010).
22. Zhang, X. *et al.* Surface induced negative photoconductivity in p-type ZnSe : Bi nanowires and their nano-optoelectronic applications. *J. Mater. Chem.* **21,** 6736 (2011).
23. Li, L. *et al.* Deep-ultraviolet solar-blind photoconductivity of individual gallium oxide nanobelts. *Nanoscale* **3,** 1120 (2011).
24. Wei, P. C. *et al.* Room-temperature negative photoconductivity in degenerate InN thin films with a supergap excitation. *Phys. Rev. B - Condens. Matter Mater. Phys.* **81,** 1–5 (2010).
25. Lui, C. H. *et al.* Trion-induced negative photoconductivity in monolayer MoS2. *Phys. Rev. Lett.* **113,** 1–5 (2014).
26. Yang, Y. *et al.* Hot Carrier Trapping Induced Negative Photoconductance in InAs Nanowires toward Novel Nonvolatile Memory. *Nano Lett.* **15,** 5875–5882 (2015).
27. Johnson, L. & Levinstein, H. Infrared properties of gold in germanium. *Phys. Rev.* **117,** 1191–1203 (1960).
28. Chang, M. C. P., Penchina, C. M. & Moore, J. S. Excited Impurity States and Transient Photoconductivity in Cobalt-Doped Silicon. *Phys. Rev. B* **4,** 1229–1234 (1971).
29. *Photoconductivity: Art: Science and Technology*. (CRC Press, 1990).
30. Zheng, G., Patolsky, F., Cui, Y., Wang, W. U. & Lieber, C. M. Multiplexed electrical detection of cancer markers with nanowire sensor arrays. *Nat. Biotechnol.* **23,** 1294–301 (2005).
31. Schütt, J. *et al.* Compact Nanowire Sensors Probe Microdroplets. *Nano Lett.* **16,** 4991–5000 (2016).
32. Choi, S.-J. *et al.* Bio-inspired complementary photoconductor by porphyrin-coated silicon nanowires. *Adv. Mater.* **23,** 3979–83 (2011).
33. Baek, E. *et al.* Optoelectronic switching of nanowire-based hybrid organic/oxide/semiconductor field-effect transistors. *Nano Res.* **8,** 1229–1240 (2015).

34. Schroder, D. Electrical characterization of defects in gate dielectrics. *Mater. Devices, Ed. by DM* ... (2009).
35. Costato, M., Fontanesi, S. & Reggiani, L. Electron energy relaxation time in Si and Ge. *J. Phys. Chem. Solids* **34,** 547–564 (1973).
36. del Alamo, J. A. & Swanson, R. M. Modelling of minority-carrier transport in heavily doped silicon emitters. *Solid State Electron.* **30,** 1127–1136 (1987).
37. Tyagi, M. S. & Van Overstraeten, R. Minority carrier recombination in heavily-doped silicon. *Solid State Electron.* **26,** 577–597 (1983).
38. Ichibayashi, T., Tanaka, S., Kanasaki, J., Tanimura, K. & Fauster, T. Ultrafast relaxation of highly excited hot electrons in Si: Roles of the L-X intervalley scattering. *Phys. Rev. B - Condens. Matter Mater. Phys.* **84,** 1–11 (2011).
39. Aspnes, D. E. & Studna, A. A. Dielectric functions and optical parameters of Si, Ge, GaP, GaAs, GaSb, InP, InAs, and InSb from 1.5 to 6.0 eV. *Phys. Rev. B* **27,** 985–1009 (1983).

CHAPTER 5
EXTERNAL OPTICAL GATE: Si nanowire FETs coated by organic molecules

In this chapter, photosensitive hybrid field-effect transistor (FET) consisting of the multiple-shell organic molecular film/oxide/silicon nanowires. The photo-induced current switching in the hybrid devices originates from the electric field effect by charge redistribution within the organic film. The switching dynamics and efficiency of the hybrid devices is strongly dependent on the thickness of the organic film wrapping the nanowires. The field effect in organic film/oxide/semiconductor junctions will be shown using a photo-induced charging model in the organic film. The contents of this chapter is mainly based upon my published article[1].

5.1 Why organic materials for hybrid applications?

Smart hybrid nano-devices[2–4] integrating inorganic electronic components and organic materials is leading to various fascinating applications, such as organic transistors[5,6], organic solar cells[7,8] and artificial photosynthetic systems[9–11]. The organic materials have interesting and material-specific properties, such as the change of conformation or electronic structure resulted as a reaction to external stimuli, *e.g.* light, temperature, ionic strength of a solution. Therefore, the key advantage of combining organic materials and conventional electronic platforms is that the interesting properties of organic molecules can be directly converted into an electrical response of the electronic device. The

functionality of conventional electronics can be, therefore, dramatically broadened towards novel fields of biomolecular nanomachines and sensors[12] or energy harvesting systems[13,14] while maintaining the excellent performance and cost benefits of silicon-based electronic devices. Based on the stably settled CMOS process, the hybrid-based applications involving switchable or changeable organic materials from molecules to polymers, could be tailored to new technological needs beyond conventional electronics.

Porphyrin and its applications

In the realm of organic molecules, porphyrin has attracted significant attention for its important role in the metabolism of living organisms[15] and in the electron transfer as well as the photochemical catalysis in chlorophyll[16]. Porphyrin's unique aromatic structure allows a conjugated system (cf. Figure 5.1(a, b)) which causes the light absorption spectrum of the molecule overlaps with the solar emission spectrum (cf. Figure 5.1(c, d)). Therefore, this property makes the porphyrin an ideal candidate as an efficient light-harvesting center for organic photovoltaics[17]. For this purpose, porphyrin/metal and porphyrin/semiconductor interfaces for developing hybrid charge transfer systems have

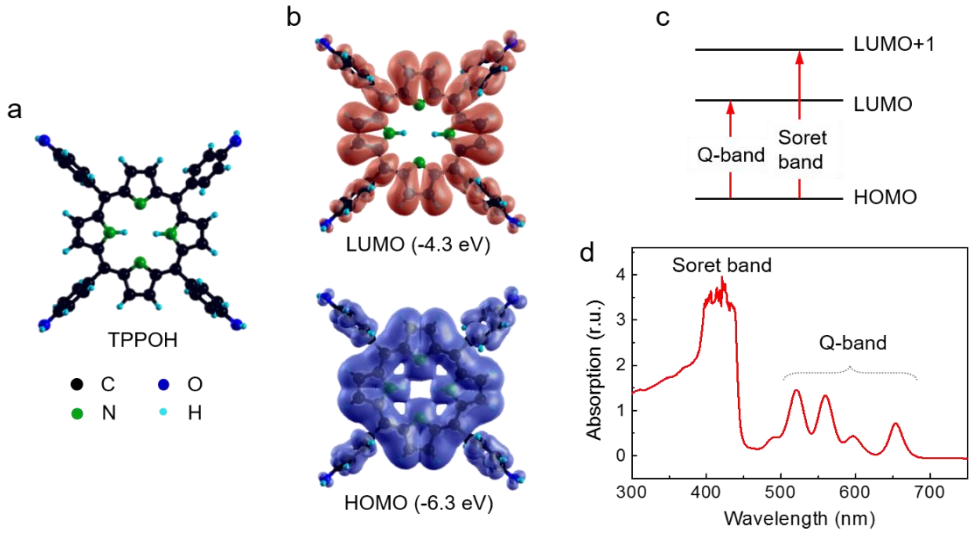


Figure 5.1 The physical characteristics of 5,10,15,20-Tetrakis(4-hydroxyphenyl)-21H,23H-porphine (TPPOH). (a) The chemical structure of TPPOH. (Black : C, Cobalt blue : O, Cyan : H, Green : N) (b) Simulated highest energy occupied molecular orbital (HOMO) and lowest energy occupied molecular orbital (LUMO) of TPPOH. (simulated by Lokamani, TU Dresden) (c) Photo-excited states and corresponding energy band structure of TPPOH. (d) UV/visbible absorption spectrum of 100μM TPPOH in methanol.

been at the center of intense investigation[18–25]. These systems exploit direct electron transport from photo-excited porphyrin molecules to inorganic electron carrier templates, which have been implemented for *e.g.* hybrid transistor memory applications[19–24] enabling charge storage in porphyrin molecules induced by light illumination.

Photo-induced charge transfer induced via interfacing the porphyrin and the 1D nanodevices, (*i.e.* carbon nanotubes[26] or nanowires[27]) was demonstrated by a number of groups[19,21–27] initiating a new direction in the field of *hybrid nanoelectronics*. Particular attention was given to silicon nanowire-based field-effect transistor (FET) devices functionalized by porphyrin molecules. In this system, Si nanowires are employed as building blocks of porphyrin hybrid devices, *i.e.* bio-inspired CMOS[23] or charge-coupled devices[24,25]. Si nanowire has strong advantages such as molecular compatible size and guaranteed sensitivity caused by the high surface-to-volume ratio. Current modulation upon light illumination of the devices can be mostly attributed to a direct photo-induced charge transfer of electrons into Si nanowire core[23,25].

Although porphyrin/inorganic hybrid systems have been considerably investigated, there are still practical challenges to realize and commercialize such hybrid devices combining silicon technology with chemical functionalization. The main shortcomings are due to a strong influence of the interface quality on the device switching efficiency caused by significant contaminations during clean room fabrication procedures. This requires a fundamentally novel and distinct way with respect to the existing hybrid devices relying on organic-semiconductor contacts.

5.2 Hybrid organic/oxide/semiconductor (OOS) nanowire FETs

A photosensitive hybrid organic/oxide/semiconductor (OOS) Si nanowire-based FET device is fabricated, which contains intruded Schottky nano-junctions, coupled to an amorphous organic film of porphyrin molecules via thermally grown oxide layer shown in Figure 5.2. In this configuration, 5,10,15,20-Tetrakis(4-hydroxyphenyl)-21H, 23H-porphine (TPPOH) molecules are attached onto the 5 nm thermally grown oxide layer surrounding Si nanowire, in contrast with typical coating of direct metal or semiconductor surfaces in previous studies (cf. Figure 5.1(a)). Different concentrations of TPPOH dissolved in a 5% aqueous ethanol solution were applied onto the devices by drop casting technique (see **Section 3.1**). Porphyrin forms the outer shell of the nanowires acting as

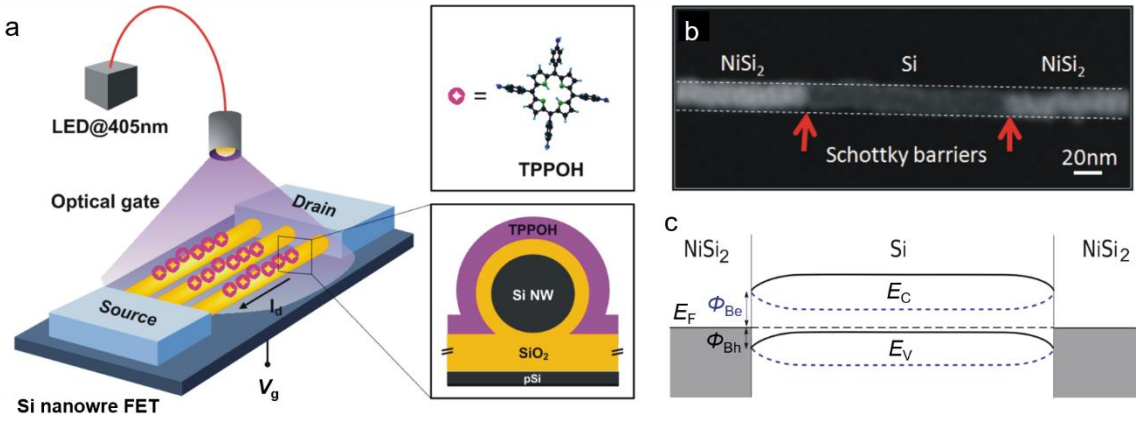


Figure 5.2 (a) Schematic diagram of a hybrid light sensitive Si nanwoire FET. The Si nanowire device is optically sensitive due to covered TPPOH molecules. The system consists of TPPOH/oxide/Si nanowire shells. (b) SEM image of $NiSi_2$ electrode to a Si nanowire. Brighter area indicates $NiSi_2$ phases and the dark part of the nanowire shows the Si channel. (c) Energy band diagram of a Schottky barrier FET. Depending on the gate voltage (V_g), the device can be switched into *n*-type (blue dashed lines) or *p*-type (black solid lines) conductance regimes by the conduction band (E_c) and the valence band (E_V) bending. Φ_{Be} and Φ_{Bh} are the Shottky barrier height for electrons and holes, respectively.

the 'OOS capacitor'. According to the location of Soret band (Figure 5.1(d)), excitation of porphyrin TPPOH is performed by violet light using LED source (405 nm, Thorlabs) with the optical power density of approximately 1.1 mW/cm^2. Therefore, photo-induced charges of porphyrin is able to tune the Schottky barriers within the Si nanowire channel (Figure 5.2(b,c)) and influences the threshold voltage (V_g) of the devices.

The hybrid OOS FETs consists of multiple bottom-up grown intrinsic Si nanowires aligned between nickel electrodes as parallel arrays[28]. Figure 5.2(b) shows well-defined phases of nickel silicide fractions within the single nanowire produced by means of axial diffusion of nickel into the nanowire body[28]. The FET devices, consisting of arrays of parallel nanowires, provide reduced device-to-device variability and high source-drain current level as well as high transconductance[28]. The structure of the devices is described in **Section 3.1.1** (see Figure 3.1). The current flowing through Si nanowire FETs is controlled by the Schottky barriers formed between metallic ($NiSi_2$) and Si segments of nanowires (see Figure 5.2 (b,c)) in the saturation regime, and by the nanowire channel charge in the sub-threshold regime[29–31]. Depending on V_g, the transport channel is opened for electrons (Figure 5.2(c), blue dashed line) or for holes (Figure 5.2(c), black solid line).

If V_g makes the Si nanowire Fermi level to position in the middle of the Si bandgap, the both electron- and hole current are minimized and the conductance of the transistor is very small. Due to (i) the charges in the oxide layer, (ii) electron-hole asymmetry in real devices and (iii) difference in Schottky barrier heights for electrons and holes, the minimum of source-drain current (I_d) as a function of V_g typically does not coincide with $V_g = 0$ V.

On the device, the porphyrin film covers whole device, including nickel electrodes and forming organic shell around nanowires. Therefore, Figure 5.3 characterizes the porphyrin coverage on nanowires and surface roughness depending on the concentration of molecules dissolved in the solution. Low concentrations of TPPOH in solutions (around 10μM) resulted into an inhomogeneous coverage of the nanowires by molecules and their aggregation into separated spots (~100 nm diameter) (see red circles in Figure 5.3(a)). Increase of the TPPOH concentration leads to the full coverage of the nanowires with molecules (see Figure 5.3(b), at 100μM). The TPPOH-covered surface has non-regular morphology with high roughness shown in Figure. 5.3(c,d). Porphyrin tends to aggregate together as the concentration increases.

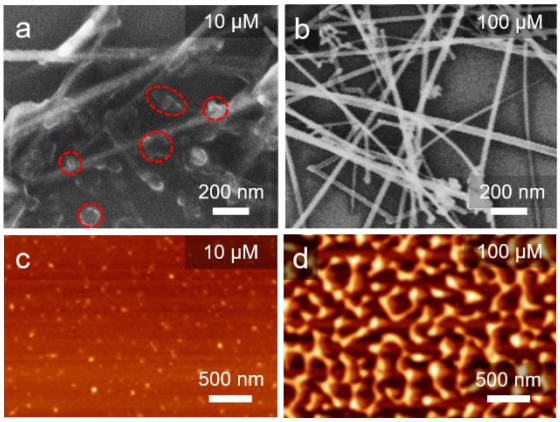


Figure 5.3 Surface functionalization of Si oxide surface with porphyrin film. Porphyrin coverage of nanowires depends on its concentration. Scanning electron microscopy (SEM) images of sprayed Si nanowires covered by (a) 10 μM and (b) 100 μM of the TPPOH solution. Atomic force microscope (AFM) images of porphyrin-coated SiO_2 surface with (c) 10 μM and (d) 100 μM of TPPOH solution

The formed organic film of TPPOH on top of nanowires has preferably amorphous structure, as proven by high resolution transmission electron microscopy (HR-TEM) analysis (see insets in Figure 5.4). The integrity and the thickness of the porphyrin film plays a significant role in switching behavior of the OOS hybrid devices and electrical charge distribution within the molecular shell, as will be discussed below. For this reason, the quantitative analysis of the resulting thickness of organic shell around the nanowires

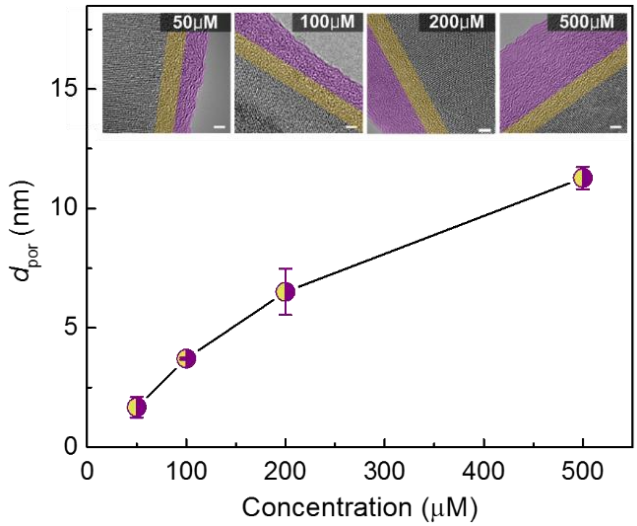


Figure 5.4 Plot of the thickness of porphyrin layer covering nanowires as a function of concentration. The thickness of porphyrin is investigated based on TEM images with different concentrations. The yellow area is the SiO_2 and the violet area is the covering porphyrin (Scale bar: 2nm). TEM analysis is conducted by Dr. Rafael Mendes, IFW Dresden.

in dependence of the TPPOH concentration is demonstrated in Figure 5.4. Here, grown Si nanowires covered by native oxide shell were used for test purposes, without electrode formation. In order to determine the shell thickness as a function of TPPOH concentration, HR-TEM investigations were conducted with nanowires incubated in solutions with different concentrations of TPPOH. Even though amorphous porphyrin and SiO_2 layer are not visibly distinguished, the thickness of TPPOH shell can be derived based on the constant oxide layer thickness (~3.2 nm), which also appears in TEM as amorphous material. Gradual increase of the amorphous fraction on the surface of the nanowires was investigated in order to quantify the thickness of the porphyrin. For better comparison, all the images were taken at the same magnification. Considering the thickness of native oxide shell around an individual Si nanowire, and the amorphous layer of TPPOH in HR-TEM, the mean thicknesses of porphyrin d_{por} were estimated as 1.6, 3.7, 6.5 and 11.2 nm for TPPOH concentrations of 50, 100, 200 and 500 µM, respectively.

5.3 Optoelectronic switching of hybrid nanowire FETs

Figure 5.5 presents the photo-induced current switching behavior (*i.e.* dynamics and efficiency) of the hybrid FETs depending on the concentration of TPPOH and thus, on

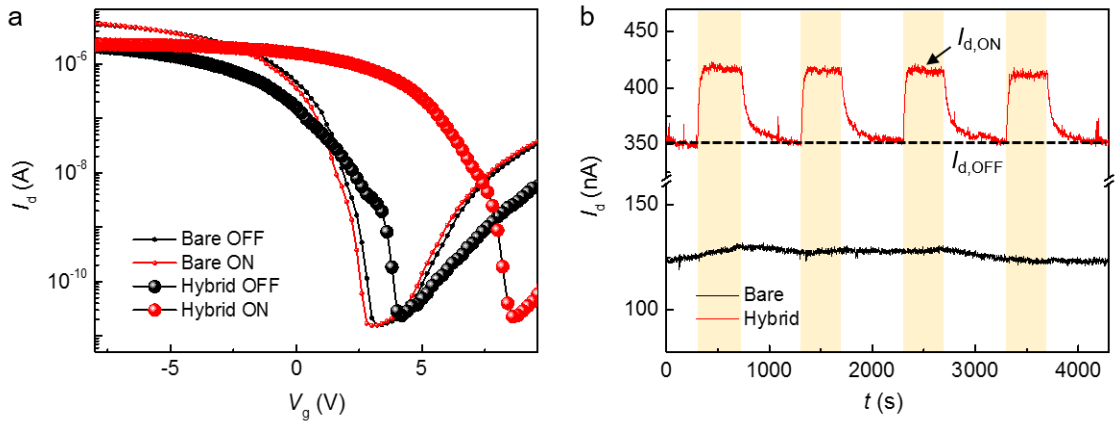


Figure 5.5 Light-induced current switching characteristics of hybrid Si nanowire FETs. (a) Transfer characteristics (I_d-V_g) of the bare device and the hybrid device covered with 200 μM of TPPOH film in the dark condition (OFF) and under light illumination (ON) (V_d = 0.1 V) (b) Current switching induced by light for bare and 200 μM porphyrin covered hybrid devices as a function of time. Shaded area indicates light irradiation. (V_d = 0.1 V and V_g = 1 V.)

the thickness of organic film. Figure 5.5(a) compares the transfer characteristics (I_d vs V_g) of the nanowire device before (Bare) and after (Hybrid) TPPOH coverage and demonstrates the effect of light illumination (OFF and ON) on the device. The transfer curve of the hybrid device is shifted towards positive gate voltages by approximately 1 V from the curve of the bare device. Under the light illumination (ON), the threshold voltage (V_{th}) of the hybrid device is further shifted towards positive direction with increasing light-exposure time. On the other hand, no significant curve shift is observed from the bare devices. Further electric characteristics of hybrid devices are lower saturation current and increased subthreshold slopes compared to the bare devices, which will be discussed in the **Section 5.4**.

The photo-induced current switching is demonstrated in Figure 5.5(b) for the bare device and the hybrid device covered with 200 μM of TPPOH (d_{por} = 6.5 nm). The gate bias values were chosen to be close to the threshold condition in the bare device, where the current level is near 100 nA. Once the device is exposed to the light (ON), I_d increases and reached the steady state level ($I_{d,ON}$) after approximately 40 s. After the light is turned off, the current relaxes to its level before illumination ($I_{d,OFF}$). Multiple switching cycles of the device were recorded upon repeatedly turning illumination ON and OFF. Absence of switching was observed from the bare nanowire devices (see black curve in Figure 5.5(b)).

This result is pleasantly comparable with the photoconductance of *p*-doped nanowire devices (Figure 4.1(d) of **Section 4.1)**. *p*-doped nanowire device shows around 200% immediate increase of current upon same wavelength and light power intensity. The low photoconductance of undoped device is caused by (i) the low photo-excited electron generation rate (only intrinsic carriers) and (ii) long interfacial trapping time. Therefore, the porphyrin coating significantly reinforces the photoconductance of poor photodetecting device.

Switching dynamics and efficiency

In contrast to the previous reports[23,25], the switching mechanism in hybrid OOS nanowire device is different, since direct charge transfer between the organic film and the conduction channel is effectively suppressed by the high quality thermally grown SiO_2 shell. The photo-induced current switching of the hybrid device is dramatically depending on the thickness of the organic porphyrin film. Thus, (i) *switching dynamics* (time to reach the steady state $I_{d,OFF}$ or $I_{d,ON}$) and (ii) *switching efficiency* ($(I_{d,ON}-I_{d,OFF})/I_{d,OFF}$) are analyzed.

The switching dynamics of hybrid OOS device is demonstrated in Figure 5.6(a) and is found to be strongly dependent on the layer thickness of the porphyrin. Remarkably, the switching time drastically decreases, if the concentration of TPPOH in applied solution and, corresponding thickness of the organic film are increased. Obtained channel current was fitted by exponential functions in order to derive the characteristics time constants for increasing I_d upon light exposure, τ_1, and decreasing I_d in the dark condition, τ_2, respectively according to

$$y = y_1 + A_1 * \left(1 - \exp\left(-\frac{t}{\tau_1}\right)\right) \tag{5.1}$$

$$y = y_2 + A_2 \exp(-\frac{t}{\tau_2}) \tag{5.2}$$

where y_1 and y_2 are offset current levels before stimuli, and A_1 and A_2 are starting values of exponential growing and decaying respectively.

Figure 5.6(a) demonstrates the exponential decrease of the time constants τ_1 and τ_2 as a function of the film thickness. τ_2 is always longer than τ_1, since current decaying processe in the dark depends on the thermal relaxation of electrons in the porphyrin layer. This process is known to be slower compared to the photoexcitation of electrons[32].

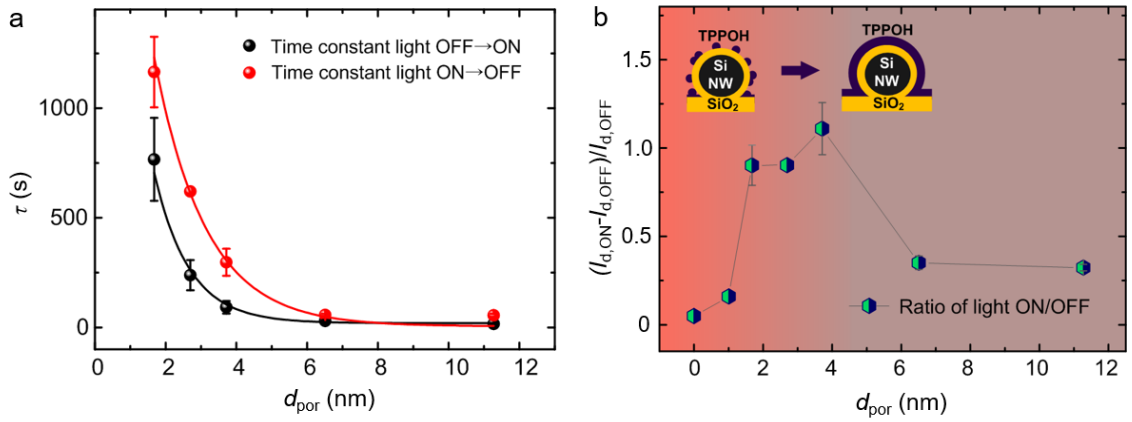


Figure 5.6 (a) Switching dynamics. Extracted time constant (τ) of the light-induced current increasing ($I_{d,OFF} \rightarrow I_{d,ON}$) and current decreasing in dark ($I_{d,ON} \rightarrow I_{d,OFF}$) as a function of the porphyrin film thickness. The solid lines are exponential decaying fitted curves. (b) Switching efficiency. Current ratio $(I_{d,ON}\text{-}I_{d,OFF})/I_{d,OFF}$ of the transistors under illumination as a function of the film thickness.

The switching efficiency of the hybrid nanowire OOSFETs, defined here as ratio of currents under light illumination (ON) and in dark conditions (OFF), is shown in Figure 5.6(b) as the function of the porphyrin film thickness. Interestingly, the switching ratio reveals a non-monotonous dependence on the organic film thickness correlated with the concentration of porphyrin. With a thin film below 2 nm, the current ratio gradually increases up to a value of 1.2 (120 %) at 4 nm film thickness. For the film thickness above 4 nm, the switching ratio decreases exponentially. Improvement of the switching efficiency under 4 nm is due to the formation of the porphyrin shell which has a more regular amorphous structure from the islands as the concentration increases (see Figure 5.3(a,b)). A 4-5 nm layer of TPPOH would be the optimal thickness of the porphyrin shell to get the highest switching ratio. Further decrease of the switching efficiency is apparently due to thick organic film. Such behavior will be discussed in details in the **Section 5.5**.

5.4 Optical gating mechanism of hybrid FETs

In the following, the shift of the surface potential due to the processes inside of the organic film, so called the *optical gating* will be discussed. When the porphyrin covers the devices without light (Figure 5.7(a)), two effects on the transfer curve are observed: (i) curve shift

along the V_g axis and (ii) saturation current reduction and subthreshold slopes degradation (Figure 5.7(d)). In the dark condition (OFF), the V_{th} shift (i) is influenced by the charge distribution in the system, the difference in the work functions of the porphyrin and Si nanowire or Si substrate (Figure 5.7(b)).

The experimental curves in Figure 5.5(a) clearly demonstrate that the shift is relatively small in the dark state (Figure 5.7(d)), indicating weak charging of the porphyrin film. Such behavior can be attributed to the fact that the TPPOH film is an intrinsic semiconductor with large energy gap, and has low conductivity. Once the TPPOH film is placed in contact with electrodes, their Fermi levels ($E_{F,TPPOH}$) tend to equilibrate. The number of free carriers in porphyrin is very low and only weakly charged dipole layer is formed between the *p*-Si substrate and the organic porphyrin film, resulting in the negligibly small band bending effect. Figure 5.7(c) reflects this situation, showing the band structure of Si nanowire near the minimum current of I_d-V_g curve. The effect (ii) could be interpreted by the reduced dielectric capacitance between nanowire channel and back gate, due to the serial connection of oxide capacitance and comparably lower porphyrin capacitance.

The shift of the transfer characteristics becomes much more pronounced under the light illumination (ON) (Figure 5.5(a), 5.7(h)). Potential explanation of this effect is that porphyrin film acquires a higher conductance as a result of light exposure. The photo induced excited electrons and holes can diffuse from the source and drain electrodes and create the double charge layer equilibrating the Fermi levels of porphyrin and the *p*-Si (Figure 5.7(f)), thus generating a large additional negative electrical potential to TPPOH. The additional potential in TPPOH can be regarded as an additional gate voltage, shifting I_d-V_g curve (see Figure 5.7(g,h)). Previous experimental and theoretical studies[33–35] demonstrate that the molecular levels of isolated TPPOH have energies of about -6.3 eV (HOMO) and -4.3 eV (LUMO) (see Figure 5.1(b)). Thus, the chemical potential ("Fermi level") of porphyrin can be estimated to be in the range of -5.5~-6 eV. Furthermore, the chemical potential of porphyrin lies lower in energy than the Fermi level of metal electrodes and *p*-Si substrate (around -5 eV) (Figure 5.7(b)). Based on the Fermi levels studies, the additional electrical potential in the porphyrin is estimated to be around -0.5 ~ -1 V which is caused by the Fermi level alignment under light exposure. However, this additional potential from the E_F alignment is significantly smaller than the V_{th} shift by

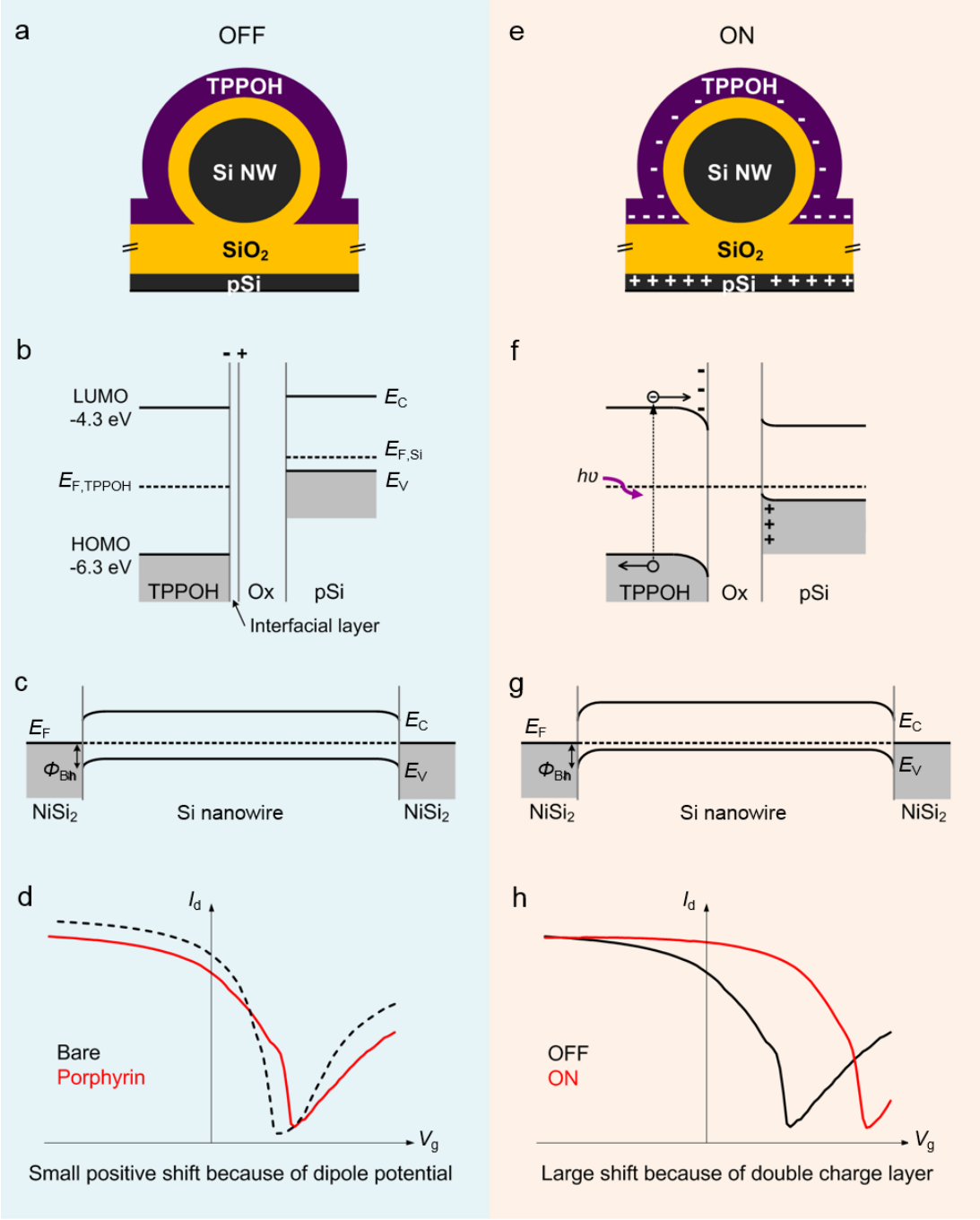


Figure 5.7 Current switching mechanism of porphyrin coated hybrid nanowire FETs. In the dark (OFF) state (left panel, a-d), the porphyrin film is ground state and insulating. When the light is turned on (right panel, e-h), the porphyrin behaves like a semiconductor inducing a negative charge close to the interface. (a,e) Schematic diagram of cross section of the hybrid nanowire FETs with induced charge. (b, f) Energy band diagrams for porphyrin and the *p*-Si substrate before and after light irradiation. (c ,g) Energy band diagrams for Si nanowire FET near the off current state (minimum current level). (d, h) Comparisons of transfer curves.

light illumination (~4 V). The larger measured shift is, thus, explained by the screening action of the charges over whole chip surface. Note, the capacitance between the back substrate and the organic film plays the dominant role in the curve shift, since its area is much larger than the areas of contacts of the porphyrin with electrodes and the Si nanowires.

5.5 *Effect of charge transfer in the organic film*

Switching dynamics depending on the mobility of porphyrin

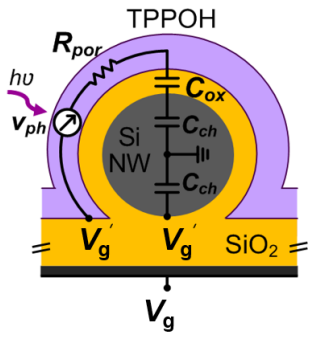


Figure 5.8 Schematic circuit diagram of porphyrin (TPPOH) coated hybrid nanowire FETs under light illumination.

In the following, the dependence of the switching behavior of OOS device on the thickness of porphyrin film will be discussed. The experimentally observed switching time constants τ_1 and τ_2 (see Figure 5.6(a)), are found to be quite large in the OOS device, ranging from ~1 sec for the thick porphyrin film to ~103 sec for the thin film. It can be explained by a long duration of the electron diffusion from the source and drain electrodes to the porphyrin shell covering NWs. Ideally, the device and corresponding processes of charging organic film is represented by the equivalent *RC*-circuit in Figure 5.8, where time constants can be estimated as the characteristic time;

$$\tau = R_{\text{por}} C_{\text{eq}} \tag{5.3}$$

where the equivalent capacitance, C_{eq}, is the series capacitance of the channel capacitance, C_{ch}, and the oxide capacitance, C_{ox}, and R_{por} is the resistance of the porphyrin film under illumination. It can be estimated that $C_{\text{eq}} \approx C_{\text{ox}}$, because C_{ox} is much larger than C_{ch}. The oxide capacitance between the back gate and the porphyrin film,

$$C_{ox} = \frac{\varepsilon S}{W} \tag{5.4}$$

where S is the area of the capacitor formed by the back gate and the porphyrin layer, W is the thickness of SiO_2 layer and ε is a dielectric constant of the oxide. The resistance of porphyrin,

$$R_{por} = \frac{l}{q(n_e\mu_e + n_h\mu_h)A} \tag{5.5}$$

where q is elementary charge, n_e and n_h are the density of electrons and holes, μ_e and μ_h are mobility of electron and hole respectively, l is the characteristic length between the source and the drain and A is a cross-section area of the porphyrin layer which is the product of the electrode length and the porphyrin thickness. In the following, a realistic value of the density of free carriers within porphyrin film generated by light is estimated. The density of free carriers depends on two subsequent processes: (i) exciton generation and (ii) dissociation of excitons into free electrons and holes and their diffusion; From the characteristic switching time of 10 sec (approx. 4 nm) and the geometrical sizes of the device, we estimate $n_e\mu_e \approx 10^{11}$ $(\text{cmVs})^{-1}$ for photo-excited electrons (assuming the case of heavy holes). Taking the typical value of the light induced electron diffusion coefficient in porphyrins ($D \approx 10^{-7}$ $\text{cm}^2\,\text{s}^{-1}$) [36], one estimates the mobility of carriers inside the organic film to be about $\mu_e \approx 10^{-5}$ cm^2/Vs. The density of the free carriers in the porphyrin layer lies in the range from $n_{max} \approx 10^{21}$ cm^{-3} (the estimation for the concentrations of the molecules ~100 μM) to $n_{min} \approx 10^{8}$ cm^{-3} which is the concentration required to create the potential shift of the order of several volts. Taking into account the obtained value for mobility μ_e, the density of the free carriers is estimated to be $n_e \approx 10^{16}$ cm-^{3}, which lies in the range between n_{max} and n_{min}. Therefore, the experimental switching time scale is reasonable for our system corresponding to the porphyrin layer density and the level of threshold voltage shift. Also, the mobility of free carriers in the organic film and thus switching dynamics of the OOS device highly depends on integrity of the organic molecular film. Therefore, at higher concentrations of porphyrin, over 100 μM, molecules improve the intermolecular percolation paths and increase electron hopping probability; this results in relatively faster switching time constant (about 1 s). In contrast, large switching time constant (up to 10^3 s), observed at low concentrations of porphyrin (lower than 100 μM) is due to a very low mobility, electron density, and

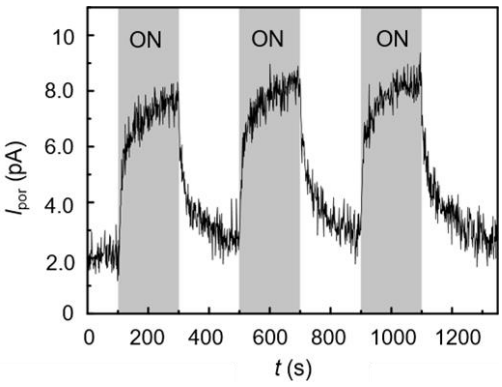


Figure 5.9 Optical current switching of porphyrin layer without nanowires. The shaded area indicates the device under light illumination. $V_g = 0$ V, $V_d = 20$ V were applied.

conductance of the organic film. The measured current switching characteristics of the porphyrin film is shown in Figure 5.9. The resistance of 1 mM of porphyrin thin film is 10 TΩ in the dark condition with same electrode distance with the nanowire devices. From this result, $n_e \sim 10^{20}$ cm^3 is calculated which also agrees with the theoretical value.

Switching efficiency depending on the diffusion

In order to understand the switching efficiency, the processes of the photo-excitation and dissociation of the excitons within the organic layer need to be considered. The typical exciton diffusion length in the organic films is about few nanometers depending on the molecular structure[37,38]. Therefore, the thicker layers have a limit to transfer the photo-energy effectively from the light incident surface to the active interfacial layer. Once the organic film of the porphyrin becomes thicker, the diffusion length of excitons becomes a crucial parameter for optimal operation of the light-induced hybrid device. Based on the previous experimental and theoretical investigations of porphyrin films, the absorption length of light is estimated to about 5-10 nm and the exciton diffusion length is about 10-15 nm[38–41]. In our case, however, these numbers should be smaller because of amorphous structure of the organic film, especially in the case of low porphyrin concentrations, when the structure of the film is inhomogeneous.

Figure 5.6(b) demonstrates that at thin porphyrin layer (< 5 nm, concentration < 100 μM), the switching ratio is low and tends to increase until the thickness reaches 5 nm. In the case of larger thickness of porphyrin (> 5 nm, concentration > 100 μM), the maximum of exciton distribution (gaussian)[39] is inside the porphyrin film (cf. Figure 5.10). Therefore, only a fraction of the excitons diffuses towards the porphyrin/oxide interfaces where the excitons can dissociate. This leads to a decrease of the switching efficiency of the hybrid device. Thus, the maximum of the switching ratio (Figure 5.6(b)) coincides with the porphyrin layer thickness of 5 nm.

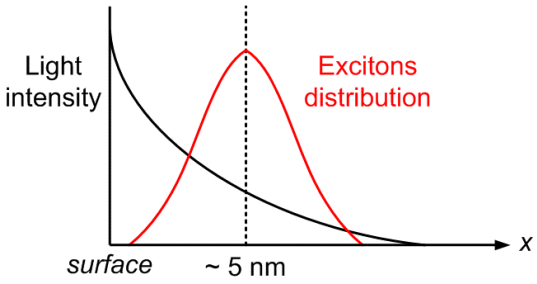


Figure 5.10 Expected schematic diagram of the exciton model for porphyrin-coated surface showing the light intensity as a function of the distance from the surface (black) and the resulting expected distribution of excitons (red).

5.6 Conclusion

A hybrid nano-scaled field-effect transistor (OOSFET) consisting of inorganic Si nanowires, coupled to a photosensitive organic film of porphyrin molecules on thermally grown oxide layer are fabricated and its switching behavior under the light illumination is demonstrated. Design of the device offers an alternative switching principle, compared to a photo-induced electron injection, valid for devices relying on direct junctions between organic molecules and metals or semiconductors. The switching dynamics and switching efficiency of the hybrid nano-devices are investigated and its strong dependence on thickness of the porphyrin film wrapping the nanowires is shown. In particular, a switching of the devices is governed by light generated excitons and further charge redistribution within the organic film. Therefore, these charges induce additional electrical potential within the TPPOH, which positions the *electric field effect* as a dominant mechanism for OOSFET switching.

Such *hybrid devices* are closely related to the fields of *hybrid memory applications*, which is deeply discussed in **Chapter 8** and a proof-of-concept *optical memory* is shown in **Appendix A.3**.

References

1. Baek, E. *et al.* Optoelectronic switching of nanowire-based hybrid organic/oxide/semiconductor field-effect transistors. *Nano Res.* **8,** 1229–1240 (2015).
2. Sanchez, C., Julián, B., Belleville, P. & Popall, M. Applications of hybrid organic–inorganic nanocomposites. *J. Mater. Chem.* **15,** 3559 (2005).
3. Inganäs, O. Hybrid electronics and electrochemistry with conjugated polymers. *Chem. Soc. Rev.* **39,** 2633 (2010).
4. Joachim, C., Gimzewski, J. K. & Aviram, A. Electronics using hybrid-molecular and mono-molecular devices. *Nature* **408,** 541–548 (2000).
5. Crone, B. *et al.* Large-scale complementary integrated circuits based on organic transistors. *Nature* **403,** 521–523 (2000).
6. Halik, M. *et al.* Low-voltage organic transistors with an amorphous molecular gate dielectric. *Nature* **431,** 963–966 (2004).
7. Günes, S., Neugebauer, H. & Sariciftci, N. S. Conjugated Polymer-Based Organic Solar Cells. *Chem. Rev.* **107,** 1324–1338 (2007).
8. Cheng, Y.-J., Yang, S.-H. & Hsu, C.-S. Synthesis of Conjugated Polymers for Organic Solar Cell Applications. *Chem. Rev.* **109,** 5868–5923 (2009).
9. Wasielewski, M. R. Photoinduced Electron Transfer in Supramolecular Systems for Artificial Photosynthesis. *Chem. Rev.* **92,** 435–461 (1992).
10. Imahori, H. Porphyrin–fullerene linked systems as artificial photosynthetic mimics. *Org. Biomol. Chem.* **2,** 1425–1433 (2004).
11. Fukuzumi, S. Development of bioinspired artificial photosynthetic systems. *Phys. Chem. Chem. Phys.* **10,** 2283 (2008).
12. Ozin, G. A., Manners, I., Fournier-Bidoz, S. & Arsenault, A. Dream Nanomachines. *Adv. Mater.* **17,** 3011–3018 (2005).
13. Qin, Y., Wang, X. & Wang, Z. L. Microfibre–nanowire hybrid structure for energy scavenging. *Nature* **451,** 809–813 (2008).
14. Donelan, J. M. *et al.* Biomechanical energy harvesting: generating electricity during walking with minimal user effort. *Science* **319,** 807–10 (2008).
15. Dawson, J. H. Probing structure-function relations in heme-containing oxygenases and peroxidases. *Science* **240,** 433–9 (1988).
16. Gust, D., Moore, T. A. & Moore, A. L. Molecular Mimicry of Photosynthetic Energy and Electron Transfer toinitiated electron transfer involving chlorophylls and quiñones which transforms excitation energy into chemical potential in the form of long-lived, trans. *Acc. Chem. Res* **26,** 198–205 (1993).

17. Martínez-Díaz, M. V., de la Torre, G. & Torres, T. Lighting porphyrins and phthalocyanines for molecular photovoltaics. *Chem. Commun.* **46,** 7090 (2010).
18. Ishii, H., Sugiyama, K., Ito, E. & Seki, K. Energy Level Alignment and Interfacial Electronic Structures at Organic/Metal and Organic/Organic Interfaces. *Adv. Mater.* **11,** 605–625 (1999).
19. Liu, Z., Yasseri, A. A., Lindsey, J. S. & Bocian, D. F. Molecular memories that survive silicon device processing and real-world operation. *Science* **302,** 1543–5 (2003).
20. Seol, M.-L., Choi, S.-J., Kim, C.-H., Moon, D.-I. & Choi, Y.-K. Porphyrin–Silicon Hybrid Field-Effect Transistor with Individually Addressable Top-gate Structure. *ACS Nano* **6,** 183–189 (2012).
21. Star, A., Lu, Y., Bradley, K. & Grüner, G. Nanotube Optoelectronic Memory Devices. *Nano Lett.* **4,** 1587–1591 (2004).
22. Li, C. *et al.* Data Storage Studies on Nanowire Transistors with Self-Assembled Porphyrin Molecules. *J. Phys. Chem. B* **108,** 9646–9649 (2004).
23. Choi, S.-J. *et al.* Bio-inspired complementary photoconductor by porphyrin-coated silicon nanowires. *Adv. Mater.* **23,** 3979–83 (2011).
24. Winkelmann, C. B. *et al.* Optical switching of porphyrin-coated silicon nanowire field effect transistors. *Nano Lett.* **7,** 1454–8 (2007).
25. Seol, M.-L., Choi, S.-J., Choi, J.-M., Ahn, J.-H. & Choi, Y.-K. Hybrid porphyrin-silicon nanowire field-effect transistor by opto-electrical excitation. *ACS Nano* **6,** 7885–92 (2012).
26. Borghetti, J. *et al.* Optoelectronic Switch and Memory Devices Based on Polymer-Functionalized Carbon Nanotube Transistors. *Adv. Mater.* **18,** 2535–2540 (2006).
27. Léonard, F. & Talin, A. A. Electrical contacts to one- and two-dimensional nanomaterials. *Nat. Nanotechnol.* **6,** 773–783 (2011).
28. Pregl, S. *et al.* Parallel arrays of Schottky barrier nanowire field effect transistors: Nanoscopic effects for macroscopic current output. *Nano Res.* **6,** 381–388 (2013).
29. Weber, W. M. *et al.* Silicon-Nanowire Transistors with Intruded Nickel-Silicide Contacts. *Nano Lett.* **6,** 2660–2666 (2006).
30. Nozaki, D. *et al.* Multiscale modeling of nanowire-based Schottky-barrier field-effect transistors for sensor applications. *Nanotechnology* **22,** 325703 (2011).
31. Martin, D. *et al.* Direct Probing of Schottky Barriers in Si Nanowire Schottky Barrier Field Effect Transistors. *Phys. Rev. Lett.* **107,** 216807 (2011).
32. Robinson, G. W. & Frosch, R. P. Electronic Excitation Transfer and Relaxation. *J. Chem. Phys.* **38,** 1187–1203 (1963).
33. Liao, M.-S. & Scheiner, S. Electronic structure and bonding in metal porphyrins, metal=Fe,

Co, Ni, Cu, Zn. *J. Chem. Phys.* **117,** 205–219 (2002).

34. Blase, X., Attaccalite, C. & Olevano, V. First-principles GW calculations for fullerenes, porphyrins, phtalocyanine, and other molecules of interest for organic photovoltaic applications. *Phys. Rev. B* **83,** 115103 (2011).
35. Refaely-Abramson, S., Baer, R. & Kronik, L. Fundamental and excitation gaps in molecules of relevance for organic photovoltaics from an optimally tuned range-separated hybrid functional. *Phys. Rev. B* **84,** 75144 (2011).
36. Savenije, T. J. & Goossens, A. Hole transport in porphyrin thin films. *Phys. Rev. B* **64,** 115323 (2001).
37. Kerp, H. R., Donker, H., Koehorst, R. B. M., Schaafsma, T. J. & van Faassen, E. E. Exciton transport in organic dye layers for photovoltaic applications. *Chem. Phys. Lett.* **298,** 302–308 (1998).
38. Lyons, B. P. & Monkman, A. P. The role of exciton diffusion in energy transfer between polyfluorene and tetraphenyl porphyrin. *Phys. Rev. B* **71,** 235201 (2005).
39. Yamashifa, K., Harima, Y. & Iwashima, H. Evaluation of Exciton Dlff usion Lengths and Apparent Barrier Widths for MetaVPorphyrin Schottky Barrier Cells by Use of the Optical Filtering Effect. *J. Phys. Chem* **91,** 3055–3059 (1987).
40. Cerullo, G. *et al.* Ultrafast Förster transfer dynamics in tetraphenylporphyrin doped poly(9,9-dioctylfluorene). *Chem. Phys. Lett.* **335,** 27–33 (2001).
41. Huijser, A., Savenije, T. J., Kroeze, J. E. & Siebbeles, L. D. A. Exciton Diffusion and Interfacial Charge Separation in meso-Tetraphenylporphyrin/TiO2 Bilayers: Effect of Ethyl Substituents. *J. Phys. Chem. B* **109,** 20166–20173 (2005).

CHAPTER 6
DESIGN OF FUNCTIONAL GATE: Ion-doped sol-gel derived silicate film

In this chapter, the tailored electronic gate platform represented by ion-doped sol-gel derived film is introduced. The film provides a huge degree of freedom for designing physical and chemical properties of the gate (dielectric) materials by controlling the doping concentration or the annealing temperature as a back-end sol-gel process step. Various analysis in this chapter verify that this amorphous gel film could be classified as a dielectric composite material which shows distinct polarization characteristics. From these results, I envision diverse applications performed on transistors in response to different stimuli.

6.1 Composite sol-gel film as a functional gate

As reported in the previous chapter, the gate material covering the oxide layer of conventional MOSFETs can significantly modify the device characteristics. From the material point of view, there is a large choice which distinct set of characteristics from non-polar/polar dielectric to ferroelectric. However, composite materials which is designed by researchers for particular purposes (*e.g.,* programmable materials[1–3]) can extend the range of materials usage. Also, nature inexhaustibly inspires researchers to develop artificial smart devices that mimic not only macroscopic structure, but also its complex electronic or optical dynamics[4] and intelligence[5–7] of nature.

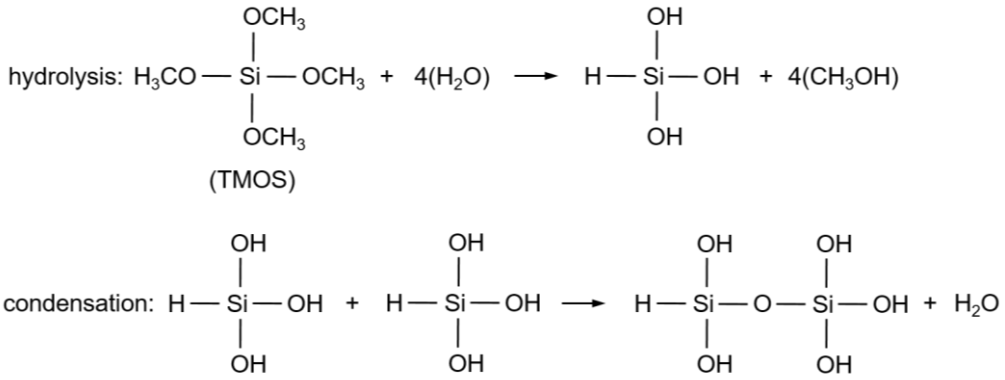
This current trend requires a stable, but functionally flexible hardware platform where multiple reactions or phase (or state) transition are performed by stimuli (energy). Among various candidates, solution-gelation (sol-gel) derived material is powerful and versatile tool to realize multiple functionalities at relatively low cost[8,9]. At the stage of 'sol' (liquid state), various materials can be mixed with sol-gel precursors and after gelation process, glass-like sol-gel derived material is obtained with high porosity depending on the choice of precursors, encapsulating various dopants such as single molecule, polymer or intracellular units[10–15] to even ionic liquid[16]. Thus, tailored materials can be synthesized by doping the encapsulated materials. Although many studies have focused on bio-[13,17,18] and optical applications[19] using effective entrapment functions of sol-gel derived materials, in other words, we can exploit it as an active living platform like cytoplasm within a living cell.

Therefore, a sol-gel derived matrix has several advantages as a gate material:

(i) dielectric property of *silicate* based sol-gel is compatible with SiO_2 dielectric layer in the MOSFET.
(ii) solution based sol-gel formation is simply implemented in CMOS process step. Sol-gel film can be formed as a back-end process using coating method (spin-coating or drop casting, etc.). Also it is low-temperature process ($\leq$ 100 ℃ in general).
(iii) on-chip *multiple* functionalities activated by different stimuli can be easily realized by various dopants. The silica framework grows around the dopants without leaching of the dopants[18]. This provides huge degree of freedom in designing the tailored devices and controlling the gate potential of the device.
(iv) it is transparent in the UV and visible spectral range. Therefore, optical properties like absorption, fluorescence or luminescence of dopants directly affects to the devices without any interrupt induced from the sol-gel platform.
(v) mechanically robust and chemically inert film is can be formed.

Therefore, the sol-gel derived materials have a great potential to extend the function of transistors beyond conventional digital switching or sensing applications, by combining with transistors.

Overview of sol-gel process



Scheme 1 Polymerization reactions (hydrolysis and condensation) of sol-gel precursor

Solution state before gelation, so-called "sol", is formed by hydrolysis and condensation process steps. Liquid alkoxide precursors such as tetraethoxysilane (**TEOS**, $Si(OC_2H_5)_4$,) or tetramethoxysilane (TMOS, $Si(OCH_3)_4$), are hydrolyzed by mixing with water (see Scheme 1). The hydrate silica tetrahedra reacts each other to form SiO_2 polymeric networks. Since the cross-linking is relying on the pH of the solution, acidic or basic solution is added in sol-gel precursor solution. Previous studies show that the acidic condition in hydrolysis and condensation process support the linear polymerization[20] and basic condition grows the size of particles in gel networks[21]. This basic procedure forms inorganic gels which have some drawbacks like low mechanical strength and low dimension of pores after densification process[22]. Therefore, organically modified precursors (organosilane), *e.g.* methyltrimethoxysilane (**MTMS**, $CH_3Si(OCH_3)_3$), are used to improve mechanical properties. During the hydrolysis process, organic precursors are introduced in inorganic one to form organic/inorganic hybrid silica network. For example, MTMS has hydrophobic and non-hydrolysable methyl group (CH_3), final sol-gel derived network has higher porosity and network complexity due to the loose polymerization[11,23,24].

At this stage, dopants are added to the solution as well and the pH condition of the sol or the usage of extra buffer solutions should be optimized depending on the type of the dopants. For example, since high acidic condition can deform some kinds of dopants like biomolecules, higher pH of the precursor solution without alcohol is required in this case. The porosity, polarity and mechanical properties of the sol-gel matrix is decided by the

processes of the hydrolysis, and condensation as well as type of precursors, water ratio, temperature, pressure, drying and curing[13].

Sol-gel derived thin-film is advantageous in many applications, especially when it should be implemented with other material platforms. Fast interaction is available due to the short diffusion path of the thin film. Thin-films are prepared by various spinning method such as spin- or dip coating. The thickness of the film, dependent on the gelation process, is strongly affected by the ratio and type of organosilane (*e.g.* MTMS) and pH of buffer solutions that are major factors for viscosity of the solution.

Under consideration of the key factors that decide the physical properties of sol-gel matrix, TMOS and MTMS mixture is chosen as sol-gel precursors (see **Section 3.2.2**) to obtain a high porosity that can provide a net of moving paths for dopants upon various stimuli. TMOS/MTMS ratio (3:2) is decided based on a preceding study[14] that minimize leaching of dopants from the sol-gel matrix. To effectively manipulate the polarization of the sol-gel derived gate material under electric or optical stimuli, highly water soluble hydrate metal salts ($Cl_2Ni \cdot 6H_2O$ and $Cl_2Cu \cdot 2H_2O$) are doped into the sol-gel film. In the solution, the metal salts are ionized and the cations and anions from the ionic compound can be trapped in the solid state to enhance the polarization of the film. The drying process is performed in the vacuum condition in order to avoid the unwanted contamination. The surface of the SiO_2 substrate to be covered with sol-gel film is activated by air plasma before spin-coating, to form hydroxyl groups on the surface which enhances the adhesion. The sample preparation detail is shown in the **Section 3.2.2** and **3.4**. The physical property of the film depending on ionic concentration and drying temperatures will be discussed in the following.

6.2 Morphology of sol-gel derived film

Figure 6.1 shows the morphology of the sol-gel derived film coated on the SiO_2 substrate. The film is formed with the 7000 rpm of spin coating speed and 100 ℃ of drying temperature. On the film surface, few tens of micro-meter flakes are observed which is not completely separated from the film (Figure 6.1(a)). This can be because of the long spin-coating time which increases surface roughness[25]. In the nano-scale, however, the film-roughness is not so critical (Figure 6.1(b)). The thickness of the film is around 2 μm as shown in the Figure 6.1(c). With lower coating speed, the significant variation in the

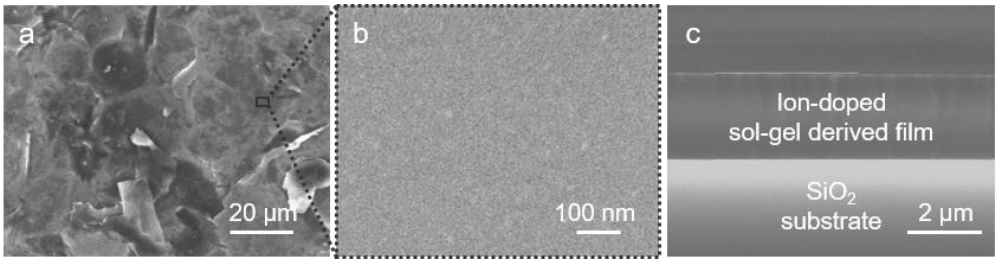


Figure 6.1 SEM image of (a,b) the surface and (c) the cross section morphology of the sol-gel derived film on the SiO_2 substrate.

film thickness was not observed. To get a thinner film, therefore, the volume and the type of the various buffer solutions (*e. g.* ethanol or water) need to be analyzed.

To understand the chemical bonding in the film affected by metal salts, X-ray photoelectron spectroscopy (XPS) analysis was conducted (Figure 6.2(a)). The clear changes after adding metal salts in the film are the broadening of carbon peak (C 1s) and slight oxygen peak (O 1s) shift. In general, this result is interpreted as increased C=O bonds. Also, Cu $2p^3$ and small Ni $2p^3$ peaks are shown after doping with 100℃ of drying temperature. Although the new peaks of Cu $2p^3$ at 931 eV and Ni $2p^3$ at 852-853 eV (blue) might imply the formation of CuO or NiO, those peaks are also shown in the cases of metal ions or pure solid metal and oxide peaks tend to be shifted to have higher binding energy[26,27]. Cu and Ni peaks are not shown in the sample with 25℃ of drying temperature. When the drying temperature is high, shrinkage of the film is expected. Therefore, inner bonding or component inside of the film is more likely to reveal on the data with higher temperature. Cl peaks are not observable in several analyses. Therefore, there is no clear evidence that Cu and Ni or Cl have formed covalent bond with sol-gel matrix. No remarkable change of Si 2p peak implies more or less the metal doping does not affect Si-O bonding. The limitation of the XPS measurement is that the even though X-ray can penetrate few micrometers, only electrons near the surface can be emitted without losing energy. Therefore, this analysis is close to surface analysis of the film.

Figure 6.2(b) shows X-ray diffraction (XRD) analysis to verify the crystallinity of the sol-gel film. In the bare SiO_2 data, strong peak observed near 32 deg. is from Si crystal under the SiO_2 substrate. This peak is also shown in all other samples using same substrate. The film has just very broad spectra depending on 2θ without any kind of peaks. This broad band is normally observed in amorphous structure like glass. Regardless the

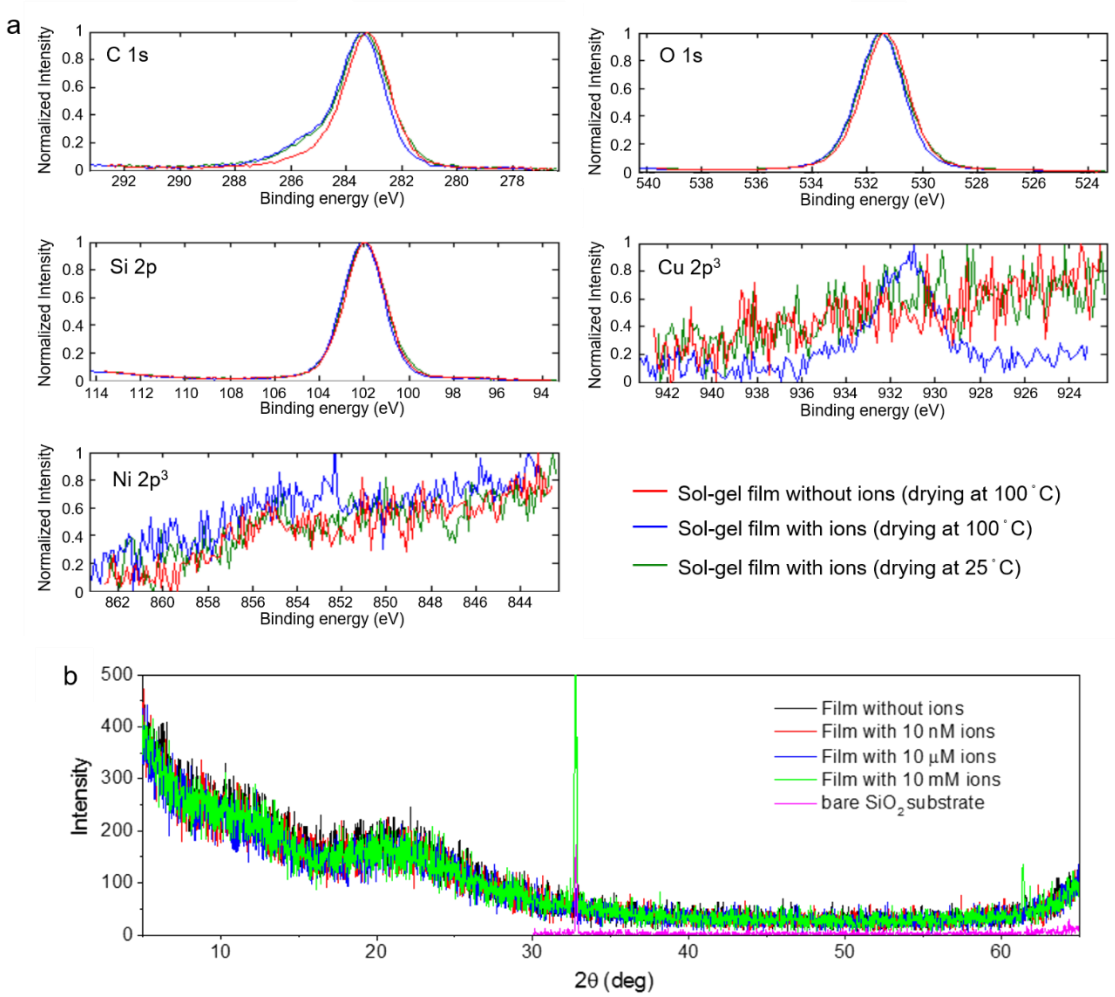


Figure 6.2 (a) X-ray photoelectron spectroscopy (XPS) of the film with various drying temperature (10 mM of ion concentration). (b) X-ray diffraction (XRD) analysis with various doping concentration of the film (drying at 100 ℃).

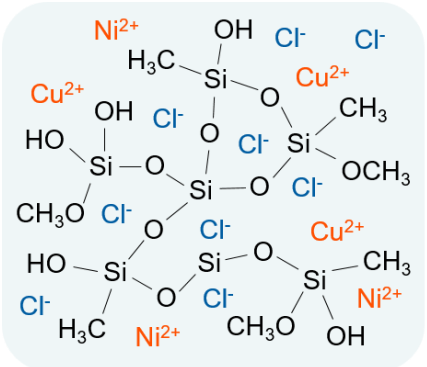


Figure 6.3 Chemical structure of the sol-gel derived film

concentration of doped metal ions, the film forms an amorphous silicate polymeric matrix. Based on above microscopic and spectroscopic analyses, metal ion doped sol-gel derived silicate film is non-crystalline amorphous film with little or no metallic bonding.

Based on the X-ray analyses and the established sol-gel derived matrix structure from preceding studies, the chemical bonding structure is illustrated in Figure 6.3. The film forms polymeric organo-silicate matrix including methyl ending groups which gives high polarizable property to the film. The doped ions are mostly weekly bound to the matrix, and hence, have a mobility in the case of the stimuli.

6.3 Dielectric properties

Dielectric property of the film plays a decisive role in the field-effect transistor devices. Critical functionalities of the transistors like memory, stimuli- or time dependent modulation, are determined by gate dielectric materials. Figure 6.4 shows dielectric constant which is extracted from the measured capacitance value depending on the frequency. In this section, film was dried at room temperature. The ion doping concentrations in the film samples are varied from 100 pM to 10 mM. In high frequency range (1 kHz – 1 MHz), the dielectric constant is around 20 to 30 regardless of doping concentration. With lower signal frequency under 100 Hz, evident concentration dependency is observed. High ionic concentration causes higher dielectric constant of the film up to 120 in the case of 10 mM of ion concentration. In general, net polarization decreases as frequency increases, and therefore, dielectric constant drops. Compared to the dielectric constant of SiO_2 (3.9) or Silicon (11.68), the sol-gel derived film is highly polarizable material. The dielectric constant of the film is in the similar range with some solutions such as methanol (30) or water (30-80). The mixing of MTMS precursor and the metal ions in the film contribute to increase the polarizability.

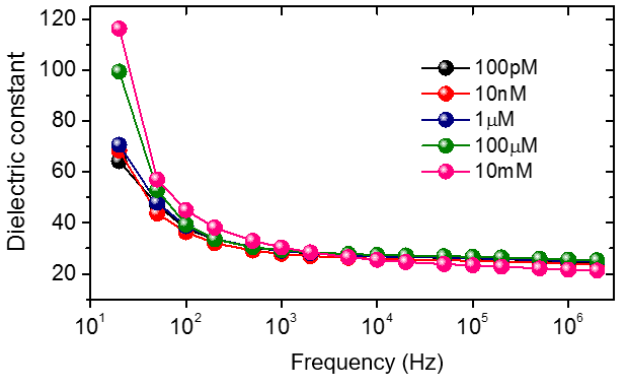


Figure 6.4 Extracted dielectric constant of the metal ion doped sol-gel derived film with various doping concentration versus frequency.

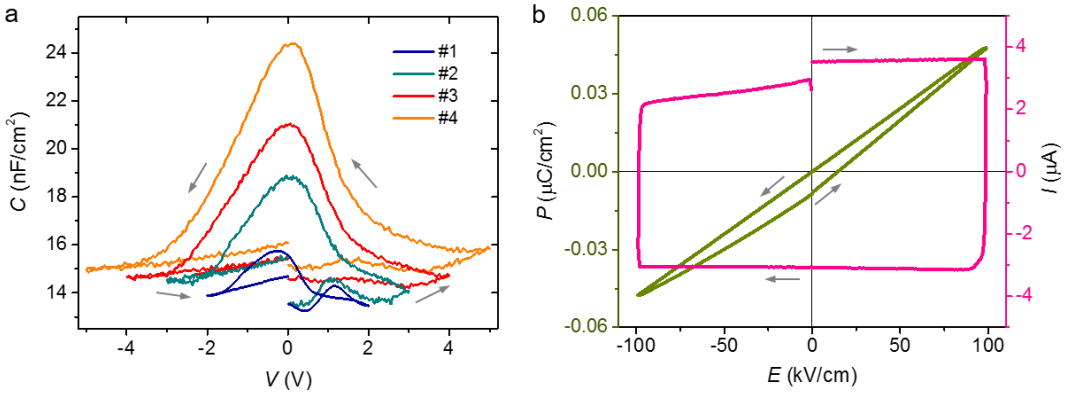


Figure 6.5 Polarization characteristics. (a) *C-V* characteristics of a sol-gel derived film by time. #1 - 4 indicate the order of the measurement at 20 sec interval. (b) *P-E* hysterisis loop and corresponding current measurement. (a) and (b) are measured with 1 kHz frequency.

Figure 6.5(a) shows a key dynamic characteristics of the metal ion-doped sol-gel derived film: time dependent polarization change. The capacitance of the film is analyzed under voltage sweep in various range. The concentration of metal salts is fixed as 10 mM. The maximum value of applied voltage increases for each curve which is measured at 20 seconds interval in numerical order. The first curve (navy) shows clear butterfly shaped two capacitance peaks during voltage sweep, as if it has ferroelectric property[28,29]. Normally this type of curve is observed when the transition of polarization direction occurs. As applied voltage range is larger, the capacitance peak at positive voltage is reduced and the peak at negative voltage is shifted to 0 V and becomes broadened and larger (orange). Also, as time passes by, initial capacitance level ($V = 0$ V) also increases. After considering all these changes, the charge accumulation capacity is increasing by voltage and time as well. That could be not only from (i) the increase of dipolar and ionic polarization, but also (ii) active movement of ions in the film by applied field which can trap electrons near the electrodes. Figure 6.5(b) supports this explanation. Although polarization curve (green) resembles the non-linear lossy dielectric material in this measurement, the corresponding current measurement (pink) for polarization shows that the current level, in other words, the flow of electrons, is continuously reduced by time (following the loop from the top at 0 kV/cm). This result also underpins the charge trapping by the film.

6.4 *Electrical properties*

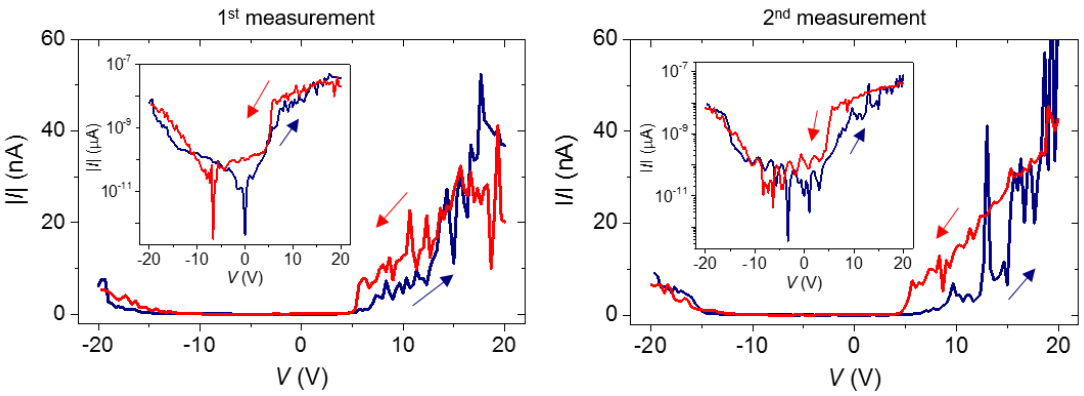


Figure 6.6 Electrical characteristics of the ion doped sol-gel derived silicate film.

Direct current *I-V* curve of the ion doped silicate film is analyzed to figure out the electrical characteristics such as a hysteresis of conductance which is typically shown in memristors (Figure 6.6). The film shows noisy current characteristics on the repeat of the measurements. Low mobility of electrons during hopping process in the amorphous film, large number of trap states (*i.e.* ions), and rough surface disturb stable current flow. Even though strong noise is consistently observed, hysteresis loops and the pinched property (at -10 V to 5 V) are observed. Without sweep (navy), a diode behavior occurs with abrupt current increase in the positive voltage range. This diode behavior is asymmetric, so that the current enhancement in negative branch is weak and requires higher potential (~ -12 V). The butterfly like loops (inset of Figure 6.6) imply that the film has resistive switching (also called "memristive") characteristics [30–33]. In addition, this curve has similarity with nanoionics devices where ions are moving through the oxide layer and forming the ionic charge transport path depending on the applied voltage condition[34]. This also shows that the ions movement plays an important role in the ion-doped sol-gel derived silicate film. Compared to typical resistively switching nanodevices constructed with crystalline oxide film, the sol-gel derived silicate sample has poor reproducibility and high noise which are caused by irregular film morphology.

Therefore, the film itself would not be an ideal candidate for electronic devices that requires stable charge carrier transport. However, such material has a great potential to be applied to transistor devices with the silicon channel used for the conductance. The film is able to supply evident memory characteristics on the basis of the stable channel

current of Si nanowire. The reason is that, as a gate dielectric material, the dielectric characteristics that can modulate the field propagation is most critical, and charge transfer characteristics is normally negligible or unwanted. However, if an oxide layer which blocks direct charge transport from gate to semiconductor channel is present on the transistor, one can exploit this distinct conduction property of the sol-gel derived film as a gate function.

6.5 Optical properties

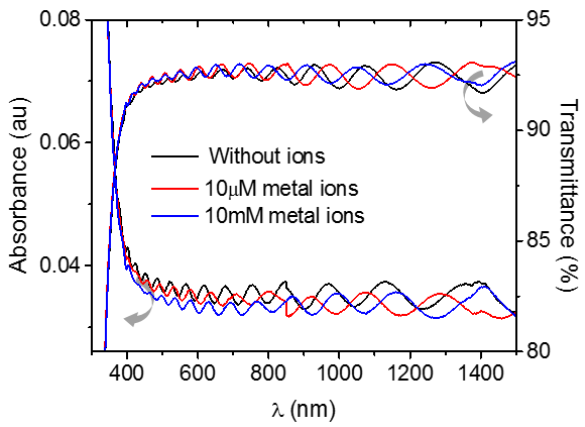


Figure 6.7 Absorbance and transmittance of the sol-gel derived film with various doping concentrations.

In order to design the viable applications of the designed sol-gel films, the optical properties should be probed as well. The absorbance and transmittance in UV/visible light range of the film is analyzed in the Figure 6.7. The film is fabricated at the glass substrate to facilitate the light penetration. The film reveals the strong absorption in the UV range, and a low level of signal absorbance in the visible and near infrared part of the spectrum. Consequently, the transmittance in visible light range is more than 92 %. With various doping concentration, the optical characteristics stays consistent. The oscilation-like perturbation of the spectroscopic data is typical property of the thin-film. This spectrum shows that most of light will directly penetrate the film without significant absorption and reach the substrate (or nanowire device in the case of hybrid device). However, important coupling between photon and components of the film (apart from absorbance) or photoelectron transport cannot be identified with this analysis. A close look at optoelectronic coupling could be determined by electrical analyses.

6.6 Conclusion

Metal ion-doped sol-gel derived silicate thin film is synthesized and analyzed using various spectroscopic and electrical methods. The advantage of organosilane-mixed sol-gel derived matrix such as high porosity or encapsulating capacity, can be actively implemented to design the gate functionality. To obtain the flexible polarization property, metal salts are added in the sol-gel precursor solution. Although the film shows high roughness, spectroscopic results support that the free metal ions are mobile in the film. Due to the ions mobility and the highly polarizable sol-gel matrix, the film shows large dielectric constant and voltage- and time dependent capacitance change. Also, resistive switching behaviors of the film implies that the memory applications would be available combining with transistors. Finally, the film is optically transparent in visible light range. The applications using those properties will be discussed further in **Chapter 7** and **8**.

References

1. Make Your Own World With Programmable Matter - IEEE Spectrum. Available at: https://spectrum.ieee.org/robotics/robotics-hardware/make-your-own-world-with-programmable-matter. (Accessed: 16th February 2018)
2. Erb, R. M., Sander, J. S., Grisch, R. & Studart, A. R. Self-shaping composites with programmable bioinspired microstructures. *Nat. Commun.* **4,** 1712 (2013).
3. Cui, T. J., Qi, M. Q., Wan, X., Zhao, J. & Cheng, Q. Coding metamaterials, digital metamaterials and programmable metamaterials. *Light Sci. Appl.* **3,** e218–e218 (2014).
4. Meredith, P., Bettinger, C. J., Irimia-Vladu, M., Mostert, A. B. & Schwenn, P. E. Electronic and optoelectronic materials and devices inspired by nature. *Reports Prog. Phys.* **76,** 34501 (2013).
5. Prezioso, M. *et al.* Training and operation of an integrated neuromorphic network based on metal-oxide memristors. *Nature* **521,** 61–64 (2015).
6. James, C. D. *et al.* A historical survey of algorithms and hardware architectures for neural-inspired and neuromorphic computing applications. *Biol. Inspired Cogn. Archit.* **19,** 49–64 (2017).
7. Schuman, C. D. *et al.* A Survey of Neuromorphic Computing and Neural Networks in Hardware. (2017).
8. Ciriminna, R. *et al.* The Sol−Gel Route to Advanced Silica-Based Materials and Recent Applications. *Chem. Rev.* **113,** 6592–6620 (2013).
9. Owens, G. J. *et al.* Sol–gel based materials for biomedical applications. *Prog. Mater. Sci.* **77,** 1–79 (2016).
10. Jin, W. & Brennan, J. D. Properties and applications of proteins encapsulated within sol-gel derived materials. *Anal. Chim. Acta* **461,** 1–36 (2002).
11. Vidinha, P. *et al.* Sol–gel encapsulation: An efficient and versatile immobilization technique for cutinase in non-aqueous media. *J. Biotechnol.* **121,** 23–33 (2006).
12. Besanger, T. R., Brennan, J. D., Besanger, T. R. & Brennan, J. D. Entrapment of membrane proteins in sol-gel derived silica. *J Sol-Gel Sci Techn* **40,** 209–225 (2006).
13. Gupta, R. & Chaudhury, N. K. Entrapment of biomolecules in sol-gel matrix for applications in biosensors: Problems and future prospects. *Biosens. Bioelectron.* **22,** 2387–2399 (2007).
14. Carrasquilla, C., Lau, P. S., Li, Y. & Brennan, J. D. Stabilizing structure-switching signaling RNA aptamers by entrapment in sol-gel derived materials for solid-phase assays. *J. Am. Chem. Soc.* **134,** 10998–11005 (2012).
15. Kassal, P., Šurina, R., Vrsaljko, D. & Steinberg, I. M. Hybrid sol-gel thin films doped with a pH indicator: Effect of organic modification on optical pH response and film surface

hydrophilicity. *J. Sol-Gel Sci. Technol.* **69,** 586–595 (2014).

16. Néouze, M.-A., Le Bideau, J., Gaveau, P., Bellayer, S. & Vioux, A. Ionogels, New Materials Arising from the Confinement of Ionic Liquids within Silica-Derived Networks. *Chem. Mater.* **18,** 3931–3936 (2006).
17. Wencel, D., MacCraith, B. D. & McDonagh, C. High performance optical ratiometric sol-gel-based pH sensor. *Sensors Actuators, B Chem.* **139,** 208–213 (2009).
18. Monton, M. R. N., Forsberg, E. M. & Brennan, J. D. Tailoring sol − gel-derived silica materials for optical biosensing. *Chem. Mater.* **24,** 796–811 (2012).
19. Klein, L. C. *Sol-gel optics : processing and applications*.
20. Hench, L. L. & West, J. K. The Sol-Gel Process. *Chem. Rev* **90,** 33–72 (1990).
21. Brinker, C. J. & Scherer, G. W. *Sol-gel science : the physics and chemistry of sol-gel processing*. (Academic Press, 1990).
22. Li, X. & King, T. A. Spectroscopic studies of sol-gel-derived organically modified silicates. *J. Non. Cryst. Solids* **204,** 235–242 (1996).
23. Rao, A. V., Bhagat, S. D., Hirashima, H. & Pajonk, G. M. Synthesis of flexible silica aerogels using methyltrimethoxysilane (MTMS) precursor. *J. Colloid Interface Sci.* **300,** 279–285 (2006).
24. Hui, C. Y., Li, Y. & Brennan, J. D. Fluorescence Analysis of the Properties of Structure-Switching DNA Aptamers Entrapped in Sol−Gel-Derived Silica Materials. *Chem. Mater.* **26,** 1896–1904 (2014).
25. W, S. B., Murthy, N., Krishna, M. & Sharma, S. C. Investigation of Influence of Spin Coating Parameters on the Morphology of ZnO Thin Films by Taguchi Method. *Int. J. Thin Film Sci. Tec* **2,** 143–154 (2013).
26. Grosvenor, A. P., Biesinger, M. C., StC Smart, R. & Stewart McIntyre, N. New interpretations of XPS spectra of nickel metal and oxides. (2006). doi:10.1016/j.susc.2006.01.041
27. Mcintyre, N. S. & Cook, M. G. X-Ray Photoelectron Studies on of Cobalt, Nickel, and Copper. *Relat. Phenom* **5,** (1974).
28. Pintilie, L. *et al.* Metal-ferroelectric-metal structures with Schottky contacts. II. Analysis of the experimental current-voltage and capacitance-voltage characteristics of thin films Metal-ferroelectric-metal structures with Schottky contacts. II. Analysis of the experiment. *J. Appl. Phys.* **98,** 124104 (2005).
29. Islam Khan, A. *et al.* Experimental evidence of ferroelectric negative capacitance in nanoscale heterostructures. *Cit. Appl. Phys. Lett* **99,** 113501 (2011).
30. Lee, Y., Kim, D. Y., Lee, S. & Fu, D. Polarization-dependent Asymmetric Hysteresis

Behavior in ZnCrO Layers. *J. Korean Phys. Soc.* **60,** 1891–1896 (2012).

31. Li, H. *et al.* Memristive behaviors of LiNbO3 ferroelectric diodes. *Appl. Phys. Lett.* **97,** 12902 (2010).
32. Strukov, D. B. & Kohlstedt, H. Resistive switching phenomena in thin films: Materials, devices, and applications. *MRS Bull.* **37,** 108–114 (2012).
33. Lee, J. S., Lee, S. & Noh, T. W. Resistive switching phenomena: A review of statistical physics approaches. *Appl. Phys. Rev.* **2,** 31303 (2015).
34. Yang, R. *et al.* On-Demand Nanodevice with Electrical and Neuromorphic Multifunction Realized by Local Ion Migration. *ACS Nano* **6,** 9515–9521 (2012).

CHAPTER 7
OPTOELECTRONIC DOUBLE-GATE: Ion-doped silicate film-coated Si nanowire FETs

In this chapter, the ion-doped sol-gel derived silicate film discussed in the previous chapter is implemented on the Si nanowire transistor devices. Because of the in-plane front gate structure on a transistor chip and fin-structure of the nanowire, film-coated hybrid devices show various coupling effects such as enhanced subthreshold slope and optical double-gate effect caused by channel separation in the nanowire. Since the doped metal cations capture optically generated electrons, the negative photo-induced current switching is observed. This study demonstrates the clear evidence of the optical gate which is able to generate the electric channel in the nanowire.

7.1 Si nanowire hybrid photodetectors

Si nanowire-based photodetectors have been dramatically developed by forming hetero-structure combining the excellent electric properties of one-dimensional platforms with the optically distinctive feature of various materials from metal or quantum dot (QD) to organic materials (see Figure 7.1). Au nanoparticles decorated Si nanowire shows enhanced optical properties thanks to the coupling of surface plasmonic effect[1] or optical modes tuning by controlling absorption and scattering in gold and Si nanostructure[2]. Also, the more complex structure has been developed to detect NIR light, consisting of Si nanowire array which is covered with Au nanoparticle-decorated graphene that can

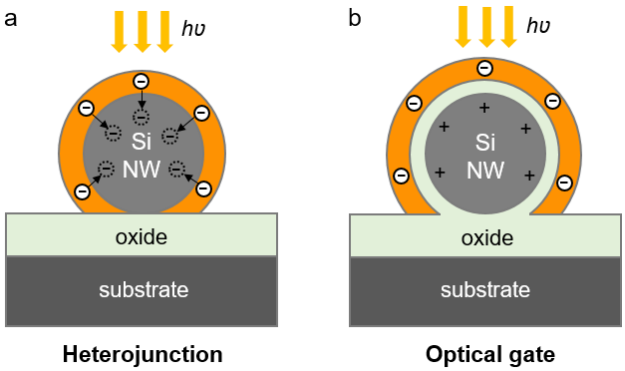


Figure 7.1 Various structures of the hybrid photodetectors such as (a) a heterojunction and (b) an optical gate.

exploit the surface plasmon of Au and enhanced detection of NIR range by graphene[1]. Similarly, the Si nanowire device with CdTe QDs showed an improvement of photocurrent in UV range[2]. These heterostructure studies support that we can tune and broaden the detecting spectra of light by decorating Si nanowire with optically characterized nanomaterials which can overcome the limitation of the band gap of Si nanowire. Meanwhile, some groups have been exploring a different approach which was an organic and inorganic hybrid photodetector. They have used direct charge-transfer characteristics from porphyrin to Si nanowire using a covalent bonding of porphyrin[3,4].

The conventional approach of photodetectors is to gain the photocurrent by exciton generation and precise bandgap engineering of the channel material to get the mobile charge from the junction material. In this case, however, a large number of photoexcited electrons is required to get enough photoresponsivity, since the photoexcited electrons are directly participating into the current flow, shown in Figure 7.1(a). Regarding that, field-effect transistors (FETs) has a great advantage for photodetection like the capability of complementary optical logic using *n*- or *p*-type transistors[5] or optical gate where the photo-induced charge generates additional gate bias[6] which is discussed in **Chapter 5** (see Figure 7.1(b)). In this case, the charge in the optically functional layer induces the opposite charge in the nanowire, and the charging dynamics also influences the induced channel current.

In this circumstances, to develop alternative photodetecting devices using optically gated Si nanowire FETs which meets the tailored requirement, sol-gel derived silicate material could be a powerful gate platform because of its advantages such as (i) flexible functionality by encapsulating various functional molecules in porous silicate matrix, (ii)

simple processing step and (iii) optical transparency discussed in **Chapter 6**. The optically functional material can be easily doped in the silicate matrix during solution preparation step. Since metal ions are excellent photoreduction agent absorbing electrons[7] , metal ion doping is a promising way to enhance the optical characteristics of the silica gels[8] or the transition metal oxide such as TiO_2[9]. Up to now, however, the electrical and optical characteristics of a hybrid system combining metal ion-doped *silicate* film and Si-based devices have not investigated yet.

7.2 Double-gate transistors

Conventional double-gate (DG) MOSFETs, where the channel current is modulated by two separated top and bottom gates, have devised to enhance the performance of the transistors, such as improved subthreshold swing, a high transconductance and reduced short channel effect which are arisen issues from scaling down of CMOS devices[10–12]. Thanks to the excellent performances of the DG device compared to a single-gate device in the initial stage, advanced structures like FinFETs[13] or gate-all-around nanowire transistors[12,14] have been successfully developed. However, the structure of the multi-gate FET, in which the gate covers different sides (top and two lateral or bottom sides) of the channel, generates the coupling effect between front and back gate (or front and lateral gate) that influences the channel formation and also induces channel separation[15,16]. Those effects are frequently observed in the *fin* structure where multiple active channels formed in the nanowires are modulated by another gate and cause threshold voltage (V_{th}) and transconductance (g_m) change. A clear hump on g_m appears due to the gradual activation of the back gate. In general, the lateral coupling appears earlier (at smaller V_g) because the interfaces are close to each other, and later the front and back gate coupling become stronger[16].

DG can also be applied to optical hybrid memory devices to program and erase the stored charge in the dielectric by second metal gate-control[17]. However, until now, DG modulation by the quantitative potential change of optically sensitive functional gate has not reported yet, and the physical phenomena in the nanowire channel with the optoelectrical DG is also not clearly explained. The optical DG study will provide strong evidence of the feasible controllability of the optical gate and how it modulates the electric field coupled with other electrical gates.

7.3 *Front and back gate coupling*

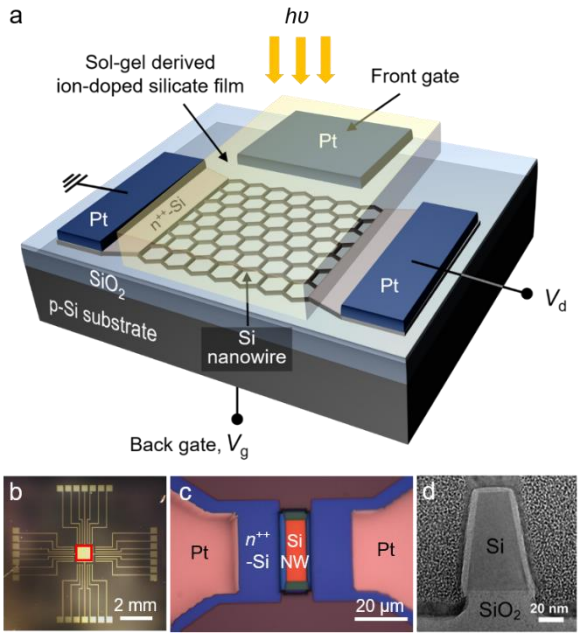


Figure 7.2 Structure of the hybrid Si nanowire FET devices. (a) Illustration of the sol-gel film coated Si nanowire FETs with front and back gate electrodes. Microscopic image of (b) the Si nanowire FET chip with a central front gate (red square) and (c) the Si nanowire active region. (d) TEM image of the cross section of the nanowire with thermally grown oxide layer.

To analyze the electrical and optical influences of the sol-gel derived film on the nanowire devices, the metal ion-doped silicate film is coated on the Si nanowire FETs by sol-gel derived method (see Figure 7.2). The general fabrication method is discussed in **Chapter 3,** and the characteristics of the film is introduced in **Chapter 6**. The honeycomb structured Si nanowire FETs are used as an electrical detecting platform because of its excellent noise characteristics in the subthreshold area[18,19]. The Si nanowire channel area is formed by electron beam lithography on an 8-inch SOI wafer and strongly doped with phosphorus (5×10^{18} cm^{-3}) to obtain junctionless-like channel operating on zero gate bias with low channel resistivity, low hysteresis, and low noise level, which is also discussed in **Chapter 4**. The *platinum* was deposited as source, drain and front gate electrodes to prevent oxidation. Only nanowire area is exposed to the air to contact the spin-coated sol-gel film. The film is dried at room temperature for 24 hours.

Figure 7.2(b) shows the configuration of the 1.5×1.5 cm^2 chip including 16 transistor devices that are sharing an in-plane central front gate electrode. The front gate electrode

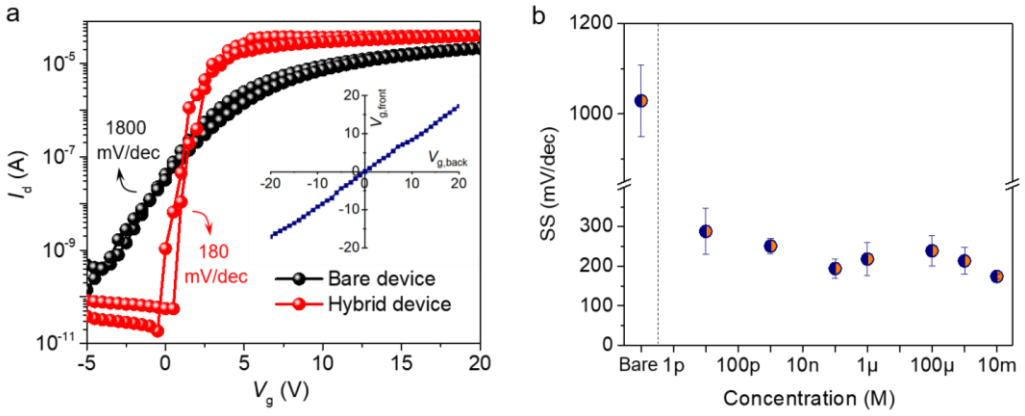


Figure 7.3 (a) Enhanced transfer characteristics of the sol-gel film-coated hybrid device (red) compared to the bare nanowire device (black). (V_d = 0.5 V) (b) Variation of subthreshold slope (SS) depending on the metal ion concentration.

does not affect the transistor behavior in the bare device without film. The orange area of Figure 7.2 (c) shows the nanowire channel region and the active Si area under the source and the drain electrode is heavily doped with phosphorus. The Si nanowire has 25 nm width (top), and 75 nm height which is more than twice of the width and the three faces of the nanowire have thermally grown 5 nm SiO_2 layer (see Figure 7.2(d)). Therefore, the cross-section of the nanowire structure is similar to the tri-gate FinFET.

Since the film is rigidly separated from the Si nanowire by a thermally grown oxide layer, the film can functionally replace the conventional metal front gate of the MOSFETs.

Figure 7.3 shows dramatically enhanced gate modulation induced by the nonlinear dielectric property of the metal ion-doped silicate film and the front-gate structure. Figure 7.3(a) shows the transfer characteristics of the bare and film-coated hybrid devices. Interestingly, the coated film enhances the subthreshold slope (SS) of the devices significantly. Bare devices have a high value of SS around 1800 mV/dec (also see the average value in Figure 7.3(b)), due to the large capacitance of buried oxide (BOX) and the Si substrate. High SS is a general drawback of using the back-gated devices and requires higher power consumption. On the other hand, film-coated devices have much smaller value, such as 180 mV/dec, which is comparable with front gated (liquid gate) devices. The inset of Figure 7.3(a) shows direct DC coupling between the back gate and the front gate. The back gate bias is linearly transformed to the front gate bias. Therefore, coupled front gate potential directly modulates the nanowire current via coated sol-gel

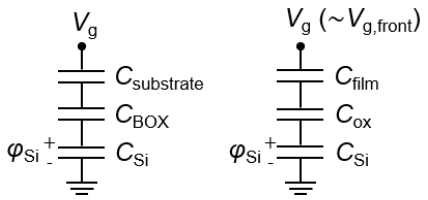


Figure 7.4 Capacitive models of bare (left) and hybrid (right) devices.

derived silicate film.

The enhanced SS characteristics is dependent on the presence and the concentration of the doped ions in the film (Figure 7.3(b)). The doped ions increase the dielectric constant (see **Chapter 6**) of the film that provides better propagation of the electric field through the film. Therefore, higher ion concentration in the film causes lower SS in the I_d-V_g curve.

The SS depends on $\frac{dV_g}{d\varphi_{Si}}$ [20] defined as,

$$\mathrm{SS_{Bare}} \propto \frac{dV_\mathrm{g}}{d\varphi_\mathrm{Si}} = 1 + C_\mathrm{Si} \cdot \left(\frac{1}{C_\mathrm{substrate}} + \frac{1}{C_\mathrm{BOX}}\right) \tag{7.1}$$

$$\mathrm{SS_{Hybrid}} \propto \frac{dV_\mathrm{g}}{d\varphi_\mathrm{Si}} = 1 + C_\mathrm{Si} \cdot \left(\frac{1}{C_\mathrm{film}} + \frac{1}{C_\mathrm{ox}}\right) \tag{7.2}$$

where φ_Si is a distinct potential applied to the Si nanowire channel, $C_\mathrm{substrate}$ and C_BOX is the bottom capacitances of the *p*-Si substrate and buried silicon dioxide (BOX), C_Si is the Si nanowire channel capacitance, C_ox is the thermally grown SiO_2 capacitance around the nanowire and C_film is the sol-gel film capacitance (*cf.* Figure. 7.4). Because of the high dielectric constant of the ion-doped sol-gel silicate film (*cf.* $\varepsilon_{\mathrm{SiO_2}} = 3.9$, $\varepsilon_\mathrm{Si} = 11.7$, $\varepsilon_\mathrm{film} \approx 20{\sim}120$, also see the **Chapter 6**), and the thickness of the each capacitor (*cf.* $d_\mathrm{substrate} = 400\ \mu\mathrm{m}$, $d_\mathrm{BOX} = 400\ \mathrm{nm}$, $d_\mathrm{film} = 180\ \mu\mathrm{m}$), C_film reduces the SS of the film-coated device which is modulated by coupled frothe nt gate. In the electric field, the doped ions are redistributed to form strong displacement between anions and cations. As a result, strongly polarizable ions in the film dramatically reduces SS.

In various sensor applications, the back gate is frequently chosen to use the area on the top of the devices for detection. The conventional wafers having thick substrate and the BOX causes large SS in the transistor devices with back gate modulation, which requires high power consumption of the transistor. In this sense, ion-doped film coating can be a good suggestion for any practical sensor platform with low power consumption.

7.4 *Optical gate coupling effects*

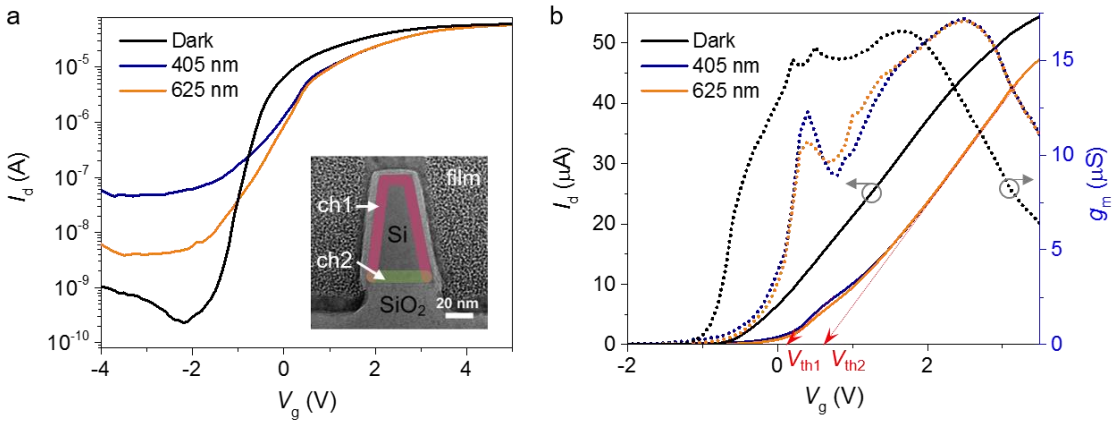


Figure 7.5 Optical gate coupling effect of the ion-doped silicate film-coated devices. (a) Transfer characteristics of the hybrid device under light illumination. Inset figure shows possible channel formations in the nanowire by optical (ch1)- and back gate (ch2). (b) Linear transfer characteristics (left black-axis) and transconductance (right blue-axis) of the film-coated hybrid device. Two different threshold voltages (V_{th1} and V_{th2}) are extracted from the I_d-V_g curve. Black lines show the electrical characteristics in the dark condition and colored lines show light responses of different wavelengths with the constant light intensity of 18.3 mW/cm^2 (V_d = 0.5 V).

The light-induced electrical characteristics of the sol-gel film-coated hybrid device is demonstrated in this section. Transfer characteristics in the dark and the light illumination with violet (405 nm) and red (625 nm) range were measured (Figure 7.5). Under the light illumination, several distinct transients in the I_d-V_g curve are observed: (i) the increase of off current (Figure 7.5(a)), (ii) the threshold voltage shift and (iii) the current hump (Figure 7.5(b)). In addition, transconductance (g_m) is calculated from the linear I_d-V_g curve, and interestingly, light illumination generates an additional clear peak in g_m apart from the general curve shift by surface charge. Using the extrapolation in the linear region method[21], shifted V_{th} can be extracted as V_{th2} (Figure 7.5(b)). The additional g_m peak and hump in the I_d-V_g curve imply that another threshold point (V_{th1}). The two threshold voltages indicate the channel separation in the nanowire (see the inset of Figure 7.5(a)) due to the coupling effect between the back gate and optical front gate. Figure 7.6 (a) illustrates major causes to change the I_d-V_g curve shape. Due to the optical transparency of the film, light can reach the nanowire by penetrating the film and generate photocurrent in the nanowire which is the dominant source of the off current increase. The stronger

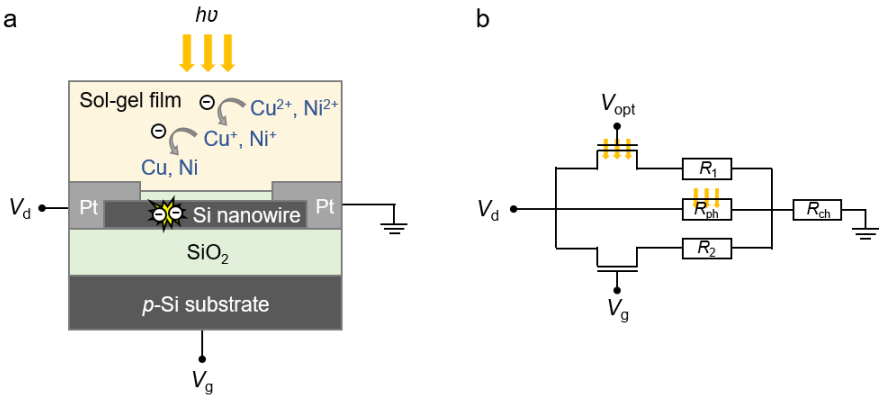


Figure 7.6 Optoelectronic double-gate effect. (a) Schematic diagram of the light-induced charging mechanism in the optical gate of the hybrid device. (b) Equivalent circuit model of the optoelectronic double gating system. (V_{opt}: optical gate bias, V_g: back gate bias, V_d: drain bias, R_1 and R_2: series resistances of the optically and electrically induced channels in the nanowire respectively, R_{ph}: photo-resistance modulated by different wavelengths, R_{ch}: other channel resistances (*e.g.* contact resistance etc.))

current growth under violet light (405 nm) shows the photoconductance property of the Si nanowire. The overall curve shift originated from photo-induced electron trapping by metal cations that provide additional negative bias around the nanowire. The metal cations acting as electron acceptors restrict the recombination of the electron-hole pair near the electrodes and retain the negative potential, namely optical gate bias.

The coupling effect between the optical front gate and the back gate shows the clear evidence that the optically sensitive film can generate a strong electrical field enabling the device modulation. In the fin-structure of the nanowire with double gates, the electric field at the corner and edge region is stronger than the body and bottom region, and the higher doping concentration also enhances channel separation[22]. Our devices have a fin-structure, and the back gate bias is coupled to the front gate via sol-gel film. In this circumstances, the light-illumination increases the number of mobile carriers in the nanowire and strengthens the electric field applied to the front edge of the nanowire. Therefore, the front channel is formed with smaller back gate bias (V_{th1}). The body channel is subsequently opened by the back gate with V_{th2}. Also, the stronger current hump is observed with 405 nm of the light compared to 625 nm. The channel separation and its conductivity are also dependent on the wavelength of the light by generating different front gate biases.

The equivalent circuit model summarizes the channel separation in the optoelectronic double-gate device (Figure 7.6(b)). The optical front gate (V_{opt}) and the back gate (V_g) separately modulate the channel conduction where V_{opt} is the coupling bias induced by V_g and photo-induced charge in the film. Resulting I_d can be presented as a sum of optically gated edge channel current (I_1), back (front-coupled) gated body channel current (I_2) and photocurrent (I_{ph}) which is given by,

$$I_d = I_1 + I_2 + I_{ph} \tag{7.3}$$

In the dark condition, the component of I_d is only induced by back gate without any optical coupling effect.

7.5 *Optical current switching characteristics*

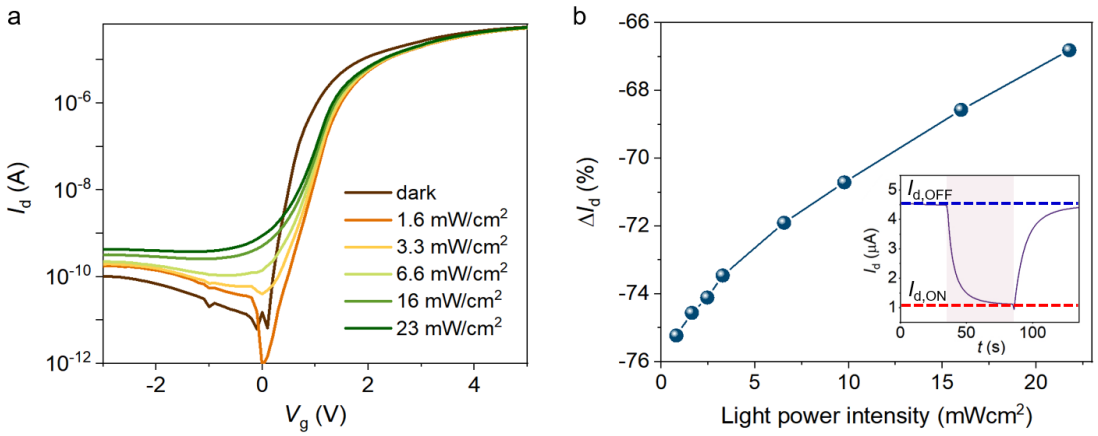


Figure 7.7 Optical current switching characteristics. (a) Transfer characteristics of the hybrid device under light illumination with various light power intensity. (b) The current switching ratio ($\Delta I_d = \frac{I_{d,ON} - I_{d,OFF}}{I_{d,OFF}} \times 100$ (%)) as a function of light power intensity where V_g = 1V. (V_d = 0.5 V, λ = 625 nm)

The film-coated hybrid device shows negative current switching behavior under light illumination. Figure 7.7 (a) shows the I_d-V_g curve shift under illumination. The trend of the current change has a strong similarity with the negative photoresponse of bare *n*-doped devices (Figure 4.3 and 4.5 in **Chapter 4**) such as the increase of threshold voltage and degradation of subthreshold slop[6]. Because of the high transparency of the sol-gel film (cf. Figure 6.7), the hybrid devices also shows the similar photoconductive behavior of highly *n*-doped nanowire FETs. However, the threshold voltage shift is stronger with the

sol-gel film coated device compared to the bare devices. The electron entrapment of metal cations provide the consistent negative potential to the device, which increases the threshold voltage of the devices. The photocurrent change by light power intensity is shown in Figure 7.7(b). Although it is difficult to directly compare the exact number of current change ratio (ΔI_d (%)) with the bare devices in Figure 4.3 because of the different $I_{d,OFF}$ level, the increasing tendency and amount of ΔI_d in the same range of light intensity (0 - 20 mW/cm^2) are comparable with the photocurrent change of bare heavily *n*-doped device. Therefore, this switching current increasing originates from the photoexcited electron generation in the nanowire (I_{ph}). On the other hand, the current switching dynamics is strongly affected by the film (see the inset of Figure 7.7(b). The longer switching time constant is from the high capacitance of sol-gel film (cf. Figure 6.4).

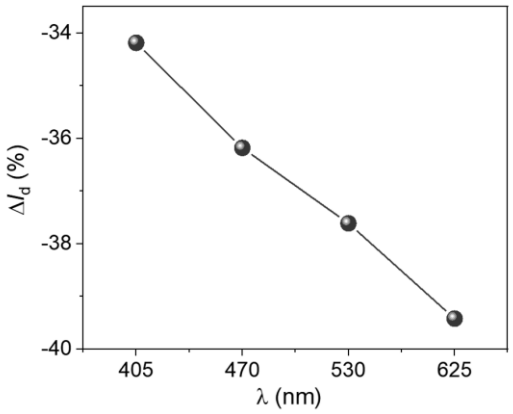


Figure 7.8 Wavelength dependence of light induced current change of the hybrid device. (V_g = 1 V, V_d = 0.5 V, light intensity is 18.3 mW/cm^2)

Figure 7.8 shows the wavelength dependency of the hybrid device, which is almost identical with the optical property of bare heavily *n*-doped devices. Since the sol-gel derived film has no distinct absorption characteristics with the visible range of the light, the hybrid devices show bare device characteristics.

7.6 Conclusion

The optical double-gate effect of ion-doped silicate film-coated Si nanowire FETs has been experimentally demonstrated. The back and front optical gate coupling of the specific *fin*-architecture of nanowire induces the channel separation. This chapter has directly shown the formed of the channel in the nanowire induced by the optical gate.

References

1. Luo, L.-B. *et al.* Light trapping and surface plasmon enhanced high-performance NIR photodetector. *Sci. Rep.* **4,** 064302–064308 (2014).
2. Tran, D. P. *et al.* Photoresponsive properties of ultrathin silicon nanowires. *Appl. Phys. Lett.* **105,** 231116 (2014).
3. Winkelmann, C. B. *et al.* Optical switching of porphyrin-coated silicon nanowire field effect transistors. *Nano Lett.* **7,** 1454–8 (2007).
4. Wen, L. *et al.* Photoelectric conversion behavior based on direct interfacial charge-transfer from porphyrin derivative to silicon nanowires. *Appl. Phys. Lett.* **97,** 253111 (2010).
5. Choi, S.-J. *et al.* Bio-Inspired Complementary Photoconductor by Porphyrin-Coated Silicon Nanowires. *Adv. Mater.* **23,** 3979–3983 (2011).
6. Baek, E. *et al.* Optoelectronic switching of nanowire-based hybrid organic/oxide/semiconductor field-effect transistors. *Nano Res.* **8,** 1229–1240 (2015).
7. Litter, M. I. Heterogeneous photocatalysis: Transition metal ions in photocatalytic systems. *Appl. Catal. B Environ.* **23,** 89–114 (1999).
8. Li, Y. *et al.* Photocatalytic reduction of CO2 with H2O on mesoporous silica supported Cu/TiO2 catalysts. *Appl. Catal. B Environ.* **100,** 386–392 (2010).
9. Chen, D. & K. Ray, A. Removal of toxic metal ions from wastewater by semiconductor photocatalysis. *Chem. Eng. Sci.* **56,** 1561–1570 (2001).
10. Wong, H.-S. P., Frank, D. J. & Solomon, P. M. Device design considerations for double-gate, ground-plane, and\nsingle-gated ultra-thin SOI MOSFET's at the 25 nm channel length\ngeneration. *Int. Electron Devices Meet. 1998. Tech. Dig. (Cat. No.98CH36217)* 407–410 (1998). doi:10.1109/IEDM.1998.746385
11. Ferain, I., Colinge, C. A. & Colinge, J.-P. Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors. *Nature* **479,** 310–316 (2011).
12. Kuhn, K. J. Considerations for Ultimate CMOS Scaling. *IEEE Trans. Electron Devices* **59,** 1813–1828 (2012).
13. Nowak, E. J. *et al.* Turning silicon on its edge. *IEEE Circuits Devices Mag.* **20,** 20–31 (2004).
14. Singh, N. *et al.* High-performance fully depleted silicon nanowire (diameter /spl les/ 5 nm) gate-all-around CMOS devices. *IEEE Electron Device Lett.* **27,** 383–386 (2006).
15. Ouisse, T., Cristoloveanu, S. & Borel, G. Influence of series resistances and interface coupling on the transconductance of fully-depleted silicon-on-insulator MOSFETs. *Solid. State. Electron.* **35,** 141–149 (1992).
16. Daugé, F. *et al.* Coupling effects and channels separation in FinFETs. *Solid. State. Electron.* **48,** 535–542 (2004).

17. Seol, M.-L., Choi, S.-J., Kim, C.-H., Moon, D.-I. & Choi, Y.-K. Porphyrin–Silicon Hybrid Field-Effect Transistor with Individually Addressable Top-gate Structure. *ACS Nano* **6,** 183–189 (2012).
18. Rim, T. *et al.* Improved Electrical Characteristics of Honeycomb Nanowire ISFETs. *IEEE Electron Device Lett.* **34,** 1059–1061 (2013).
19. Kim, K. *et al.* Suspended honeycomb nanowire ISFETs for improved stiction-free performance. *Nanotechnology* **25,** 345501 (2014).
20. Wouters, D. J., Colinge, J.-P. & Maes, H. E. Subthreshold slope in thin-film SOI MOSFETs. *IEEE Trans. Electron Devices* **37,** 2022–2033 (1990).
21. Ortiz-Conde, a. *et al.* A review of recent MOSFET threshold voltage extraction methods. *Microelectron. Reliab.* **42,** 583–596 (2002).
22. Song, J.-J., Moon, D. & Kim, O. Effects of Geometrical Fin Parameters on Transfer Characteristics in Triple-Gate Fin Field Effect Transistors. *Jpn. J. Appl. Phys.* **48,** 06FD09 (2009).

CHAPTER 8
HISTORY-DEPENDENT PSEUDO GATE: Neurotransistors for memory and learning

Neuromorphic architectures are envisioned to merge learning and memorizing functions within one unit-cell like a neuron. In this chapter, a neurotransistor is designed using a silicon nanowire device coated by an ion doped sol-gel silicate film, possessing an ability to emulate the neuronal intrinsic plasticity. The use of mobile ions enables the silicate film to act as a pseudo gate that generates plasticity and allows a short-term memory of neurotransistors. A pulsed input signal of the neurotransistor is transformed into a sigmoidal weighting of the output current resembling functionality of a neuron cell, where a membrane potential induces a sigmoidal change of ionic current. The output response is governed by the history of the input signal, stored as ionic states within the silicate film and thereby enabling the learning capability of the neurotransistor. Finally, the neurotransistor having intrinsically multiple outputs represents a building block for a fully-on-chip physical neural network system. This work is prepared to be published.

8.1 Human-made machine to mimic the human brain

The human brain has singular characteristics; it is a computing machine where both memory and processing of information are contextually performed in the same and unique active matter framework. In contrast to contemporary computers, learning and memorizing information in the brain occur simultaneously and in parallel across multiple

neurons, which are the basic unit of computing in the brain active matter. The complex parallel computing is accomplished by 1000 synaptic connections on a single neuron up to a hundred of trillion connections spanning the whole brain. The brain functionality and computation emerge as a result of collective electrical and chemical operations passing by synaptic interactions through cell-networks including neurons. The complexity of this refine machinery is far to be understood completely, and the brain research has been lively ongoing in various fields from neuroscience[1], molecular biology[2,3], medicine[4] to network science[5,6] or psychology/psychiatry[7].

The brain is fundamentally different from standard von Neumann machines, which split memory and processing of information into separated units. Conventional von Neumann architecture is restricted to solve extremely complex problems. The extra bus connections between split-ups restrict solving complex problems (like recognition, prediction or judgment of the brain), which require a huge amount of energy and materials consumption[8,9]. Going beyond the von Neumann computer, *neuromorphic architectures*[10] have been proposed borrowing the elegance of brain. They perform both learning and memorizing of information at the same time within the same functional unit, and can realize powerful brain-inspired algorithms such as deep learning[11] or memcomputing[12] at a hardware level.

Artificial neurons and *synapses*[13–31] are functional building blocks of neuromorphic architecture, although each of them plays fundamentally different roles (See Table 8.1). Their primary task is to mimic the temporal or permanent reinforcement (or attenuation) of synaptic connections, *i.e.*, short-[32,33] and long-term synaptic plasticity[34,35]. While the main function of a synapse is to assure the information flow with synaptic weighting (*cf.* the role of edges in the artificial neural networks), a neuron is in charge of the information processing, *i.e.,* learning and information storage. In this respect, most memristor-based synapses are exploiting localized conducting filaments formed with injected ions or nanoparticles by an applied voltage in pre-synaptic electrode[13–22]. Also, memristor-crossbar networks are successfully applied to design circuits for training and pattern recognition[16,18,21,22]. On the other hand, spintronic nanodevices have been launched for brain-inspired computing, such as racetrack memory to fulfill the huge memory storage of brain[23], spintronic oscillators to imitate rhythmic activity of brain[26] and memristors[24,36] as well that tunes the dynamics of resistance using spin torques[25]. Recently, synaptic

	brain	memristors /synaptic transistors	spintronics	neurotransistors (our work)
materials	biological cells[37]	oxide-based various materials[38]	ferromagnetic material[39]	silicon/ ion doped silicate composite
charge transport entity	ions[40,41]	ions, electrons[38]	spins[25]	electrons/ ions
integration (number of device units)	neuronal network (10^{11})[42]	crossbar arrays (165,000 synapses, IBM[43])	spintronic arrays[44,45] (-)	conventional CMOS integration (extendable to max. 10^{10})
response time	1 - 10 ms[34,46,47]	1ns - 10ms[13,48]	1ns - 1 µs[25]	10 - 100 ms
nonlinearity with pulsed input	sigmoid firing rate[49]	window function[50]	-	tunable sigmoid function
model Components	neurons/synapses /glia etc.[51]	synapses[52,53]	neurons[54]/synapses[55]	neurons
emulating functionality	memory storage /learning /synchronization[56–58]	memory storage /learning[15]	memory storage[36] /learning[45] /synchronization[26]	memory storage /learning /information processing

Table 8.1 Comparison between the nanoelectronic candidates for neuromorphic computing machine

transistors using either memristive channel-[28,29,31] or dielectric materials[17,27,30] have been reported. Very prominently, these transistors reveal synaptic plasticity and do resemble the functionality of synapses rather than neurons.

Intrinsic plasticity of neurons and neurotransistors

Although a synapse is a well-known element for storing memory and transmitting neuronal signals, numerous observations have proven that a critical player for learning and memorizing is a *neuron*[59–61]. The neuron can store information by modulating its intrinsic excitability, which is initiated by the change of a membrane (gate) voltage and to process information through the summation of presynaptic signals and generating new postsynaptic signals. This neuronal activity is known as intrinsic plasticity[47,62]. In contrast to synapses that can be considered as two-terminal devices, the structure of a neuron has a striking similarity to a transistor[31,63], which has the potential to emulate the intrinsic

plasticity of the neuron. Like a gate of transistors, membrane potential gated ionic channels in the neuron[41] modulate the intrinsic excitability depending on a number and activity of K^+, Na^{2+} and Ca^{2+} ion channels. Also, a neuron requires threshold voltage achieved by ionic current injection for generating a spike. Similarly, the threshold modulation is one of the key properties of transistors. The intracellular plasticity could be realized by verifying the dielectric and the channel materials of the transistors, that is relatively difficult to be considered in the two-terminal devices. If realized, this architecture would act as a *neurotransistor*, which is crucial to perform as a computing node in a complex neural network, and which is out of reach by now.

8.2 Neurotransistors with tunable memory

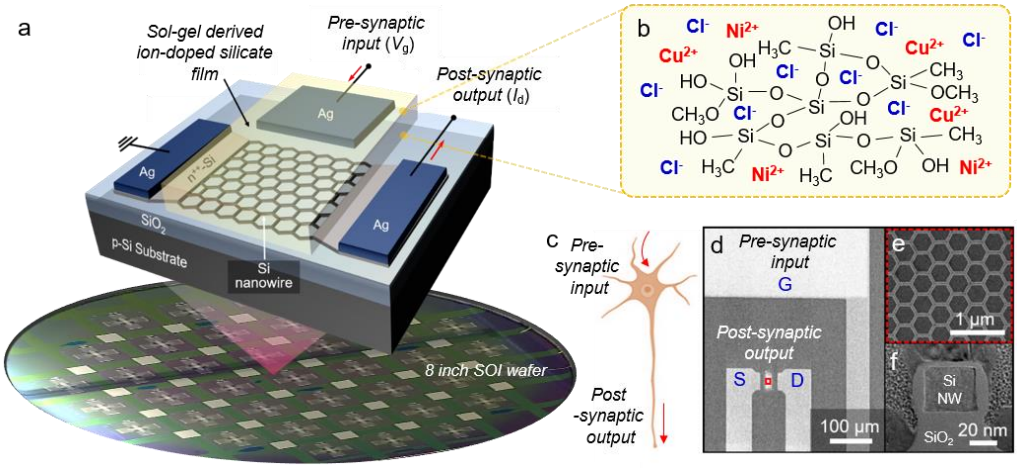


Figure 8.1 Structure of a Si nanowire neurotransistor. (a) Schematic diagram of scalable neurotransistors with pre- and post-synaptic signal transmission. (b) Chemical structure of the ion-doped sol-gel derived silicate film coated on the transistors. (c) Illustration of a biological neuron with synaptic input and output. SEM images of (d) the neurotransistor (top view) and (e) the nanowire network with honeycomb structure. (f) TEM image of cross section of nanowire.

A brain-inspired memory functionality is realized based on Si nanowire-based neurotransistors (see Figure 8.1(a)). The metal ion-doped silicate film covering both a gate electrode and a Si nanowire network (cf. **Chapter 7**) enables the emulation of neuronal intrinsic plasticity in a conventional transistor (see **Chapter 3** for device fabrication. Drying temperature for the film is 100 ℃.). Ionic sol-gel film is aimed at mimicking the local or global ionic movement through Na^{2+}, Ca^{2+} and K^+ ion channels in

a neuron, by means of metal cations (Cu*2*+ and Ni^{2+}) and Cl^- anions that are loosely captured in a polymeric silicate structure (Figure 8.1(b)). Because of doped ions, the film mimics the properties of a high-κ dielectric material that enables the device to preserve good gate coupling at a long distance between the gate and the nanowire channel (180 μm). Moreover, the ions stay mobile in the sol-gel film without chemical bonding (shown in **Chapter 6**). Figure 8.1(c) shows a biological neuron transforming pre-synaptic input signal to post-synaptic output signal by complex ionic channel activity. Similarly, a pre-synaptic input is applied to the gate (like action potential) to modulate the conductivity of nanowires, which is transferred to the post-synaptic output (Figure 8.1(d)). Thanks to a simple solution-based film-coating process, a neurotransistor with planar gate modulation could be obtained on an 8 inch SOI wafer with honeycomb-structured nanowires (Figure 8.1(d-f)).

Tunable memory

The transfer- and the output characteristics of the neurotransistor resembles the functionality of dynamic random-access memory without extra-capacitor (1T-DRAM)[64] (Figure 8.2(a)). A feature of I_d-V_g curve of the neurotransistor is a "*tunable* memory window," which is varying up to around 10 V depending on V_g sweep speed (Figure 8.2(a), inset). In comparison to 1T-DRAM cells featuring fixed memory windows[64–66], the neurotransistor can vary its charging capacity using mobile ions in the dielectric layer.

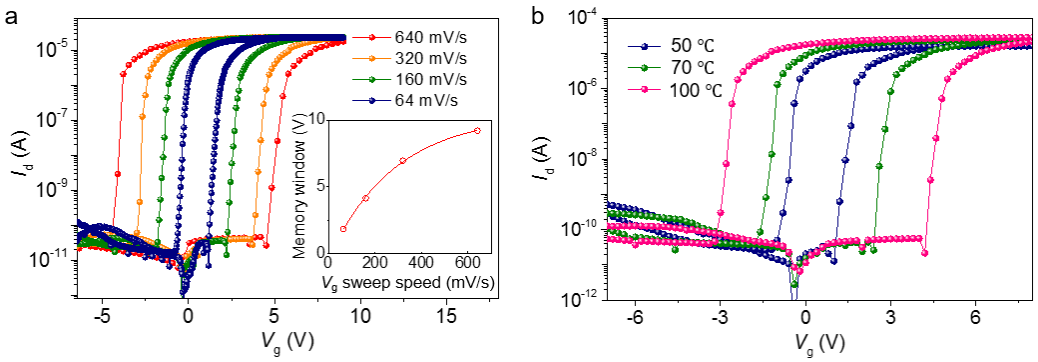


Figure 8.2 Tunable memory of the neurotransistors. (a) Transfer characteristics (I_d-V_g) of the neurotransistor with various V_g sweep speed. The memory window is shown in the inset as a function of the V_g sweep speed. (SS = 99.1±19.3 mV/dec) (b) Transfer characteristics of Si nanowire devices wrapped by sol-gel derived layers with various drying temperature. V_d = 0.5 V is applied for (a,b).

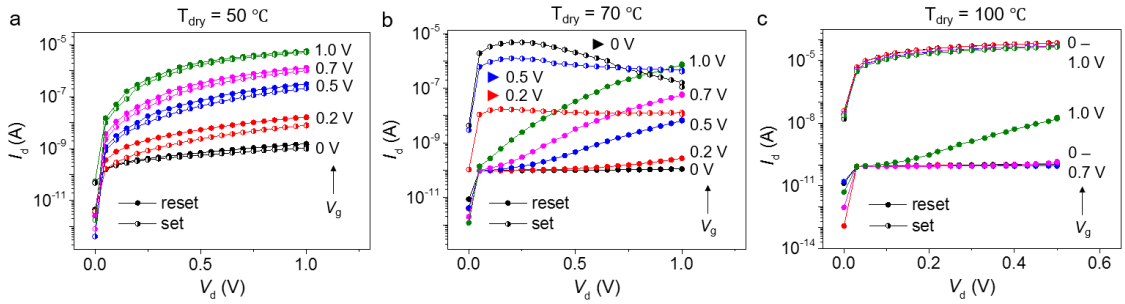


Figure 8.3 1-transistor (1T) memory functionality of the sol-gel film coated Si nanowire transistors with various drying temperature: (a) 50, (b) 70 and (c) 100 °C. ($V_{g,set}$ = 8V, $V_{g,reset}$ = -8V)

This allows the transistor to have short-term plasticity so that I_d is modulated by a frequency and width of V_g pulses, corresponding to the speed of the electric-field change around the nanowire. The average subthreshold slop (SS) of the I_d-V_g curve is 99.1±19.3 mV/dec implying that the gate coupling is comparable with ion-sensitive FETs using ion-contained liquid gate[67–69]. These results demonstrate the memory functionality of the sol-gel derived film-coated nanowire FETs.

Also, the memory capacity is tuned at the fabrication step, such as the drying temperature (T_{dry}) of the film (Figure 8.2(b) and Figure 8.3). Higher drying temperature induces a larger memory window with constant voltage sweep speed. To demonstrate the origin of the hysteresis (memory window) I_d-V_d curves are measured to analyze the current level change after the set and reset by V_g (Figure 8.3). Based on the current saturation level of the transfer characteristics, the set voltage and reset voltage are chosen as 8V and -8 V respectively. V_g in the graphs is applied to the devices right after (< 1 s) the sweeping of gate voltage from 0 V to 8 or -8 V (set or reset). With T_{dry} = 50 °C, I_d-V_d curves are modulated by V_g even after the set and reset, like conventional output characteristics of the transistor (Figure 8.3(a)). When the higher drying temperature (70 °C) is employed, I_d-V_g curves do not follow the conventional output characteristics (Figure 8.3(b)). After set, the current level is not reduced even when V_g = 0 V, but he curve shape is distorted due to the relaxation during measurement. When V_g = 0.2 and 0.5 V are applied, current levels do not follow the conventional rule (cf. Figure 8.3(a)) but still keep higher value. After reset, although I_d-V_d curves tend to increase as V_g increases, the growth of current level requires higher drain voltage. Finally, Figure 8.3(c) with T_{dry} = 100 °C shows that after the device is set, the output characteristics is maintained clear

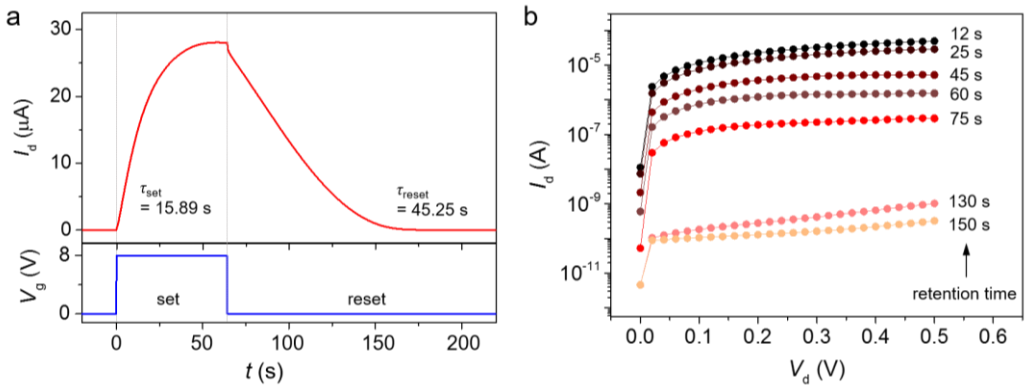


Figure 8.4 Set and reset time of memory. (a) The drain current saturation dynamics. The time constant to reach the current saturation level (V_g = 8 V, set) is 15.89 sec. The relaxation time constant (V_g = 0 V, reset) is 45.25 sec. (b) I_d-V_d curves depending on memory retention time with V_g = 0 V. The film drying temperature is 100 ℃ for (a) and (b).

high current at the level of about 10^{-5} A, even when 0 V is applied on the gate. After reset, I_d keeps off current level. Figure 8.3(c) verifies clear memory behavior of the sol-gel film-coated FET device with T_{dry} = 100 ℃. Drying temperature dependence is due to the shrinkage of the sol-gel derived matrix during the annealing process which reduces the porosity, so that ionic mobility is enhanced and more ions can be accumulated on the electrode area. In the following sections, the film dried at 100 ℃ is used for the neurotransistor.

The dynamics for the set and reset for memory is shown in Figure. 8.4(a). The neurotransistor requires τ_{set} = 15.9 s and τ_{seset} = 45.25 s (time constant for memory set and reset) for fully turning *on* and *off* the devices with V_g = 8 V and V_g = -8 V respectively. The extracted time constant is too slow for conventional reading and writing of digital memory. However, analog reading and writing (*i.e.,* programming) are available where the current level is gradually increased or decreased by V_g pulses. Figure 8.4 (b) shows the retention time of the I_d-V_g curve. In the logarithmic scale of the I_d, it takes around 150 s for fully turning-off of the device.

8.3 Intrinsic plasticity in neurotransistors

As a consequence of long reading and writing time of the neurotransistor, the I_d response (post-synaptic output) to V_g pulses (pre-synaptic input) with high pulse-amplitude (V_A = 6 V and -6 V) shows clear short-term potentiation (STP) (temporal neuronal signal

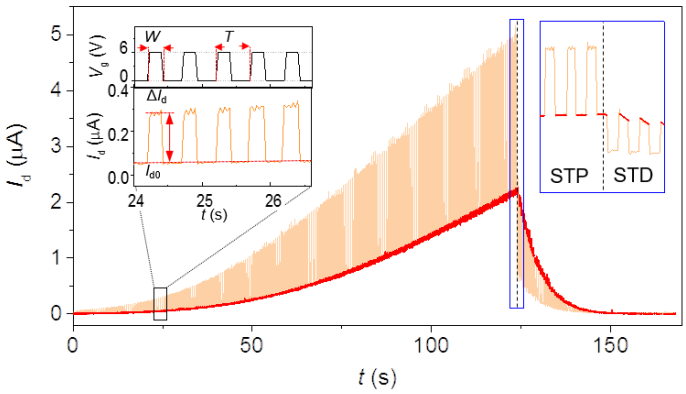


Figure 8.5 The post-synaptic output current (I_d) responding to pre-synaptic pulse-train (V_g) in the neurotransistor. T is a period of the pulses and W is a pulse width. Potentiation (increasing red line) is leaded by positive pre-synaptic pulses (V_A = 6 V, T = 500 ms and W = 200 ms) and depression (decreasing red line) is leaded by negative pre-synaptic pulses (V_A = 6 V, T = 500 ms and W = 300 ms). V_d = 0.5 V is applied.

enhancement remained milliseconds to few minutes which is induced by the diffusion driven redistribution of ions within a membrane) and short-term depression (STD) behavior (represented as an output signal reduction, and remained milliseconds to few minutes in the absence of the input pulses) respectively, as the dramatic nonlinear increase of post-synaptic current ΔI_d (Figure 8.5).

To investigate the intrinsic plasticity of the neurotransistors, we analyzed the output current (I_d) as a function of the input pulse amplitude (V_A) with fixed pulse period (T = 500 ms) and pulse width (W = 100 ms) (Figure 8.6(a)). The tendency of input signal variation is dependent on the V_A. When the weak input pulses (V_A = 1-3 V) are applied on the gate, no distinct change of ΔI_d along the input pulses is observed, but the current only shows direct pulse response by the input pulses like conventional transistor behavior. When V_A is over 4 V, the ΔI_d increases linearly as pulse number increases. This strengthening of the output signal is a signature of the STP by intrinsic neuromorphic excitability. Moreover, higher V_A (> 7 V) leads to the nonlinear growth of ΔI_d along the pulse number. Also, the nonlinear increasing of I_{d0} is observed as pulse number increases. This current weight by repeated input pulses implies that the transistor has a feature of synaptic potentiation. Similarly, the input pulse period (T) also modulates the plasticity including STP in the synaptic transistors (Figure 8.6(b)). A shorter period of the pulses leads to stronger STP and increase of ΔI_d. In conclusion, strong and frequent stimulations entering input dramatically raise output signal in the synaptic transistor.

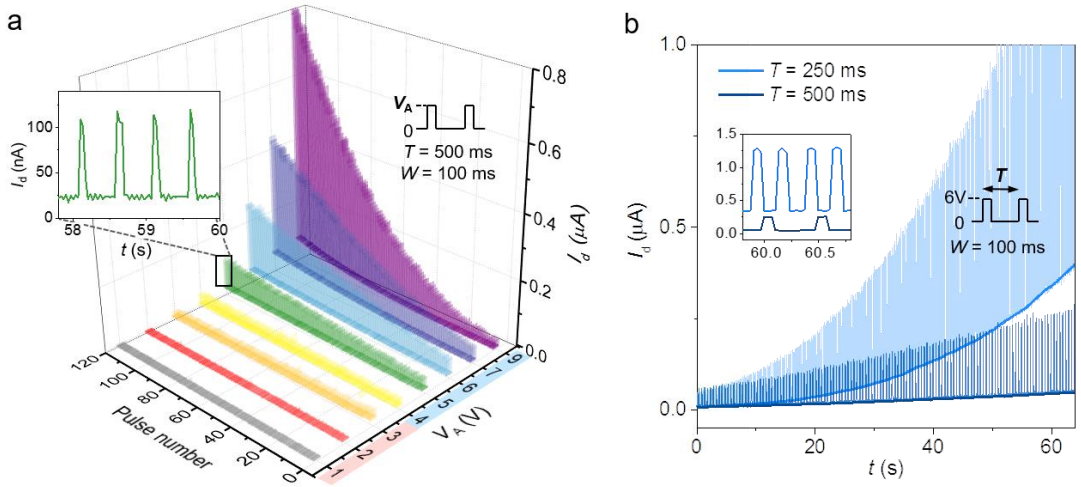


Figure 8.6 Neuroplasticity of neurotransistors. (a) Post-synaptic responses as a function of pre-synaptic pulse amplitude (V_A). Applied pre-synaptic pulse duration and width are fixed as T = 500 ms and W = 100 ms. (b) Post-synaptic potentiation depending on the presynaptic pulse duration (T). Applied pre-synaptic pulse amplitude and pulse width are fixed as V_A = 6 V and W = 100 ms. V_d = 0.5 V is applied for (a, b).

This resulting plasticity is mainly due to the ionic polarization in the sol-gel film (Figure 8.7). The diffusivity of ions decreases when the porosity of the medium increases[70]. Therefore, the mobility of metal cations and Cl^- anions is limited in the sol-gel processed silicate polymer that has higher porosity than the conventional dielectric material does[71]. If the input pulse amplitude V_A is too small to exceed ionic potential energy barrier ($E_{barrier}$), the applied pulses cannot induce a meaningful movement of ions, and the gate potential is only transferred by dielectric polarization. (Figure 8.7(i)) With this condition, the potentiation is not able to occur. On the other hand, a strong V_A can tilt the energy barrier of ions causing easier ion drift. (Figure 8.7(ii)) This gradual ionic migration generates strong ionic polarization between cations and anions. Even when the input signal is turned off (V_g = 0 V), ionic polarization is maintained because of the high diffusivity leading long relaxation time to come back to an equilibrium state. This ionic polarization keeps a certain amount of interface potential on the nanowires like a pseudo gate, causing short-term (pre-synaptic) potentiation. Also, if the next input pulses are applied before the ions return to equilibrium state (pulse duration < relaxation time), the output current continuously increases by the weighting of ionic polarization. Therefore, the strong potentiation is observed when the period of pulses is shorter. This pulse-induced ionic migration and its diffusion and polarization properties generate non-linear

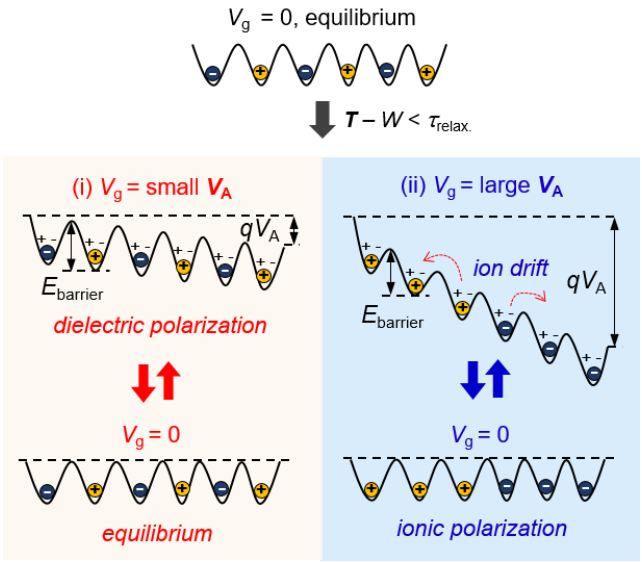


Figure 8.7 A schematic diagram showing the various polarization occured in the ion-doped sol-gel silicate film through potential energy barrier when V_g is applied. The ionic migration and energy states are shown when the pulse amplitude is (i) small and (ii) large to induce ion drift.

current operation by pulses on the transistor device. In addition, small polarity change in the film induces the strong plasticity by field-effect when combined with a transistor. This is obvious because the memristive behavior of the ion-doped film itself is not critical to induce strong potentiation, *i.e.*, memory behavior, under the same amount of electric potential (shown in Figure 6.6 of **Chapter 6**). When combined with transistors, the impact of the electrically induced response of the film is more obvious. Slight change of the polarization in the film is able to induce strong *intrinsic plasticity* in the transistors by the electrical field-effect.

Interestingly, the time evolution of the output potentiation (I_{d0}) and output peak ($I_{d,peak}$) can be perfectly fitted with a sigmoidal curve (Figure 8.8(b) and **Appendix A.4**). This is in agreement with a sigmoidal increase of the ionic current in a neuron cell[72], caused by the membrane potential (V_{memb}) (cf. Figure 8.8(a)) and which has been also well described by Hodgkin-Huxley model[73]. Here, the curve is fitted to the following sigmoidal equation:

$$I_{d0(d,peak)} = I_{d0(d,peak),max} - \frac{I_{d0(d,peak),max} - I_{d0(d,peak),min}}{1+(t/t_{0.5})^{n}} \quad (1)$$

where $I_{d0(d,peak),max}$ and $I_{d0(d,peak),min}$ are extrapolated maximum and minimum value of the entire curve respectively, and $t_{0.5}$ and n are the time constant to reach the half of $I_{d0/peak,max}$ and power coefficient (cf. Hill coefficient) respectively. This result implies that the time-dependent output signal ($\boldsymbol{O}(t) = I_d$) is a nonlinear sigmoidal function of the pulsed input signal ($\boldsymbol{I}(t) = V_g$) which decides all coefficients of the sigmoidal function (*i.e.* $\boldsymbol{O}(t) = \boldsymbol{\sigma}(\boldsymbol{I}(t))$ where $\boldsymbol{\sigma}(x)$: sigmoidal growth function). Figure 8.4(a) shows I_d reaching the saturation with constant high gate bias. It means that consistently repeated pulses with

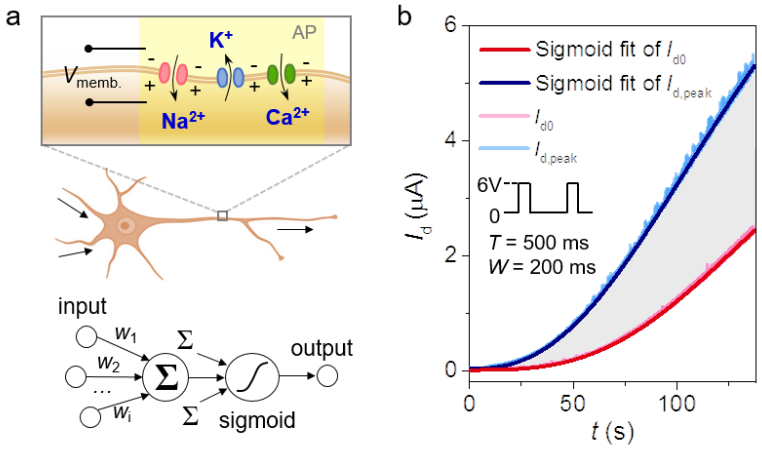


Figure 8.8 Sigmoid weight of neuron cell and neurotransistor. (a) Illustration of the ionic current modulated by membrane potential ($V_{memb.}$) change in the case of action potential (AP) spiked in a biological neuron (top) and the perceptron model of a single neuron (bottom). (b) Sigmoid function fitted output corresponding to the pulse input as a function of time.

high amplitude would induce the output saturation. In this case, there is an increase in the residual value of the ionic polarization and the actual electric potential affected on the nanowire channel increase.

The critical result of this study is that the stronger ionic polarization in the film acts similar to the increase of the membrane potential in a neuron cell, and induces a sigmoidal increase of the output current of neurotransistors. Interestingly, the neurotransistor follows such nonlinear functions depending on amplitude and frequency of the pulsed input voltage. This is the key aspect to build a controllable neurocomputing architecture which is defined by sigmoid formulas. At the same time, the sigmodal behavior of the signal is an important feature to keep the homeostatic intrinsic plasticity, which regulates ongoing ionic activities or synaptic potentiation in neurons[74]. Moreover, in models of the artificial neural network with deep learning architecture[11], the sigmoidal function is frequently used as an activation function between the input and output due to its differentiability to minimize errors[75] (Figure 8.8(a), bottom). Therefore, considering the tunable sigmoidal output response, the proposed neurotransistor is a good candidate to be employed for hardware implementation of artificial neural networks.

8.4 Emulation of memory and learning of neurons

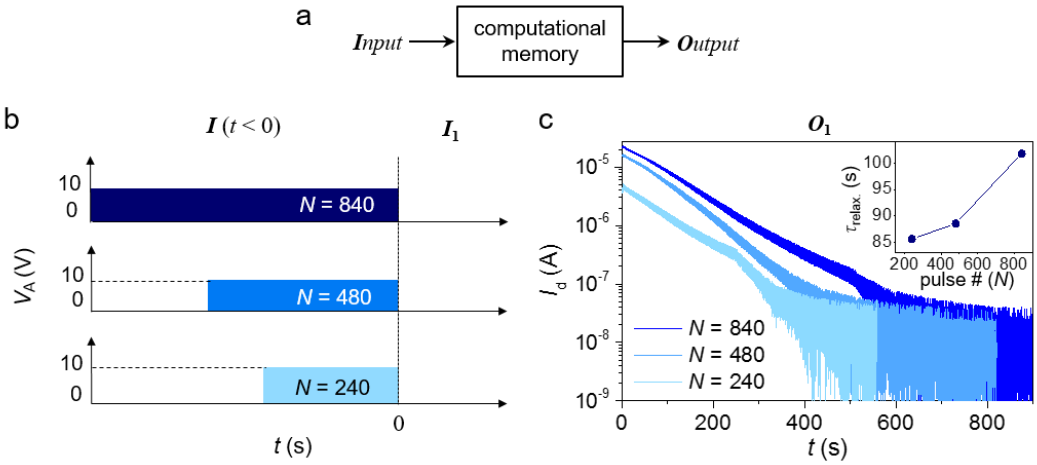


Figure 8.9 History-dependent memory in the neurotransistor. (a) A block diagram of memory dependent output corresponding to the current input in the neurotransistor. (b) The input history of the transistors over time. ***I*** ($t < 0$) implies past input before measurement. Input pulse number is varied as $N = 840$, 480 or 240, with $V_A = 10$ V, $T = 500$ ms and $W = 200$ ms in past ($t < 0$) and zero input signal is applied as a current signal ($t > 0$). (c) The output responding to the current input signals. The output signal of zero input after pulse length modulation. The inset shows the relaxation time constant depending on the past input pulse number.

Inspired by the process of information retaining in neuronal cells[76], we emulate the memory storage process of neurons on the neurotransistor modulated by a pulsed learning signal. A neurotransistor is a computing device that transforms an input signal (***I***) to output signal (***O***) depending on memory (Figure 8.9(a)). Figure 8.9(b) and Figure 8.10(b) show the time dependence of the pulsed input signal. In Figure 8.9(b), after the modulation of the numbers of pulses for learning as $N = 840$, 480 and 240, respectively, zero input ($V_A = 0$ V) is applied as a present input signal (***I***$_1$). Figure 8.9(c) shows spontaneous thermal relaxation of the output current (***O***$_1$) caused by ionic diffusion processes in the film. When the pulsed input signal is off, the spontaneous relaxation process is dependent on the stored (accumulated) memory, which is proportional to the number N of the input pulses (*i.e.*, learning times). This implies that the longer learning time leads to "better memorizing" and longer relaxation processes (Figure 8.9(c), inset). The relaxation time constant ($\tau_{relax.}$) is more than 100 s when the current level is close to the saturation level of the transistor (~24 μA). This time constant is comparable to the time scale of STP in biological neurons, that is around a few milliseconds to minutes[32].

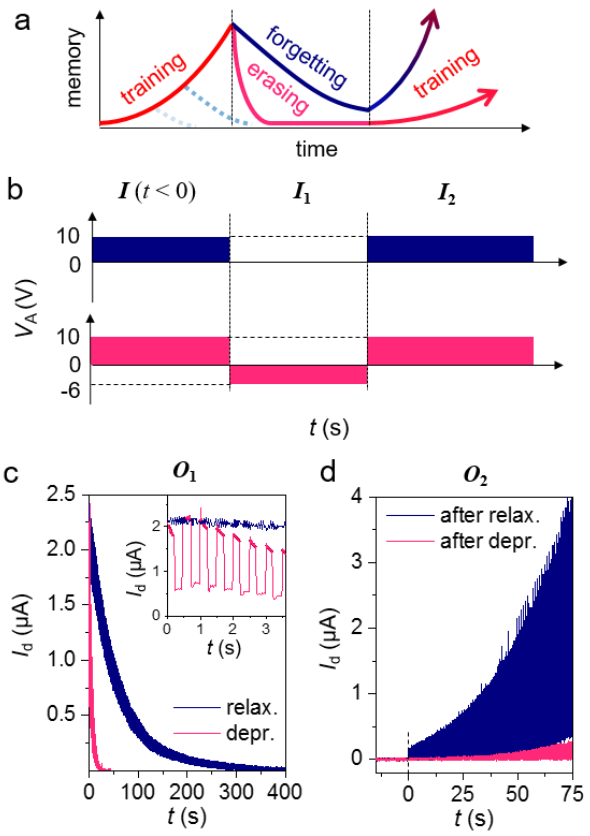


Figure 8.10 Metaplasticity of the neurotransistors. (a) Memory storage model in a neurotransistor performing the neuronal computing. The functional terms, "learning", "forgetting" and "erasing", are corresponding to potentiation, thermal relaxation and depression of neurotransistors. (b) The input amplitude is varied between zero and negative values as a current input ($t > 0$) and the past input ($t < 0$). (c) The comparison between the output current responses of zero input (relaxation) and negative pulsed input with V_A = -6 V, T = 500 ms and W = 300 ms (depression). (d) Comparison between output current responses of pulsed input signal with V_A = 10 V, T = 500 ms and W = 200 ms, depending on the history of inputs.

The relaxation is emulating the spontaneous "*forgetting*" process (memory loss) in a neuron (Figure 8.10(a)).

In Figure 8.10(b), responses of two devices with different input histories (indicated with navy and pink symbols) are compared. After a series of input pulses of constant amplitude (Phase ***I***), we applied V_A = 0 V and V_A = -6 V as the input pulses on each device (phase $\boldsymbol{I_2}$). Figure 8.10(c) shows the corresponding output currents ($\boldsymbol{O_2}$). Negative input pulses induce STD (pink curve in the inset of Figure 8.10(c)). The depression process can be used to "*erase*" information in computing (Figure 8.10(a)) which leads to a much faster

current drop than the forgetting process since the negative pulses change the direction of the ionic polarization that turns off the transistor quickly.

When the current decreases to the low level (~1 nA), equal input pulses are applied to the gate of each neurotransistor (phase $\boldsymbol{I_3}$) (Figure 8.10(b)). Interestingly, Figure 8.10(d) shows that the input history of the neurotransistor ($\boldsymbol{I}$ (t < 0) + $\boldsymbol{I_2}$) decides the forthcoming output ($\boldsymbol{O_3}$) apart from the present input signal (I_3). The much stronger current increase is observed after the relaxation process (navy curve) than after the depression process (pink curve). Precisely, the history-dependent information is stored as ionic states, such as the position and mobility of ions or ionic dipole moment, in the sol-gel derived film of the neurotransistor. The thermal relaxation of the ions in the film tends to return the ions to the equilibrium state conserving the direction of polarization that guarantees normal (or faster when the current level is high) initial learning speed. However, the depression process induces opposite ionic polarization in the film, which requires more energy to compensate for the reversed ion migration. Therefore, it requires longer learning time (*i.e.*, more pulses applied) to reach the same current level. This result demonstrates that the ionic polarization plays the key role in the unique memory and learning functionality of the neurotransistors. The stored information is hidden as ionic states in the film and not visible as the output current, but as soon as the input signal is present, different consequences are revealed depending on the accumulated input history. This behavior shows a strong similarity to the activity-dependent *metaplasticity* of biological neurons: it is not visible but remains in a cell long time as ionic or protein states and generates consequences such as synaptic plasticity[77].

Finally, using this plastic property of the neurotransistor, we form the probable memory storage model (Figure 8.10(a)). Since the neurotransistor is an analog device, the information is stored or erased as the continuous current level change by input pulses. The continuous input pulses increase the level of information storage in the transistor in the “learning” phase. The learning speed and the amount of stored memory are controlled by the number of input pulses. If the input pulses are stopped, the neurotransistor starts to lose the information in the “forgetting” phase. Also, the “erasing” phase can actively manipulate the reduction speed of the information storage level. Therefore, not only the number of pulses but also the history of information affects the learning speed.

8.5 *Intrinsically multiple output transistor*

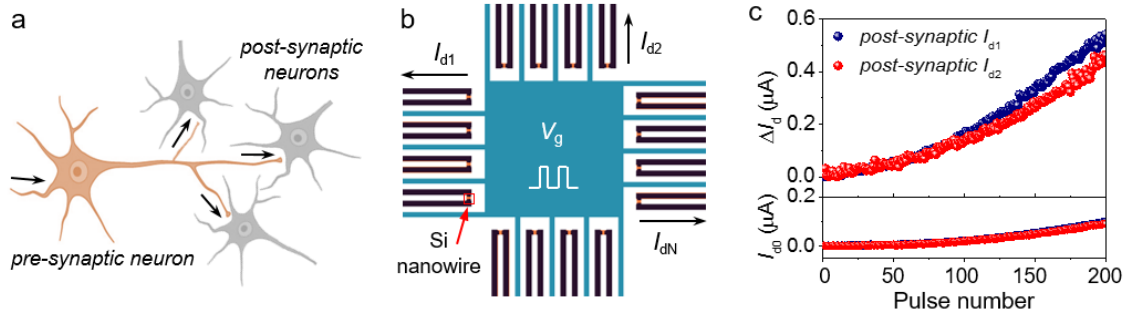


Figure 8.11 Multiple outputs of the neurotransistor. (a) Illustration of a neuron with multiple axon terminals that connects to other post synaptic neurons. (b) The actual chip design of the multiple (16) transistor outputs (I_d) with a single gate (pre-synaptic V_g on a single chip, which represents the equivalent of 16 axon terminals. This design can be extensible to N axon terminals. (c) The simultaneously measured current response (ΔI_d) and the potentiation (I_{d0}) of transistor 1 and 2. $V_A = 6$ V with $T = 500$ ms and $W = 100$ ms is applied as the pre-synaptic gate pulses.

In a biological neuronal network, extensive axon terminals of a pre-synaptic neuron transfer the neuronal signal to multiple post-synaptic neurons. This is a fundamental requirement to build a networked circuit of neurons. Using an array of neurotransistors prepared on an 8-inch wafer, we successfully emulate the multiple axon terminals for multi-neuron interconnection (Figure 8.11(a)). We designed a single pre-synaptic neurotransistor system using multiple Si nanowire channel outputs, can perform transmission to multiple post-synaptic devices (Figure 8.11(b)). On a single chip, multiple nanowire channels and central gate electrodes are connected through ionic silicate film. Therefore, multiple nanowire devices (similar to multiple axons terminals) are modulated by one pre-synaptic gate potential keeping homeostasis.

Figure 8.11(c) shows the output current values (I_d) of two separate transistors which are simultaneously measured. Since the distance between the gate and a nanowire channel is constant for all post-synaptic transistors, the potentiation (I_{d0}) of multiple devices increases with the input pulses at the same measurement time. Any inhomogeneity of the microenvironment around each device induces a slight difference in ΔI_d. This result shows a simple scheme of multiple axon terminals possibly contacting various post-

synaptic neurons which are bound by covered sol-gel film and which could be extended to a complex network using transistor-based logic and analog circuits. Furthermore, this design could be conveniently adapted to a conventional CMOS process for 3D integration.

8.6 Conclusion

Si nanowire based neurotransistors with sol-gel derived ion-doped silicate film are demonstrated. The film works as a pseudo-gate of the transistors under the modulation of a pre-synaptic gate input. Remarkably, the film doped by mobile ions enables the functionality of intrinsic plasticity and memory in neurotransistor devices. Therefore, the dielectric engineering (*e.g.*, ion doping) in neurotransistors could complement and intensify the function of memristive materials for the next-generation neuromorphic computing devices. The short-term potentiation of neurotransistors is dependent on the amplitude and period of pre-synaptic pulses. Due to the ionic polarization and diffusion in the film, the device shows a non-linear (sigmoidal) potentiation behavior, which emulates the membrane function of real neurons.

A device architecture performs the global multi-output neurotransmission, similar to a true neuron. This peculiar structure is fundamental to enable network-based connectivity in real neuronal circuits. Those can be emulated by building a network of neurotransistors.

This work represents a major step towards the interconnection between neuromorphic nanoelectronic devices and conventional Si-based CMOS systems. The developed architectures could act as a neurotransistor performing as a computing node in complex neural networks, which is out of reach by now. When combining it with memristor devices as synaptic edges, the realization of the entirely brain-inspired hardware based neuronal network becomes possible. Furthermore, the non-linear operation of the neurotransistor paves the way towards functional hardware machine learning, where the sigmoid function is self-tuned by the time-dependent input signals.

References

1. Alivisatos, A. P. *et al.* The Brain Activity Map Project and the Challenge of Functional Connectomics. *Neuron* **74,** 970–974 (2012).
2. Kandel, E. R., Dudai, Y. & Mayford, M. R. The Molecular and Systems Biology of Memory. *Cell* **157,** 163–186 (2014).
3. Mayford, M., Siegelbaum, S. A. & Kandel, E. R. Synapses and memory storage. *Cold Spring Harb. Perspect. Biol.* **4,** a005751 (2012).
4. Duman, R. S., Aghajanian, G. K., Sanacora, G. & Krystal, J. H. Synaptic plasticity and depression: new insights from stress and rapid-acting antidepressants. *Nat. Med.* **22,** 238–249 (2016).
5. Stam, C. J. & Van Straaten, E. C. W. The organization of physiological brain networks. *Clin. Neurophysiol.* **123,** 1067–1087 (2012).
6. Cannistraci, C. V., Alanis-Lobato, G. & Ravasi, T. From link-prediction in brain connectomes and protein interactomes to the local-community-paradigm in complex networks. *Sci. Rep.* **3,** 1–13 (2013).
7. Plomin, R. & Deary, I. J. Genetics and intelligence differences: five special findings. *Mol. Psychiatry* **20,** 98–108 (2015).
8. Hasler, J. Special report : Can we copy the brain? - A road map for the artificial brain. *IEEE Spectr.* **54,** 46–50 (2017).
9. Sengupta, B. & Stemmler, M. B. Power consumption during neuronal computation. *Proc. IEEE* **102,** 738–750 (2014).
10. Mead, C. Neuromorphic electronic systems. *Proc. IEEE* **78,** 1629–1636 (1990).
11. Lecun, Y., Bengio, Y. & Hinton, G. Deep learning. *Nature* **521,** 436–444 (2015).
12. Traversa, F. L. & Di Ventra, M. Universal Memcomputing Machines. *IEEE Trans. Neural Networks Learn. Syst.* **26,** 2702–2715 (2015).
13. Jo, S. H. *et al.* Nanoscale memristor device as synapse in neuromorphic systems. *Nano Lett.* **10,** 1297–1301 (2010).
14. Ohno, T. *et al.* Short-term plasticity and long-term potentiation mimicked in single inorganic synapses. *Nat. Mater.* **10,** 591–595 (2011).
15. Wang, Z. Q. *et al.* Synaptic Learning and Memory Functions Achieved Using Oxygen Ion Migration/Diffusion in an Amorphous InGaZnO Memristor. *Adv. Funct. Mater.* **22,** 2759–2765 (2012).
16. Yu, S. *et al.* A Low Energy Oxide-Based Electronic Synaptic Device for Neuromorphic Visual Systems with Tolerance to Device Variation. *Adv. Mater.* **25,** 1774–1779 (2013).
17. Zhu, L. Q. *et al.* Artificial synapse network on inorganic proton conductor for neuromorphic

systems. *Nat. Commun.* **5,** 1–7 (2014).

18. Prezioso, M. *et al.* Training and operation of an integrated neuromorphic network based on metal-oxide memristors. *Nature* **521,** 61–64 (2015).
19. Wang, Z. *et al.* Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing. *Nat. Mater.* **16,** 1–13 (2017).
20. van de Burgt, Y. *et al.* A non-volatile organic electrochemical device as a low-voltage artificial synapse for neuromorphic computing. *Nat. Mater.* **16,** 414–418 (2017).
21. Sheridan, P. M. *et al.* Sparse coding with memristor networks. *Nat. Nanotechnol.* **12,** 784–789 (2017).
22. Choi, S., Shin, J. H., Lee, J., Sheridan, P. & Lu, W. D. Experimental Demonstration of Feature Extraction and Dimensionality Reduction Using Memristor Networks. *Nano Lett.* **17,** 3113–3118 (2017).
23. Nayak, A. K. *et al.* Magnetic antiskyrmions above room temperature in tetragonal Heusler materials. *Nature* **548,** 561–566 (2017).
24. Fukami, S., Zhang, C., DuttaGupta, S., Kurenkov, A. & Ohno, H. Magnetization switching by spin–orbit torque in an antiferromagnet–ferromagnet bilayer system. *Nat. Mater.* **15,** 535–541 (2016).
25. Grollier, J., Querlioz, D. & Stiles, M. D. Spintronic Nanodevices for Bioinspired Computing. *Proc. IEEE* **104,** 2024–2039 (2016).
26. Torrejon, J. *et al.* Neuromorphic computing with nanoscale spintronic oscillators. *Nature* **547,** 428–431 (2017).
27. Lai, Q. *et al.* Ionic/Electronic Hybrid Materials Integrated in a Synaptic Transistor with Signal Processing and Learning Functions. *Adv. Mater.* **22,** 2448–2453 (2010).
28. Shi, J. *et al.* A correlated nickelate synaptic transistor. *Nat. Commun.* **4,** 56–63 (2013).
29. Tian, H. *et al.* Anisotropic Black Phosphorus Synaptic Device for Neuromorphic Applications. *Adv. Mater.* **28,** 4991–4997 (2016).
30. Xu, W., Min, S.-Y., Hwang, H. & Lee, T.-W. Organic core-sheath nanowire artificial synapses with femtojoule energy consumption. *Sci. Adv.* **2,** e1501326–e1501326 (2016).
31. Sangwan, V. K. *et al.* Multi-terminal memtransistors from polycrystalline monolayer molybdenum disulfide. *Nature* **554,** 500–504 (2018).
32. Zucker, R. S. & Regehr, W. G. Short-Term Synaptic Plasticity. *Annu. Rev. Physiol* **64,** 355–405 (2002).
33. Regehr, W. G. Short-term presynaptic plasticity. *Cold Spring Harb. Perspect. Biol.* **4,** 1–19 (2012).
34. Cooke, S. F., Bliss, T. V. P. & Cooke, S. Plasticity in the human central nervous system. *Brain* **129,** 1659–1673 (2006).

35. Lynch, M. A. Long-Term Potentiation and Memory. *Physiol. Rev.* **84,** (2004).
36. Lequeux, S. *et al.* A magnetic synapse: multilevel spin-torque memristor with perpendicular anisotropy. *Sci. Rep.* **6,** 31510 (2016).
37. Kandel, E. R. *Principles of neural science*. (McGraw Hill Professional, 2013).
38. Chua, L. If it's pinched it's a memristor. *Semicond. Sci. Technol.* **29,** 104001 (2014).
39. Locatelli, N., Cros, V. & Grollier, J. Spin-torque building blocks. *Nat. Mater.* **13,** 11–20 (2013).
40. Zonta, M. *et al.* Neuron-to-astrocyte signaling is central to the dynamic control of brain microcirculation. *Nat. Neurosci.* **6,** 43–50 (2003).
41. Armstrong, C. M. & Hille, B. Voltage-Gated Ion Channels and Electrical Excitability. *Neuron* **20,** 371–380 (1998).
42. Herculano-Houzel, S. The human brain in numbers: a linearly scaled-up primate brain. *Front. Hum. Neurosci.* **3,** 31 (2009).
43. Burr, G. W. *et al.* Experimental Demonstration and Tolerancing of a Large-Scale Neural Network (165 000 Synapses) Using Phase-Change Memory as the Synaptic Weight Element. *IEEE Trans. Electron Devices* **62,** 3498–3507 (2015).
44. Ramasubramanian, S. G., Venkatesan, R., Sharad, M., Roy, K. & Raghunathan, A. SPINDLE: SPINtronic Deep Learning Engine for Large-scale Neuromorphic Computing. *Proc. 2014 Int. Symp. low power Electron. Des.* 15–20 (2014). doi:10.1145/2627369.2627625
45. Sengupta, A., Panda, P., Wijesinghe, P., Kim, Y. & Roy, K. Magnetic Tunnel Junction Mimics Stochastic Cortical Spiking Neurons. *Sci. Rep.* **6,** 30039 (2016).
46. Neves, G., Cooke, S. F. & Bliss, T. V. P. Synaptic plasticity, memory and the hippocampus: a neural network approach to causality. *Nat. Rev. Neurosci.* **9,** 65–75 (2008).
47. Kourrich, S., Calu, D. J. & Bonci, A. Intrinsic plasticity: an emerging player in addiction. *Nat. Rev. Neurosci.* **16,** 173–184 (2015).
48. Li, Y. *et al.* Ultrafast Synaptic Events in a Chalcogenide Memristor. *Sci. Rep.* **3,** 156–166 (2013).
49. Hopfield, J. J. Neurons with graded response have collective computational properties like those of two-state neurons. *Proc. Natl. Acad. Sci. U. S. A.* **81,** 3088–3092 (1984).
50. Strukov, D. B., Snider, G. S., Stewart, D. R. & Williams, R. S. The missing memristor found. *Nature* **453,** 80–83 (2008).
51. Bezzi, P. & Volterra, A. A neuron–glia signalling network in the active brain. *Curr. Opin. Neurobiol.* **11,** 387–394 (2001).
52. Chua, L. Memristor, Hodgkin–Huxley, and Edge of Chaos. *Nanotechnology* **24,** 383001 (2013).

53. Biolek, Z., Biolek, D. & Biolková, V. SPICE Model of Memristor with Nonlinear Dopant Drift. *Radioengineering* **18,** 210–214 (2009).
54. He, Z. & Fan, D. A tunable magnetic skyrmion neuron cluster for energy efficient artificial neural network. in *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2017* 350–355 (IEEE, 2017). doi:10.23919/DATE.2017.7927015
55. Huang, Y., Kang, W., Zhang, X., Zhou, Y. & Zhao, W. Magnetic skyrmion-based synaptic devices. *Nanotechnology* **28,** 08LT02 (2017).
56. Poldrack, R. A. *et al.* Interactive memory systems in the human brain. *Nature* **414,** 546–550 (2001).
57. Buzsáki, G. *Rhythms of the brain*. (Oxford University Press, 2006). doi:10.1093/acprof:oso/9780195301069.001.0001
58. Deng, W., Aimone, J. B. & Gage, F. H. New neurons and new memories: how does adult hippocampal neurogenesis affect learning and memory? *Nat. Rev. Neurosci.* **11,** 339–350 (2010).
59. Nikitin, E. S. *et al.* Persistent Sodium Current Is a Nonsynaptic Substrate for Long-Term Associative Memory. *Curr. Biol.* **18,** 1221–1226 (2008).
60. Kemenes, I. *et al.* Role of Delayed Nonsynaptic Neuronal Plasticity in Long-Term Associative Memory. *Curr. Biol.* **16,** 1269–1279 (2006).
61. Sánchez-Aguilera, A., Sánchez-Alonso, J. L., Vicente-Torres, M. A. & Colino, A. A novel short-term plasticity of intrinsic excitability in the hippocampal CA1 pyramidal cells. *J Physiol* **59213,** 2845–2864 (2014).
62. Mozzachiodi, R. & Byrne, J. H. More than synaptic plasticity: Role of nonsynaptic plasticity in learning and memory. *Trends Neurosci.* **33,** 17–26 (2010).
63. Hasler, J. & Marr, B. Finding a roadmap to achieve large neuromorphic hardware systems. *Front. Neurosci.* **7,** 1–29 (2013).
64. Okhonin, S., Nagoga, M., Carman, E., Beffa, R. & Faraoni, E. New Generation of Z-RAM. in *2007 IEEE International Electron Devices Meeting* 925–928 (IEEE, 2007). doi:10.1109/IEDM.2007.4419103
65. Bawedin, M., Cristoloveanu, S. & Flandre, D. A Capacitorless 1T-DRAM on SOI Based on Dynamic Coupling and Double-Gate Operation. *IEEE Electron Device Lett.* **29,** 795–798 (2008).
66. Wan, J., Le Royer, C., Zaslavsky, A. & Cristoloveanu, S. Progress in Z 2 -FET 1T-DRAM: Retention time, writing modes, selective array operation, and dual bit storage. *Solid State Electron.* **84,** 147–154 (2013).
67. Cho, H. *et al.* Optimization of Signal to Noise Ratio in Silicon Nanowire ISFET Sensors. *IEEE Sens. J.* **17,** 2792–2796 (2017).

68. Rim, T. *et al.* Improved Electrical Characteristics of Honeycomb Nanowire ISFETs. *IEEE Electron Device Lett.* **34,** 1059–1061 (2013).
69. Kim, K. *et al.* Silicon nanowire biosensors for detection of cardiac troponin I (cTnI) with high sensitivity. *Biosens. Bioelectron.* **77,** 695–701 (2016).
70. Rodriguez, O. R., Gill, W. N., Plawsky, J. L., Tsui, T. Y. & Grunow, S. Study of Cu diffusion in porous dielectrics using secondary-ion-mass spectrometry. *J. Appl. Phys.* **98,** 123514 (2005).
71. Yan, Y., Hoshino, Y., Duan, Z., Chaudhuri, S. R. & Sarkar, A. Design and Characterization of Interconnected, Microporous Hybrid Thin Films by a Sol-Gel Process. *Chem. Mater.* **9,** 2583–2587 (1997).
72. Huguenard, J. R. & McCormick, D. A. Simulation of the currents involved in rhythmic oscillations in thalamic relay neurons. *J. Neurophysiol.* **68,** 1373–83 (1992).
73. Abbott, L. E. & Kepler, T. B. MODEL NEURONS: FROM HODGKIN-HUXLEY TO HOPFIELD. in *Statistical mechanics of neural networks* 5–18 (Springer Berlin Heidelberg, 1990).
74. Turrigiano, G. G. & Nelson, S. B. Homeostatic plasticity in the developing nervous system. *Nat. Rev. Neurosci.* **5,** 97–107 (2004).
75. Tino, P., Benuskova, L. & Sperduti, A. Artificial Neural Network Models. in *Springer Handbook of Computational Intelligence* 455–471 (Springer Berlin Heidelberg, 2015). doi:10.1007/978-3-662-43505-2_27
76. Sehgala, M., Song, C., Ehlers, V. L. & Moyer Jr, R. J. Learning to learn – Intrinsic plasticity as a metaplasticity mechanism for memory formation. *Neurobiol. Learn. Mem.* **105,** 186–199 (2013).
77. Wickliffe C. Abraham. Metaplasticity: tuning synapses and networks for plasticity. *Nat. Rev. Neurosci.* **9,** 387–399 (2008).

CHAPTER 9
CONCLUSION AND OUTLOOK

9.1 Conclusion

The previous chapters have introduced the-state-of-the-art hybrid applications to enhance the functional capability of Si nanowire FETs which are governed by the environmental stimuli like light irradiation and, are eventually able to emulate biological phenomena such as neuronal plasticity. The physical properties of the gate material (e.g., capacitance, conductance or nonlinear memristive characteristics) decide the transfer characteristics and time-dependent dynamics of the devices which can generate memory property.

Chapter 2 introduced the working principle of Si nanowire FETs with various structures which can be extended to the hybrid structure. Chapter 3 explained the experimental method including fabrication of the transistor device, synthesis of the hybrid films and electrical measurements.

Chapter 4 showed how photo-induced hot electron trapping by the interface and the dopants ions in the nanowire could modulate the threshold voltage of the Si nanowire FETs. Unlike well-known semiconductor optoelectronics, the conductivity of the nanowire FETs does not always increase. Especially in the subthreshold condition, the number of mobile carriers is small, so that the electron trapping strongly reduces the conductivity of the nanowire. Chapter 5 demonstrated the photo-induced electron generation and diffusion in the organic molecular gate layer that modulates the dynamics and efficiency of the light-induced current switching. The important message of this chapter is that an activated organic layer by external stimuli is able to act as a gate of the transistor with MOSFET structure when an electric potential is changed at the gate area.

In Chapter 6, the new gate stack material, the ion-doped sol-gel derived silicate matrix, was introduced. Although these material has used as a biosensor platform with a chemical and optical way of detection, this is the first time to analyze its electrical properties like capacitance or conductance to exploit those for the electric device applications. Chapter 7 demonstrated that the optical double gate effect from the sol-gel film gate devices which have FinFET structure. The double gate effect which appeared only under the optical stimulus expands the role of the hybrid gate from the supportive field effect (cf. extra voltage fluctuation of the DC (back) gate bias) shown in chapter 5 to the additional channel opening in the nanowire by light illumination.

Finally, Chapter 8 the ion-doped sol-gel film combining with the transistor emulated the memory and processing of a neuron cell. The redistribution of mobile ions in the film controlled by gate voltage allows the transistor to capacitor-less resistance switching memory device. Also, because of the comparably slow process of ionic movement (milliseconds range), the information storage was changed continuously depending on the timing properties of gate input signal (*e.g.*, frequency or pulse width of the on-voltage) apart from the signal amplitude (cf. set/reset voltage at conventional memory device). Therefore, the hybrid transistor could have the ability to mimic the neuroplasticity of a neuron cell which follows the sigmoid function of gate potential change.

Within this work, hybrid structured gates led to novel and diverse transistor functionalities which cannot be achieved by conventional FET devices. This work demonstrates that various physical elements like photons or ions could induce the electric charge on the gate that modulated the gate potential of the transistor. In other words, hybrid gate transistors obeying the original rule can replace existing conventional transistor applications like memory or logical operation. Hybrid devices showed the possibility to realize the next computing machine operated by new algorithms using physical phenomena (*e. g.*, ionic diffusion or coupling with photons, *etc*.) following mathematically nonlinear functions, which could help to solve very challenging computing problems requiring intelligence[1]. Also, the further study including mathematical modeling of the physical system in the hybrid layer will be required to build a stable system that can step forward into the future computing machine.

9.2 Outlook

Sensor applications using sol-gel derived matrix

The sol-gel-derived matrix can be used as efficient detecting platform thanks to its porous structure and the simple solution based procedure to synthesize, as discussed in **Chapter 6**. Also, Si nanowire FETs has been used as an effective ion-sensitive-biosensors in many previous studies. Therefore, the hybrid device using sol-gel derived gate material is expected to provide a new detecting platform that can include various types of biomolecules from RNA, protein to cell or even longer polymer chains.

However, the major challenge of the Si nanowire-based sensor is that this structure requires to form proper chemical linkages (usually covalent bonding) on the Si nanowire or oxide surface, which strictly decides the detection limit. Also, the analytes should be positioned in the electric double layer to be detected by nanowire, so that the detecting length is also limited.

The sol-gel based approach has the potential to solve the issues in Si nanowire ISFETs. The film can entrap many different types of detecting molecules without forming covalent bonding as well as buffer solutions. We can easily control the concentration of the detecting molecules at the solution preparation step which is not decided by the number of chemical links on the nanowires. Also, since the dielectric constant, which is changed by applied analytes or inner ionic or molecular mobility in the sol-gel derived matrix, can govern the conductivity change of the nanowires, the more volume of analytes can be applicable. Various detecting molecules in the sol-gel derived matrix could enable sensing of multiple molecules on a single nanowire device which is not yet performed from previous studies.

Neural network for neurocomputing

The most significant step using neurotransistor discussed in **Chapter 8** is to build a neural network system. Unlike von Neumann computing which is fundamentally based on the simple summation of the performance of each logic cell, the memory, and processing in the brain are performed in the more collective way. Although it has been reported that a single unit cell (*cf.* neuron) participates to memorize and to learn, the memory and learning are the final results of the plasticity of many neuron cells that forms new connections, intensifies (or suppresses) the existing connections or changes intrinsic

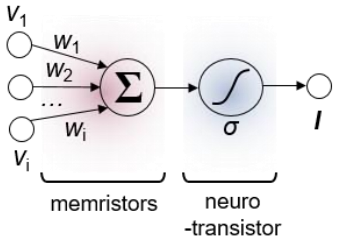


Figure 9.1 The schemetic diagram of perceptron: the simplest model of a neuron cell.

excitabilities. Therefore, human brain using complex cell networks outperforms the power efficiency and computing performance (*e.g.,* flops) of existing supercomputers. Recently, the memristor-based neural network is intensively studied, and its objective is to form a network of synapses that performs supervised or unsupervised learning [2–4]. However, apart from the hardware related issues arose from the memristor devices themselves[3], the architecture is still far from the real neuron models and even from the perceptron model, because of the lack of the stable sigmoid (logistic) *activation function* (σ in Figure 9.1*)*. Current memristive crossbar network generates an output signal which is a simple summation of weighted signals of memristor synapses.

The neurotransistor is an excellent solution that derives the activation function by mimicking the intrinsic plasticity (cf. the membrane potential change) which is represented by the sigmoid function. Up to now, the activation function is implemented by an additional circuit involving more than 20 transistors[2]. Therefore, the neurotransistor can dramatically reduce the number of transistors and their power consumption. To build a neural network involving the neurotransistors, the input gate area of neurotransistor needs to be connected to the multiple weighting elements (w_i in Figure 9.1, *e.g.*, resistive switching (memristive) layers) that mimic the biological synapses. The overall system is indicated by Eq. 9.1:

$$I = \sigma \sum_{j=1}^{i} (w_j \cdot v_j) \tag{9.1}$$

where v_j is input voltage of presynaptic neurons and I is output current.

The mentioned system would be a single neuronal building block that is connected with multiple presynaptic neuronal inputs. Further step should be the forming the multi-layer network. Although there are various neural network topologies of brain which is not clearly investigated[5], we can start to build the hardware using the simplest neural network model with two or theree hidden layers. The mentioned design will bring forward a full-functioning neurocomputing chip with complete CMOS process compatibility.

References

1. Di Ventra, M. & Traversa, F. L. Perspective: Memcomputing: Leveraging memory and physics to compute efficiently. *J. Appl. Phys.* **123,** 180901 (2018).

2. Li, C. *et al.* Efficient and self-adaptive in-situ learning in multilayer memristor neural networks. *Nat. Commun.* **9,** 2385 (2018).

3. Boybat, I. *et al.* Neuromorphic computing with multi-memristive synapses. *Nat. Commun.* **9,** 2514 (2018).

4. Prezioso, M. *et al.* Training and operation of an integrated neuromorphic network based on metal-oxide memristors. *Nature* **521,** 61–64 (2015).

5. Avena-Koenigsberger, A., Misic, B. & Sporns, O. Communication dynamics in complex brain networks. *Nat. Rev. Neurosci.* **19,** 17–33 (2017).

APPENDIX

A.1 Ohmic contacts between Si nanowire and electrodes

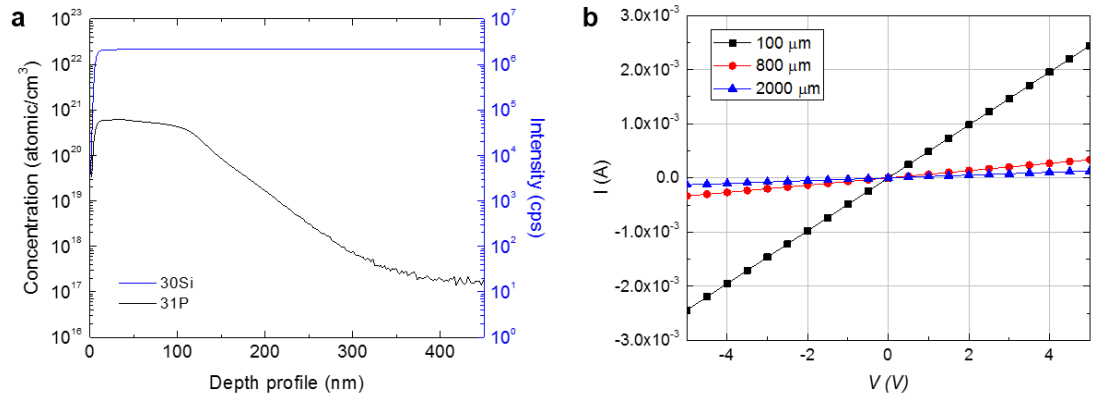


Figure A.1 The ohmic contact between metal electrode pad and the highly doped Si active area. (a) Doping concentration of phosphorus (P) in Silicon (Si) vs. depth profile by secondary ion mass spectrometry (SIMS). (b) *I- V* curves of heavily P-doped Si transmission lines with Ag/Ti metal electrode.

Phosphorus was implanted in Si wafer with a concentration of $8x10^{15}$ cm^{-2} with 50 keV for verifiyng the doping distribution (Figure A.1(a)). The black line shows that the concentration of phosphorus the ions is around $5x10^{20}$ cm^{-3} in 120 nm thick from the surface. The blue line shows that the intensity from Si is constant in measured area. This thickness of super-highly doped area fully covers the thickness of active area (see in Figure 3.2 (iii))

Based on this concentration ($5x10^{20}$ cm^{-3}), the thickness of depletion layer between Ti adhesion layer and the highly P-doped Si is calculated. The barrier height between Ti and Si is considered as 0.8 eV and the fermi level of the doped Si is positioned in the conduction band. Consequently, the barrier thickness (depletion width) is obtained as *1.4 nm*. With this thickness and the fermi energy condition, we believe that the tunneling is a dominant charge transport mechanism in this contact. Therefore, this contact is considered as a tunneling "ohmic" contact[1].

500 nm-thick Ag on 50 nm-thick Ti adhesion layer were deposited on source and drain area of the highly P-doped ($5x10^{20}$ cm^{-3}) Si transmission line with 70 μm-width and various lengths such as 100, 800 and 2000 μm (Figure A.1(b)). The current and the voltage is in a perfect linear relationship *i.e.*, ohmic behavior. Using the transmission line method (TLM) measurement, we extracted the contact resistivity as $9.15x10^{-5}$ Ω/cm^2. Even though this value is comparably higher than the theoretical value of ohmic contacts (< 10^{-6} Ω/cm^2), the contact between the tungsten probe and the Ag/Ti electrode can increase the contact resistivity and also the high barrier height between Ti and highly doped Si (0.8 eV) also can contribute to increase the value. This data is provided by T. Rim at POSTECH.

A.2 Substrate potential measurement

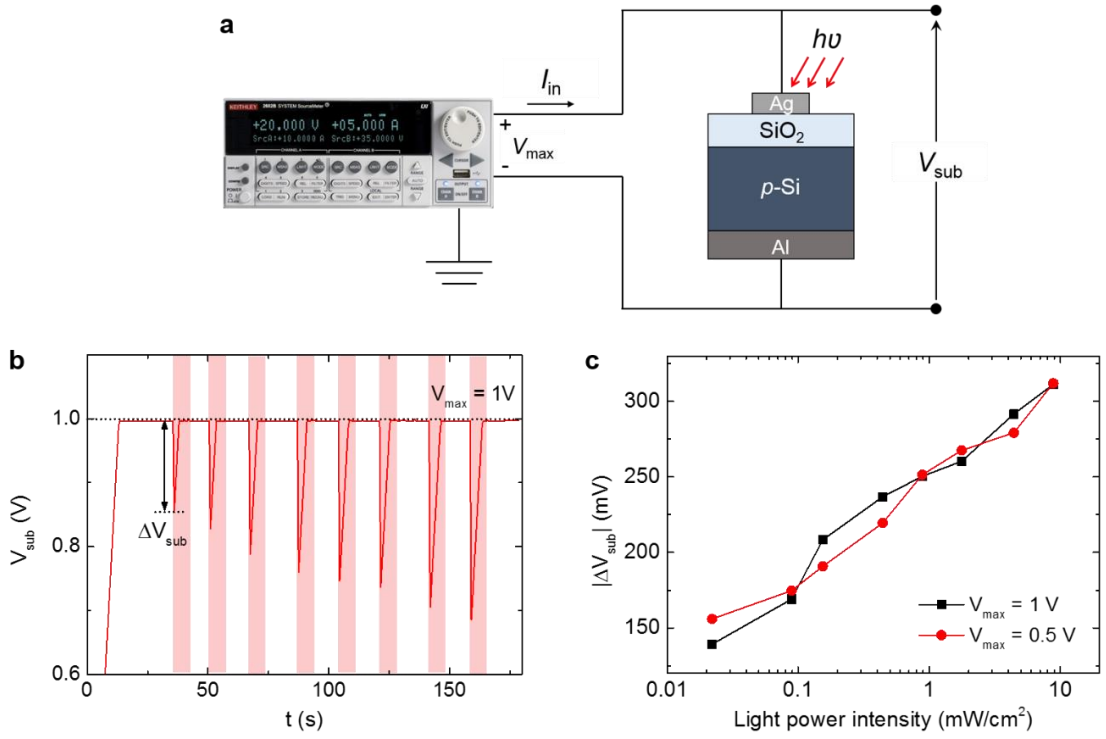


Figure A.2 Substrate potential change upon light illumination. (λ = 625 nm) (a) Schematic circuit diagram of the substrate potential measurement. The electric potential difference between the silver electrode on the SOI substrate and the aluminum chuck is measured. Applied current level (I_{in}) was 1 pA and V_{max} is voltage compliance limit which is varied. (b) Measured substrate potential on the time domain. The light is illuminated in the shaded area. Because of continuous

charging in the SOI capacitor, V_{sub} is maintained as V_{max} except the case in the illumination. (c) The substrate potential change depending on the light power intensity. The V_{max} value does not affect the V_{sub} change. The values of light intensities in (b) are gradually increasing by time that are exactly same as the data points of light intensities in (c).

A.3 Optical memory

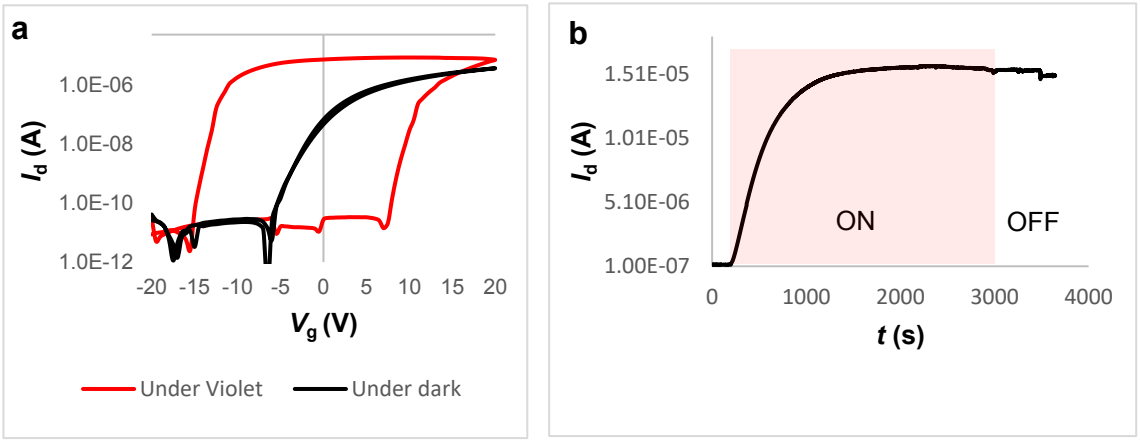
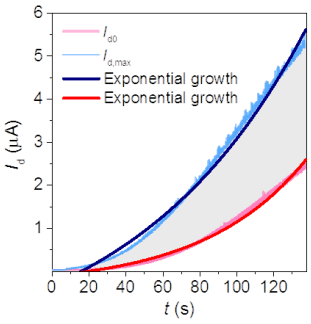
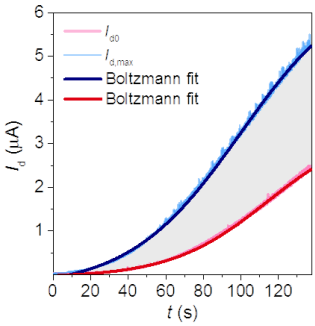
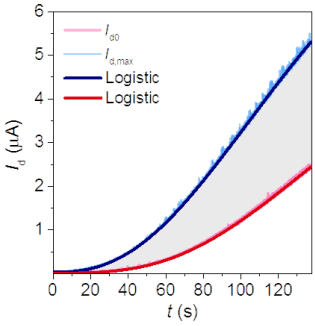
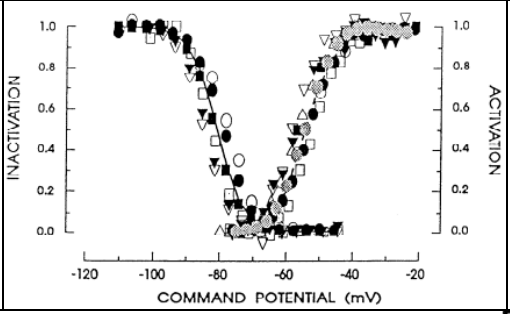


Figure A.3 (a) Transfer characteristics of Naphthalenediimide-based polymer coated Si nanowire FET under the light illumination (wavelength: 405 nm) with 10 mW of light intensity (red) and in the dark condition (black). (V_g = 5 V) (b) I_d vs time curve of the polymer coated device with (ON) and without (OFF) illumination. The shaded area indicates the condition of the light illumination. (V_d = 0.1 V for (a) and (b))

The organic *n*-type semiconductor polymer-coated devices (see **Chapter 3**) show huge hysteresis under light illumination. The time domain measurement in Figure A.4(b) shows that the light illumination causes strong current increase that agrees the transfer characteristics. The increased current reached the saturation current level keeps its level even after the light illumination is shut down. The Naphtalenediimide-based polymer has strong absorption peak in the range of violet light (λ = 390 nm)[2]. The photo-generation and dissociation of electron-hole pair in the amorphous semiconductor film produces the hysteresis in the transfer curve because of the limited recombination of the electron-hole pairs. The hysteresis implies that the device behaves like a memory device and the current saturation without illumination verify the memorization capability. The current is maintained around 800 seconds without light illumination.

Even though further investigation is required, the devices could be used as optical volatile or nonvolatile memory devices depending on the retention time.

A.4 Sigmoid fitting

Model	Fitted curves	Equation	R-squre
Exponential		y = a exp(x/x0)+b	**0.992**
Boltzmann		y = b+(a-b)/[1+exp((x-x0)/c)] a = initial value, b = final value, x0 = center, c = time constant	**0.998**
Logistic (Hill function)		y = b+(a-b)/[1+(x/x0)^p] a = initial value, b = final value, x0 = center, p = power (red: a=9.47E-9, b=6.55e-6, x0=163.4, p=3.045, blue: a=2.99E-8, b=1.14E-5, x0=145.9, p=2.48)	**0.999**
Neuronal ionic current (I/I_{max}) vs. membrane potential (V) (case of activation, right curve)		y = 1/[1+exp((x-x0)/c)]^p [ref.[3]]	

Exponential growth curve does not fit our curve well, which means the curve will not diverge. Sigmoid functions such as Boltzmann and Hill function are comparably well-fitted to the measured curve. Both equations can explain thermodynamic phenomena of ions. From the similarity with the experimental and fitted curve (based on Hodgkin-

Huxley's model) of neuronal membrane, we can expect that our curve is comparable to the sigmoid-like real model. This fitted result implies that the current growth of neurotransistors follows ionic dynamic of cell membrane.

References

1. Hu, C. *Modern semiconductor devices for integrated circuits*. (Prentice Hall, 2010).
2. Schubert, M. *et. al.* Influence of Aggregation on the Performance of All-Polymer Solar Cells Containing Low-Bandgap Naphthalenediimide Copolymers. *Adv. Energy. Mat.* 2, 369-380 (2012).
3. Huguenard, J. R. & McCormick, D. A. Simulation of the currents involved in rhythmic oscillations in thalamic relay neurons. *J. Neurophysiol.* 68, 1373–83 (1992).

LIST OF PUBLICATIONS

Publications

1. E. Baek, T. Rim, J. Schütt, L. Baraban and G. Cuniberti, "Negative photoconductivity of highly doped Si nanowire FETs," *Nano Letter* **17**(11), 6727–6734 (2017).
2. E. Baek, S. Pregl, M. Shaygan, L. Römhildt, W. M. Weber, T. Mikolajick, D. A. Ryndyk, L. Baraban and G. Cuniberti, "Optoelectronic switching of nanowire-based hybrid organic/oxide/semiconductor field-effect transistors," *Nano Research* **8**(4), 1229-1240 (2015).
3. D. Bodilovska, D. Nozaki and E. Baek, "Analysis of electric field and electrostatic potential distributions in porphyrin-coated silicon nanowire field-effect transistors," *Electronics and Nanotechnology (ELNANO), 2014 IEEE 34th International Conference* 119-122 (2014).
4. B. Jin, T. H. Thu, E. Baek, S. Sakong, J. Xiao, T. Mondal and M. J. Deen, "Walking-age Analyzer for healthcare application," *IEEE Journal of Biomedical and Health Informatics* **18**(3), 1034 (2014).
5. S. Kim, T. Rim, K. Kim, U. Lee, E. Baek, H. Lee, C.-K. Baek, M. Meyyappan, M. J. Deen and J.-S. Lee, "Silicon nanowire ion sensitive field effect transistor with integrated Ag/AgCl electrode: pH sensing and noise characteristics," *Analyst* **136**(23), 5012-5016 (2011).

Book chapter

1. L. Baraban, F. Zoergiebel, C. Pahlke, E. Baek, L. Roemhildt and G. Cuniberti, "Nanowire Field Effect Transistors: Principles and Applications," *Springer Science + Business Media New York* (2014).

Conference contributions

1. E. Baek, T. Rim, K. Kim, C.-K. Baek, L. Baraban and G. Cuniberti, "Tunable memory of Si nanowire FETs using ion modulation in sol-gel derived gate layer," *18th IEEE International Conference on Nanotechnology (IEEE NANO), Cork,* talk (2018).
2. E. Baek, T. Rim, C. V. Cannistraci, D. Makarov, L. Baraban and G. Cuniberti, "Neuromorphic memory and emulation of synaptic behavior by Si nanowire transistors," *14th European Conference on Molecular Electronics (ECME)*, *Dresden*, poster (2017).
3. E. Baek, T. Rim, M. Park, G. S. Cañón Bermúdez, D. Makarov, L. Baraban and G. Cuniberti, "Multiple Synaptic Modulation and Memory in Ionic Film-coated Si Nanowire Transistors," *Trends in Nanotechnology (TNT)*, *Dresden*, talk (2017).
4. E. Baek, T. Rim, L. Baraban and G. Cuniberti, "Negative photoconductivity of doped silicon nanowire FETs," *Trends in Nanotechnology (TNT)*, *Fribourg*, talk (2016).
5. E. Baek, T. Rim, L. Baraban, G. Cuniberti, "Optoelectronic gate modulation of hybrid Si nanowire FETs by metal ion-doped organic sol-gel film," *Europian Material Research Society (E-MRS) Spring meeting*, *Lille*, talk (2016).
6. E. Baek, S. Pregl, M. Shaygan, L. Römhildt, W. M. Weber, T. Mikolajick, D. A. Ryndyk, L. Baraban1 and G. Cuniberti, "Optoelectronic switching of nanowire-based hybrid

organic/oxide/semiconductor field-effect transistors," *582. WE-Heraeus-Seminar, III-V Nanowire Photonics*, *Bad Honnef*, poster (2015).

7. E. Baek, S. Pregl, M. Shaygan, L. Römhildt, D. Ryndyk, L. Baraban and G. Cuniberti, "Optoelectronic switching mechanism of porphyrin-coated Si nanowire field-effect transistors," *Europian Material Research Society (E-MRS) Spring meeting*, *Lille*, talk (2014).
8. E. Baek, S. Pregl, M. Shaygan, L. Römhildt, D. Ryndyk, L. Baraban and G. Cuniberti, "Light-induced switching mechanism of porphyrin-coated Si nanowire field-effect transistors," *Deutsche Physicalische Gesellschaft (DPG) Spring Meeting*, *Dresden*, talk (2014).
9. E. Baek, S. Pregl, L. Römhildt, D. Ryndyk, L. Baraban and G. Cuniberti, "Light-induced electrical switching of porphyrin-covered silicon nanowire FETs" *Trends in Nanotechnology (TNT)*, *Seville*, poster (2013).

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