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RESEARCH PAPER

20–25 Gbit/s low-power inductor-less single-chip optical receiver and transmitter frontend in 28 nm digital CMOS

LÁSZLÓ SZILÁGYI, GUIDO BELFIORE, RONNY HENKER AND FRANK ELLINGER

The design of an analog frontend including a receiver amplifier (RX) and laser diode driver (LDD) for optical communication system is described. The RX consists of a transimpedance amplifier, a limiting amplifier, and an output buffer (BUF). An offset compensation and common-mode control circuit is designed using switched-capacitor technique to save chip area, provides continuous reduction of the offset in the RX. Active-peaking methods are used to enhance the bandwidth and gain. The very low gate-oxide breakdown voltage of transistors in deep sub-micron technologies is overcome in the LDD by implementing a topology which has the amplifier placed in a floating well. It comprises a level shifter, a pre-amplifier, and the driver stage. The single-chip frontend, fabricated in a 28 nm bulk-digital complementary metal-oxide-semiconductor (CMOS) process has a total active area of 0.003 mm², is among the smallest optical frontends. Without the BUF, which consumes 8 mW from a separate supply, the RX power consumption is 21 mW, while the LDD consumes 32 mW. Small-signal gain and bandwidth are measured. A photo diode and laser diode are bonded to the chip on a test-printed circuit board. Electro-optical measurements show an error-free detection with a bit error rate of 10^{−12} at 20 Gbit/s of the RX at and a 25 Gbit/s transmission of the LDD.

Keywords: RF front-ends, Active circuits, Broadband amplifiers

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I. INTRODUCTION

Global video traffic over the Internet is forecast to reach 80% of the global IP traffic by 2019 from 67% in 2014. The increasing popularity of video-on-demand (VoD) in ultra-high definition necessitating about 18 Mbit/s bit rate, thus nine times more than standard definition video streaming, forecast to reach 21% of the global VoD traffic by 2019 results in an ever-increasing load on data centers to fast delivery of services and data [1]. Furthermore, according to [2], more than 75% of the total data traffic are within the data center. This traffic is enabled by high-performance servers interconnected by multiple switching networks [3]. The data rate (DR) of this short-to-medium interconnect is in the range of 25 Gbit/s in year 2014 [4].

Using electrical interconnects at these DRs necessitates compensation of the high insertion losses as well as the reflections done at the cost of a high-power consumption and an increased circuit complexity with a high-order decision-feedback equalizer [5]. Fiber-optic interconnects offer a power efficient alternative due to their lack of reflections, weight, high channel bandwidth (BW), and low attenuation, which makes them suitable to transmissions up to hundreds of meters [4, 6].

A further trend is to integrate the complete unit into one silicon substrate. The advancement of complementary metal-oxide-semiconductor (CMOS) technologies makes it possible to have the digital data-processing core in the same system-on-chip (SoC) with the analog interface and supply circuits, reducing the overall costs and performance degradation [7]. In case of high-speed analog frontends, the BW is a key requirement. Its enhancement necessitates often inductive peaking with inductors occupying a significant area [3–10]. As the cost of manufacturing deep sub-micron CMOS technologies is extremely high, the area is nowadays among the most important considerations when evaluating an analog circuit from the mass-production cost perspective. To optimize the area, only active-peaking methods were employed in the presented design. Another important challenge in the design of electro-optical frontends in sub-micron CMOS is the high DC bias and operation voltage of electro-optical components. Modulators and vertical cavity surface-emitting laser (VCSEL) diodes need to be operated at voltages, which are multiples of the breakdown voltage of CMOS technologies. Special architectures are used, such as in [11], to provide the necessary DC bias to the VCSEL but not exceed the breakdown voltage of individual transistors.

The architecture of the electro-optical frontend consisting of a receiver (RX) and a laser diode driver (LDD) is presented in Section II. Section III discusses the design challenges, dimensioning of the devices, and simulation result of each block of the RX frontend. As active peaking was used extensively to increase the BW and gain of the circuits, the

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mechanism of this method is analyzed. In Section IV, the design and simulation result of the LDD is described. The circuit was fabricated in a 28 nm super low-power (SLP) digital CMOS process. Electrical measurements evaluate the small-signal performance of both the RX and the LDD in Section V. Electro-optical measurements are performed on the chip on a printed circuit board (PCB), bonded to a commercial photo diode (PD) and a VCSEL. Optical signal-integrity measurements show an error-free operation with a bit error rate (BER) of 10^{-12} up to a DR of 20 Gbit/s of the RX and 25 Gbit/s of the LDD. Finally, the results of both the RX and the LDD are compared with existing designs in the “Conclusion” section.

II. ARCHITECTURE OF THE ELECTRO-OPTICAL FRONTEND

The electro-optical frontend consists of two main parts, the RX and LDD as depicted in Fig. 1. In addition, there are bias, logic, and electrostatic discharge protection circuits. A PD with 190 fF is bonded at the input of the RX with additional 30 fF of pad capacitance. A transimpedance amplifier (TIA) converts the current generated by the PD into a voltage. In order to have a signal amplitude in the hundreds of mV range, the signal is further amplified by the limiting amplifier (LA) consisting of three cascaded differential stages. Since the TIA is single-ended and the LA differential, a dummy TIA provides the common-mode (CM) signal at the other input of the LA. For measurement purposes, the output of the LA should be matched to $50\ \Omega$ and a single-ended voltage swing of at least 200 mV should be provided on a $50\ \Omega$ load. For this reason, a buffer (BUF) is used, supplied from a separate power supply, V_{DDB} .

There are two challenges when considering the design of a RX for optical communications. First, the DC current caused by the average optical light, which can change depending on the data pattern as well as the transmission medium. This

current, present at the input of the TIA, can cause the DC-operating points of the TIA and LA to shift. This influence can go as far as entirely hinder the functionality of the RX. The second consideration is the effect of process variation and mismatch on the amplifier. Offset can cause the same issues as the DC current. When this offset is amplified, the differential output becomes unbalanced, thus clipping the signal. The amount of unbalance can be so high that the outputs stick to the upper and lower limits, thus no signal can be seen. To overcome these two issues, the offset compensation (OC) and common-mode control block was added to the RX. The input of the TIA is adjusted if offset is measured at the output of the RX.

The common-cathode (CC) LDD, as depicted in the lower half of Fig. 1, consists of a level shifter, a pre-amplifier, and the driver stage. In order to be able to provide the DC bias voltage to the anode of the VCSEL, the LDD is supplied from a high-voltage (HV) supply V_{DDH} . The pre-amplifier and the output stages have V_{DDH} as positive supply; however, the negative supply is not the global VSS but a floating V_{SSH} which is 1.2 V lower than V_{DDH} . The signal is transferred to the HV domain by the level shifter. This block provides an isolation between the two voltage domains. At the output, a current source is used to tune the DC current through the VCSEL.

The presented electro-optical frontend is implemented in a 28 nm SLP digital CMOS process. As this is a technology optimized for digital circuits, the performance of high-speed analog circuits is lower than those realized in silicon on insulator (SOI) CMOS [12] or BiCMOS [13] technologies. Furthermore, the devices in SLP are intended for low-power digital design, thus more challenging for analog high-speed design than, for example, high-performance bulk CMOS processes that have dedicated devices for analog circuits. It is however more convenient to implement high-density digital circuits such as processors and digital signal processing blocks in bulk SLP CMOS. The presented frontend can be then integrated on a single SoC with the high-density digital blocks.

Fig. 1. Block diagram of the single-chip electro-optical frontend.

III. DESIGN OF THE OPTICAL RECEIVER

A) Transimpedance amplifier

The schematic of the TIA is shown in Fig. 2. As the supply voltage is low, so the voltage headroom for stacking devices is modest, a shunt-feedback topology was preferred instead of a common-gate TIA. The transimpedance gain is set by R_{FB} . This topology has the trade-off between the input impedance, defining the BW which is inversely proportional – and the gain that is proportional to R_{FB} . Thus, a compromise must be made when selecting the R_{FB} , so that the BW of the TIA is in accordance with the maximum BW of the following blocks. With this regard, R_{FB} is chosen to 240 Ω , and with a total input capacitance of the PD and a pad of 220 fF, a BW of 12 GHz can be reached in simulation.

Transistors M_2 and M_3 form a CMOS inverter-type amplifier stage as in [3, 6, 8, 14, 15] when both transistors are in saturation. The gain of this stage can be written as

$$A_{v,M_2+M_3} = -(g_{m,M_2} + g_{m,M_3}) \times (r_{DS,M_2} \parallel r_{DS,M_3}). \quad (1)$$

It can be seen in equation (1) that in order to increase the open-loop gain of the TIA, which would decrease its input resistance as a result of increase of BW, the transconductances g_{m,M_2} and g_{m,M_3} need to be as high as possible. By increasing the area of M_2 and M_3 , the g_m would indeed increase; however, the input capacitance would also be higher, thus reducing the BW. Instead, a common-drain (CD) stage M_1 is added to shift the input voltage to a lower value, thus increase the V_{GS,M_2} . Another beneficial effect of adding M_1 is the decreasing of the capacitance at the input of the TIA by splitting the Miller capacitances created by the gate-drain capacitances of M_2 and M_3 , so only half is seen at the input node. Meanwhile, a pole and zero are created at high frequencies at the source of M_1 . The open-loop gain of the TIA calculated with equation (1) matches the simulated gain of -4.6 . The power consumption of the TIA is 4.5 mW.

B) Limiting amplifier

To have a signal swing of 400 mV_{pp}, the output voltage at the TIA needs to be further amplified. Since the signal format is non-return to zero, only the low and high levels are important, thus a LA is suitable. Given the low supply voltage and intrinsic gain of the devices, both gain and BW-enhancing techniques must be implemented. Using them, the required gain

Fig. 2. Schematic diagram of the TIA.

Fig. 3. Schematic diagram of a LA stage.

of around 20 dB can be reached with three cascaded stages. The schematic of one LA stage is depicted in Fig. 3. Transistors M_{4a} and M_{4b} together with R_{1a} and R_{1b} form a differential amplification stage. The gain is enhanced by M_{5a} and M_{5b} , while the BW is boosted using M_{6a} , M_{6b} , and C_{pk1} . The most straightforward way to increase the gain would be to use a higher resistor for $R_{1a,b}$ which would however result in the decrease of BW and output CM affecting the next stage. For this reason, the gain boosting technique from [16] is used. The gain will change from $-g_{m,M_{4a,b}}R_{1a,b}$ by adding the positive feedback stage with M_{5a} and M_{5b} to

$$A_{v,LA} = -\frac{g_{m,M_{4a,b}}R_{1a,b}}{1 - (g_{m,M_{5a,b}}R_{1a,b}/2)}. \quad (2)$$

The gain is enhanced by increasing the load resistances of the differential stage. The highest gain can be reached when $2/g_{m,M_{5a,b}}$ is close to $R_{1a,b}$. However, $g_{m,M_{5a,b}}$ should not reach the maximum value since this would cause transistors M_{5a} and M_{5b} to latch. Equation (2) yields a gain of -2.55 , confirmed by simulation. With the presented technique, the gain is increased by 35%, from -1.6 .

To boost the BW, the stage consisting of transistors M_{6a} , M_{6b} , and capacitor C_{pk1} is added. This block boosts the gain in a similar way to $M_{5a,b}$ but it becomes active only with capacitor C_{pk1} . In other words, this stage introduces a zero to

$$\omega_z = \frac{g_{m,M_{6a,b}}}{C_{gs,M_{6a,b}} + 2C_{pk1}}. \quad (3)$$

In the stage from Fig. 3, the zero will be at approximately 11 GHz. When the total capacitance at the output node C_L is larger than C_{pk1} , ω_z will create a peak in the transfer function, which will be lower than the dominant pole. Nevertheless, it is important that the zero ω_z comes always before the dominant pole in order to maintain the LA stable. In order to ensure this

$$g_{m,M_{6a,b}} < \frac{C_{gs,M_{6a,b}} + 2C_{pk1}}{((R_{1a,b})/(1 - (g_{m,M_{5a,b}}R_{1a,b}/2)))(C_{pk1} - C_L)} \quad (4)$$

must be satisfied [16]. In the most conservative case, $g_{m,M_{6a,b}}$ must be according to equation (4) < 4 mS, thus $I_{bBW1,2}$ is set to 0.3 mA.

Simulations on the LA consisting of three cascaded stages from Fig. 2 were performed. The LA consumes 13.2 mW power while having 25 dB gain and 16.4 GHz of BW.

C) Output buffer

Since the electro-optical frontend is a stand-alone chip, it needs an interface that is able to drive the $50\ \Omega$ transmission lines and measurement equipment. The LA can not provide enough current to reach a reasonable voltage swing on the $50\ \Omega$ for which reason an output BUF must be used. In SoCs, the RX is connected to the clock-data recovery block and a BUF is not required, so the energy needed by the BUF is not included in the overall power balance. As it can be seen in Fig. 4, a separate power supply is used for the output BUF, V_{DDB} . A broadband matching is achieved to $50\ \Omega$ by the output stage consisting of common-source (CS) stage $M_{9a,b}$ and CD stage $M_{8a,b}$ in push-pull configuration [17]. The output resistance is approximately equal to

$$R_{out,RX} = \frac{1}{g_{m,M8a,b}}, \quad (5)$$

resulting in an $R_{out,RX}$ of $30\ \Omega$. In order to decrease the capacitive load on the output of the LA a pre-amplifier is added. Two differential stages with different output CMs provide the signal to the CS and CD stages. The gate voltage at $M_{8a,b}$ is higher than that at $M_{9a,b}$, so the CM of the V_{outRX} is approximately $V_{DDB}/2$.

The BUF consumes 13 mW power from the supply V_{DDB} in simulation. On a $50\ \Omega$, the differential gain is $-4\ \text{dB}$ with approximately 60 GHz BW. The reflection coefficient is less than $-20\ \text{dB}$ up to the frequency of interest of 20 GHz.

D) Offset compensation and common-mode control

As already mentioned in Section II, the PD creates a DC current, which needs to be sunken. This current might drift in time and depends on several factors such as the bit pattern, transmission medium as well as temperature. When no circuit is available to sink this current, the operating

Fig. 4. Schematic of the output BUF.

point of the TIA will change, resulting in an offset voltage at the output. Furthermore, process variation and mismatch cause offset of the CM, especially in the LA. When amplified, the offset can drive the output out of saturation and even clip it, thus interfering with the functionality of the RX. The OC block from Fig. 5 solves this problem. As in [4], [6], or [10] a feedback loop is used to measure the offset of the CM at the output and adjust the input in order to minimize the error. All these feedback mechanisms use an RC filter. However, as it is shown in [18], a switched-capacitor (SC) filter needs a much smaller area.

The OC loop works as follows: the output, differential CM is measured by R_{4a} and R_{4b} as $v_{outCM} = (v_{outRX+} + v_{outRX-})/2$. The high-frequency phase shift is filtered by R_z and C_z [19]. v_{outCM} is then compared with the CM of v_{outRX-} obtained by low-pass filtering (LPF) the output signal. The error is minimized by pushing or pulling current from/to the input of the TIA with transistors M_{10} and M_{11} .

A LPF in the SC technique is used to extract the CM of v_{outRX-} as in [18]. The residual offset can be approximated by $V_{os,res} = V_{os}/(1 + A_{v,RX} + A_{v,OPA})$, which means that $A_{v,OPA}$ should be maximized. However, the lower cut-off frequency of the RX $f_{l,RX} = A_{v,OPA} \times f_{l,LPF}$, thus a compromise between $V_{os,res}$ and $f_{l,RX}$ needs to be made. For a pseudo-random bit sequence (PRBS) of $2^{31} - 1$, $f_{l,RX}$ should be lower than 200 kHz. The $f_{-3\ \text{dB}}$ of the SC filter from Fig. 5 can be expressed as

$$f_{l,LPF} = f_{clk} \frac{C_{s1}}{C_{s2}}. \quad (6)$$

This SC filter needs an anti-aliasing filter (AAF) with $f_{AAF} < f_{clk}/2$, where f_{clk} is the clock frequency. It can be seen that the larger the f_{clk} the smaller the area occupied by the AAF. Nevertheless, according to equation (6), a high f_{clk} implies also a large area occupied by the SC filter capacitor C_{s2} . As a good compromise, f_{clk} was set to be at least 5 MHz and can be slightly increased if the signal pattern allows it. The resulting f_{AAF} should be at least 2.5 MHz, although 1.2 MHz was rather implemented for a lower clock feedthrough. Given the fact that 35 fF is the smallest capacitor available in the technology, the ratio C_{s1}/C_{s2} was set to 125.

Simulations with the complete RX show the lower cut-off frequency is 40.5 kHz for a 5 MHz clock and 76 kHz for 10 MHz f_{clk} . A very small ripple can be seen on the output due to the clock feedthrough in the OC filter. The lower f_{clk} the higher the ripple, still, it is always in the μV domain.

Fig. 5. Schematic diagram of the OC block.

Fig. 6. (a) Schematic diagram of the level shifter. (b) Functionality of the level shifter.

IV. DESIGN OF THE LASER DIODE DRIVER

Commercial VCSEL diodes need typically 1.8–2.5 V DC bias voltage and are often developed by vendors in CC configuration [11, 20, 21]. When a 3.3 V supply voltage as in [20] or [21] is not possible, different techniques have to be applied to supply the signal at the anode of the VCSEL, meanwhile having it biased at a sufficient DC voltage. Transistors can be stacked to reach multiples of breakdown voltages. This is a technique common for drivers in CMOS such as [22], [23], or [24]. However, this technique is sensitive to start-up sequences and might breakdown on transient peaks. The LDD placed in a triple-well topology is implemented and further developed [11, 25].

It has to be mentioned that CC VCSEL drivers will inherently consume more power than common-anode (CA) drivers. This comes from the need of CA drivers to be supplied at much higher voltages, above the DC threshold of the VCSELs, which have their cathode connected to ground and driven on the anode terminal. On the other hand, CA drivers do not need a high-supply voltage as they drive the VCSEL at the cathode while the anode is the only terminal of the circuit, which requires a HV supply.

A) Level shifter

Since the pre-amplifier and output stages are in a floating well, the current-mode logic (CML) signal coming from a GND and VDD referenced generator needs to be transferred to the HV domain. This operation is done by the level shifter depicted in Fig. 6(a). The differential pair M_{12a} and M_{12b} transforms the input signal v_{inLDD} in a current, which is transformed back into a voltage by resistors R_{5a} and R_{5b} . As it can be seen in Fig. 6(b), the output signal v_{outLVL} is a CML signal between $VDDH$ and $VSSH$. HV transistors with thick oxide $M_{H1a,b}$ have a breakdown voltage of approximately 2.5 V and their role is to protect the drain potential of $M_{12a,b}$ from exceeding 1.2 V. I_{bLVL} and $R_{5a,b}$ are dimensioned in such way that the v_{outLVL} CM never goes under the potential of $VSSH$, thus the circuits in the well are protected from overvoltage.

A similar peaking method as in the LA, a positive feedback at the frequency set by C_{pk2} , is used to extend the BW of the

level shifter. Simulations show 33.5 GHz of BW while consuming 6.2 mW of power from the 2.7 V V_{DDH} supply.

B) Pre-amplifier and output stage

Transistors in the circuits from Fig. 7 are low-voltage, thin oxide devices, but since they are placed in a floating well, $VDDH$ can be as high as 2.7–2.9 V, thus having an output DC voltage of more than 2 V. The local ground, which is the potential of the well, is $VSSH = VDDH - 1.2$ V, thus at 1.5 V. The pre-amplifier in Fig. 7(a) further amplifies the signal, driving it above a certain level in limitation. Peaking is realized by positive feedback with transistor $M_{15a,b}$ at the frequency given by C_{pk3} .

A totem-pole structure is used for the output stage as it can be seen in Fig. 7(b), in order to achieve an increased efficiency as in [11, 17, 25]. Since many of the commercial VCSELs have $50\ \Omega$ impedance, the driver stage should have an output impedance of $50\ \Omega$ for an efficient power transfer. As $Z_{out, LDD} \approx 1/g_{m, M18}$, the size of M_{18} is three times of M_{19} . Furthermore, the DC bias of the gate is set much higher than that of M_{19} , to obtain a higher $g_{m, M19}$. In order to compensate for the smaller gain on the high side of the totem pole, so the CD stage M_{18} , a gain boosting is realized with the positive-feedback cell of $M_{17a,b}$ as already explained in Section III.

Small-signal simulations, considering a VCSEL diode with 300 fF capacitance and 50 Ω resistance, show that the LDD has a BW of 17 GHz and a gain of 6 dB, while 16 mW of power is consumed from the 2.7 V V_{DDH} . Transient simulations show that the LDD modulates 6 mA_{pp} current through the 50 Ω VCSEL diode. The bottle neck of the LDD is the output stage where on one hand large transistors are needed in order to provide enough current swing through the VCSEL, while on the other hand they have a large capacitance which slows down the driver.

V. MEASUREMENT RESULTS

The fabricated die can be seen in Fig. 8(a). It has $0.64 \times 0.9 \text{ mm}^2$, size defined by the DC and signal pads. The active area of the RX is $52 \times 36 \text{ }\mu\text{m}^2$, while the LDD occupies $36 \times 27 \text{ }\mu\text{m}^2$ totalizing 0.00284 mm^2 active area.

Fig. 7. Schematic diagram of (a) the pre-amplifier and (b) the LDD output stage.

Small-signal electrical measurements were realized with the chip placed on the wafer prober and by contacting both DC and signal pads with probes. For the electro-optical measurements, the die was bonded together with the optical components on a PCB. The circuits are supplied with 1.2 V for VDD and $VDDb$, while $VDDH$ is 2.7 V and $VSSH$ is 1.5 V. The power consumption of the complete electro-optical front-end is 20 mW from VDD , 8 mW from $VDDb$, and 32 mW without- and 45 mW with the VCSEL diode from $VDDH$. A 20 MHz external clock with CMOS levels is supplied for the SC circuit via one of the pads.

A) Small-signal measurements

For the small-signal characterization, a 67 GHz vector network analyzer was used with 40 GHz differential GSGSG probes. Calibration and measurements were done using the SOLT algorithm. The Z-parameters were extracted from the measured S-parameters.

As it can be seen in Fig. 9(a), the differential transimpedance gain of the RX is 69 $\text{dz } \Omega$ over a BW of 6.2 GHz. The input impedance is around 100 Ω . A good agreement can be seen between the simulated and measured gain. However, the measured input impedance deteriorates from the simulated values since the open-loop gain of the TIA heavily depends on process variation. A higher input impedance results in the

drop of BW. Further, parasitic capacitances, not included in the simulations, contribute to the decrease in BW.

Figure 9(b) shows the transfer characteristic of the LDD. A gain of 6 dB is achieved and due to a large amount of peaking, the BW is as high as 13 GHz. The high capacitance of the VCSEL is not included in these measurement and simulation results. The output impedance is maintained under 50 Ω , averaging 35 Ω , so an enhanced power transfer from the LDD to the VCSEL is possible.

Further measurements show that the OC network fulfills its purpose as the maximum output offset voltage was around 20 mV. DC voltage measurements show that the LDD has a voltage drop between $VDDH$ and the output of around 0.45 V, thus for a VCSEL with a minimum bias of 1.8 V, a minimum $VDDH$ of around 2.3 V would already suffice, proving the viability of the presented LDD topology.

B) Electro-optical measurements

The electro-optical front-end chip was bonded to a PCB as it can be seen in Fig. 8(a). To the input of the RX, a 25 Gbit/s PD for 850 nm light was bonded with a responsivity of 0.6 A/W and a capacitance of 140 fF. One of the DC pads can provide the anode DC voltage of 3 V. On the LDD side, a 25 Gbit/s VCSEL diode for 850 nm wavelength and 0.6 W/A slope efficiency is bonded to the chip. The bias current

Fig. 8. (a) Chip micrograph and (b) the electro-optical measurement setup.

Fig. 9. Small-signal measurements of the (a) RX and (b) LDD.

provided by the driver is higher than the minimum of 0.5 mA and a DC voltage higher than 1.8 V required by the VCSEL.

Figure 8(b) shows the electro-optical measurement setup. To measure the RX, a VCSEL module, biased at 10 mA, was modulated by a $2^7 - 1$ PRBS with an amplitude of approximately 12 mA_{pp}. Then 1 m of optical multimode fiber (MMF) was connected to the optical attenuator, which was then connected through additional 1 m of MMF to the optical probe that provided the signal to the PD. To measure the LDD, the optical probe collects the light emitted by the VCSEL and provides it to the PD module through the same 1 m MMF optical attenuator. The electrical

signal of the PD module is fed to the bit error-rate tester and sampling oscilloscope.

As the eye diagram in Fig. 10(b) shows, the RX works error free with a BER of 10^{-12} up to a DR of 20 Gbit/s. This is demonstrated also by the bathtub tests from Fig. 11(a). The single-ended output swing of the RX is approximately 175 mV_{pp}, which is enough to drive the next block in the optical RX chain. A higher DR of 25 Gbit/s can be reached by the LDD as the eye diagram in Fig. 10(d) shows and the bathtub tests in Fig. 11(a) confirm. For this measurement, the LDD was supplied with a PRBS $2^{31} - 1$ signal with 1.3 V_{pp} differential amplitude.

Fig. 10. Electro-optical measurements (a, b) of the RX and (c, d) of the LDD.

Fig. 11. Signal-integrity measurements of the electro-optical frontend. (a) Measured optical bathtub tests of the electro-optical frontend. (b) Optical sensitivity measurement of the RX.

Optical sensitivity measurements of the RX are shown in Fig. 11(b). At 20 Gbit/s, the maximum sensitivity with an error-free detection with a BER of 10^{-12} is -2.5 dBm. The optical modulation amplitude is estimated by measuring the average current through the PD at the DC bias pad and knowing the responsivity of the PD and modulation parameters of the VCSEL module as in [26]. At this input optical power, the transmission was error free.

Electro-optical eye diagrams of the LDD can be seen in Figs 10(c) and 10(d). The eye diagram in Fig. 10(d) and the bathtub tests in Fig. 11(a) show that the LDD is capable of driving the VCSEL up to a DR of 25 Gbit/s. Further electrical measurement shows that the driver provides a 250 mV_{pp} voltage swing on the $50\ \Omega$ load resulting a 5 mA_{pp} current swing through the VCSEL.

VI. CONCLUSION

An inductor-less electro-optical frontend consisting of a RX and VCSEL driver was designed in a 28 nm SLP digital CMOS process. The frontend consists of a RX with TIA, LA, output BUF, and an OC circuit in the SC technique as well as CC VCSEL diode driver, which is able to provide the

high DC bias voltage. The driver has a level shifter in addition to a pre-amplifier and output stage in a floating well. Active-peaking methods are used in both of the circuits that enhance the BW and gain, thus using much less area than inductive peaking.

Small-signal S-parameter measurements show that the RX has a differential transimpedance gain of $69\text{ dB}\ \Omega$ over a BW of 6.2 GHz while consuming 20 mW. An additional output BUF drives the $50\ \Omega$ instruments consuming additional 8 mW power. The LDD needs 32 mW while achieves 13 GHz BW. Commercial PD and VCSEL are bonded on a PCB to the chip. This way electro-optical measurements are performed that show the RX can work error free with a BER of 10^{-12} up to 20 Gbit/s with an input optical sensitivity of -2.6 dBm. The LDD can work on the other hand error free up to a DR of 25 Gbit/s.

As it can be seen in Table 1, the RX is among the designs with the smallest active area and one of the most energy-efficient optical RXs. Although the BW and DR are not comparable with what can be achieved in SiGe technologies such as the designs in [28, 30], CMOS has the advantage of highly dense digital circuits, thus this RX can be fully integrated together with the digital core. The RX in [26] is designed in the same technology node, occupies the same area as the proposed

Table 1. Comparison of the RX with state of the art

Ref. Year	Tech. (nm)	DR (Gbit/s)	Power (mW)	Energy/bit (pJ/bit)	Area (mm ²)
[27] 2015	250 SiGe	40 (O)	275	6.88	> 1
[28] 2016	130 SiGe	88 (E)	29.9	0.34	0.015
[29] 2015	130 SiGe	40 (O)	158	3.95	0.99
[30] 2015	130 SiGe	71 (O)	860	12	n/a
[6] 2015	65 CMOS	30 (O)	41	1.37	0.26
[9] 2015	65 CMOS	25 (O)	49	1.96	0.26
[8] 2014	65 CMOS	25 (O)	93	3.72	0.06
[4] 2014	65 CMOS	28 (O)	91	3.25	0.32
[31] 2013	32 SOI CMOS	35 (O)	42	1.2	0.01
[12] 2015	32 SOI CMOS	25 (O)	84	3.36	n/a
[3] 2016	28 CMOS	25 (O)	58	2.32	0.25
[10] 2014	28 CMOS	28 (E)	28.8	1	0.246
		10 (O)		2.9	
[26] 2014	28 CMOS	25 (O)	4.5	0.18	0.0018
This work	28 CMOS	20 (O)	21	1	0.0018

(O) Optical and (E) electrical measurement.

Table 2. Comparison of the LDD with state of the art

Ref. Year	Tech. (nm)	Type CA/CC	DR (Gbit/s)	Power (mW)	FOM (mW/Gbps)	Area (mm ²)
[20] 2012	250 SiGe	CC	40 (O)	130	3.25	0.06
[21] 2014	130 SiGe	CC	40 (O)	312	7.8	0.5
[30] 2015	130 SiGe	CA	71 (O)	950	13.4	n/a
[32] 2015	130 SiGe	CA	40 (O)	376	9.4	n/a
[25] 2015	90 CMOS	CC	25 (O)	60	2.4	0.006
[11] 2015	80 CMOS	CC	17 (O)	60	3.5	0.003
[22] 2014	65 CMOS	CC	25 (O)	257.5	10.3	0.32
[33] 2015	65 CMOS	CC	15 (O)	60	4	0.003
[34] 2015	65 CMOS	CC	30 (E)	155	5.2	n/a
[24] 2014	65 CMOS	CC	35 (E)	157	4.49	0.09
[35] 2015	65 CMOS	CC	26 (O)	46.8	1.8	0.024
[31] 2013	32 SOI CMOS	CA	35 (O)	46.7	1.33	0.002
This work	28 CMOS	CC	25 (O)	45	1.8	0.001

(O) Optical and (E) electrical measurement.

one, but consumes less power, and it can achieve a slightly higher DR. However, a sampled system is used in the mentioned implementation, which requires four phases of precise clock. The generation of the sampling signal will occupy significant area and consume additional power resulting in comparable numbers with this design.

Table 2 compares the LDD from the electro-optical frontend to other recent designs. The proposed driver has the smallest area and one of the best figures of merit (FOM). The high FOM of [31] can be attributed to the fact that it is a CA driver and thus necessitates a much lower supply voltage as the anode of the VCSEL can be separately connected to a high DC supply and driven on the cathode. It is worth mentioning that the optical measurements, in contrast with only electrical, consider also the significant power consumed by the VCSEL diode. The power consumption of the proposed driver alone is 32 mW to which 13 mW drawn by the VCSEL adds.

With 0.003 mm² of total active area, the electro-optical frontend is among the smallest and with a total link energy efficiency of 2.8 pJ/bit among the most energy-efficient fully integrated electro-optical frontends to date.

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