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Assembly of optical transceivers for board-level optical interconnects

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ABSTRACT

This paper demonstrates an approach for passive alignment and assembly of link components for board-level very-short range optical interconnects. This interchip optical link is based on planar polymeric multimode waveguides and glass-based electro-optical transceivers. The main aim of the work is the investigation of assembly processes of link components in order to fulfill the tolerance requirements using passive alignment. The optical characterization in regard to the optical coupling between link components will define the tolerances for the alignment process. This optical analysis is based on measurements of spatial coupling characteristics. The influence of assembly tolerances on the coupling efficiency is investigated. Flip-chip assembly of electro-optical devices on the glass interposer and of the glass interposer on optical overlay is presented to prove the implementation of the concept.

Keywords: optical packaging, board-level optical interconnects, passive alignment, polymeric optical waveguides, glass interposer, out-of-plane coupling optics, optical characterization, parallel optical interconnects

1. INTRODUCTION

The high bandwidth capacity and energy efficiency of optical communication depicts the supremacy of optics as competitive solutions for future interconnects in electronic systems [1]. Recent advances in the silicon photonics confirm the emergence of this technology [2, 3, 4]. Board-level optical interconnects are especially interesting for applications, as high performance computers or data centers, where the channel density and power consumption become critical. The lack of robust assembly routines compatible with standard assembly processes, e.g. surface mount technology (SMT), causes that optical boards are not yet widely applied. It is widely assumed that the passive alignment of optical components will enable a volume capable assembly process with an acceptable cost regime. In order to accommodate the assembly tolerances typical for SMT-processes dedicated transceivers with integrated micro-optics are needed to reach both low-loss redirection of the optical signals and coupling of active and passive optical components.

Different material platforms for integration of optics in electronic systems on board- and module-level have been proposed. Silicon [5], silica glass [6] and polymer [7, 8, 9] have been deployed for realization of planar lightwave circuits (PLC).

In this paper a combination of polymer and glass waveguides respectively for board- and module-level integration is proposed in order to exploit specific advantages of each solution. The development of planar polymeric waveguides on flexible substrate and glass interposer for optical transceiver is described. An approach for passive alignment and assembly of link components for board-level very-short range optical interconnects is discussed.

2. BOARD-LEVEL INTERCHIP OPTICAL LINK

2.1 Concept of on-board optical communication for high-performance computing

In this paper a chip-to-chip optical link based on planar polymeric multimode waveguides and glass-based optical transceiver is discussed. As the high bandwidth density of the optical links for the communication between computing nodes within a high-performance computer is required, a multichannel optical network system as shown in Figure 1 is targeted. In future system an electro/optical printed circuit board (E/O-PCB) with an array of computing nodes (e.g. 4x4 as depicted in Figure 1 (a)) is expected. In order to achieve high cumulated data rates needed for exascale systems [11, 12] a highly-parallel optical link connecting computing nodes is investigated. In this work optical links are based on array of polymer waveguides integrated into the PCB. In Figure 1 (b) a schematic view of 2D array of optical I/O ports at the bottom of each computing node is shown, where the light is coupled into the PCB-waveguides using glass-based out-

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of-plane optics with 90° micro-mirrors. Figure 1 (c) depicts the packaging concept of an optical computing node in a HPC system, which integrates optical transceiver and computing elements (processor and memory) for performance enhancement. The optical transceiver features vertical hybrid integration of driver and receiver ICs, (SiGe or CMOS), optoelectronic ICs (III-V E/O converters or Si-photonics circuits) and glass-based coupling optics using 3D wafer integration, through silicon vias (TSVs) and flip-chip assembly in order to shorten the electrical interconnects and hence lowering the power consumption and increasing performance at high data rates.

Figure 1. Packaging concept of an optical interchip multichannel link in a HPC system: a) optical network connecting computing nodes on the PCB, b) bottom view of package showing optical transceiver with shifted micro-mirror array and c) schematic view of node optical transceiver

2.2 Fabrication of optical waveguides on flexible substrate

The planar polymer single mode [13] and multimode [8] optical waveguides are often discussed as very promising approach for optically functionalized hybrid electro/optical printed circuit boards (E/O-PCB). In this work multimode waveguides are discussed since relative large core dimensions (30 – 50 μm) lead to relaxed alignment tolerances, which are essential for incorporation of passive alignment scheme. The planar strip waveguides were fabricated usingOrmocere® inorganic-organic hybrid material, which features high transparency in a wide spectral transmission range (from visual range 600 – 900 nm up to telecommunication wavelengths 1310 nm / 1550 nm), high thermal stability and excellent structuring properties. This material can be structured using UV-photolithography (negative type). In this work mask-based UV-photolithography was applied for the structuring of core and cladding material [14]. In preliminary work low optical attenuation below 0.05 dB/cm have been proved [15].

The concept considers structuring of polymeric waveguides on flexible substrate for realization of an optical overlay on the top of electrical PCB. This approach features an increased yield and simplified testability in comparison to inlay technologies because of separate fabrication of optical and electrical PCB layer. Additionally using flexible substrate mechanical decoupling of optical and electrical layers is applied, which enhance the reliability at alignment-sensitive coupling interfaces. In order to enable structuring of waveguides in subsequent photolithography processing steps the flexible substrate has to be temporary bonded on carrier a rigid substrate. These criteria have been used for selection of

suitable substrate material [16]. Because of excellent thermal and chemical stability of the temporary bond, for this work heat-stabilized polyethylene-naphthalate (PEN - Teonex® Q65H) foil has been used. This foil is pretreated on one side of the foil and therefore can be laminated on a carrier wafer. The used foil has a thickness of 50 μm and features a smooth surface ($R_a = 0.7 \text{ nm}$) and high transparency making it suitable for optical application. After the temporary bonding of the PEN-foil the cladding and core layers were subsequently deposited on 6" carrier wafer with flexible substrate using spin coating. The core pattern was UV-structured by a proximity exposure followed by a post exposure bake and an immersion developing step. Finally, the covering of the core with the upper cladding polymer and hard baking of the layer sandwich were performed. In Figure 2 (a) an optical layer on a PEN-flexible substrate temporarily bonded on Si-carrier wafer is shown.

Figure 2. Overlay optical waveguides: a) structured on PEN-flexible substrate temporarily bonded on Si-wafer and b) cross section of waveguide array with core width of 40 μm

This photograph shows in-/out-coupling end faces of waveguides with landing areas for transceiver glass-based modules. Three multichannel link arrays (3-, 12- and 40-channel link) with 250 μm pitch have been realized for a coupling with different transceiver modules for basic optical characterization and transmission tests. For the optical coupling tolerance analysis straight waveguides including 8-channel waveguide arrays with the variation of its core width from 30 μm to 50 μm and line/space ratio of 0.5 for each waveguide width have been used. An example cross section of the waveguide array with a core width of 40 μm is depicted in Figure 2 (b).

The commercially availableOrmocere®-material combination for the waveguide fabrication (Ormoclad and Ormocore) has an index contrast of $\Delta = 0.014$ ($n_{\text{core}} = 1,550$ and $n_{\text{cladding}} = 1,528$) at the target wavelength of $\lambda = 850 \text{ nm}$ which yields a numerical aperture of $\text{NA} = 0.26$. This corresponds to an acceptance angle of 15.3° . Mixing of both materials enables tuning of the numerical aperture NA in the range from 0.26 down to 0.14 (for a detailed description of NA tuning refer to [15]). Waveguide samples with different NA have been used in this work for tolerance analysis in section 3.2.

2.3 Glass interposer for optical transceiver

In this work the transceiver package for optical communication between the computing nodes is based on silica glass since a wavelength range from approx. 800 nm up to 1600 nm is targeted. In comparison to waveguide integration on silicon, glass enables a wider range of wavelength from UV to near IR. As depicted in Figure 1 (c) the glass interposer integrates three functions. The integrated optical waveguides realize pitch conversion from a 1D I/O array defined by polymer waveguides to a 2D array of optoelectronic converters and guide the optical signal to micro-mirrors. These mirrors perform 90° redirection of the light from the horizontal PCB-plane in order to couple the signal from/into vertical lasers/photodetectors (out-of-plane coupling optics). Additionally the interposer includes a metallization for the assembly of electrical components (optoelectronic and electronic transceiver ICs) on the top of the interposer. In this way optical transceiver subassemblies can be manufactured on wafer-level using precise enabled processing suitable for high-volume production.

The integrated waveguides are embedded in glass by an E-field assisted ion-exchange process using two-step diffusion. In the first step, ions from a molten AgNO_3 source are diffused into the surface of the glass, while the second diffusion process from a NaNO_3 source is performed in order to bury the waveguides under the glass surface and to give them a circular shape. Figure 3 (a) shows a cross section of the glass-integrated multimode waveguides with an almost circular core shape of approx. 50 μm x 60 μm dimensions and gradient index profile. The micro-mirrors for out-of-plane coupling have been fabricated by wafer dicing (sawing). Since for this work 90° -light redirection is aimed, a dicing blade with

double-side 45° profile was chosen. In Figure 3 (b) a profile of a diced mirror trench with a goal depth of 50 μm is shown. The profile characterization using confocal and optical microscopy shows that the geometrical dimensions of the realized mirror approximate the desired values regarding the trench depth and angle. The roughness of mirror surface of $R_a = 51$ nm (using 2000 mesh blade) confirms an optical surface quality ($R_a < 0.1 \lambda$).

Figure 3. Glass interposer with embedded waveguides and micro-mirror: a) cross section of glass-integrated waveguides, b) confocal profile measurement result of micro-mirror for out-of-plane coupling realized by wafer sawing.

After mirror processing the bottom surface of interposer is metallized with 200 nm thick Al layer. This additional metallization enables fully under-filling or an encapsulation of the glass interposer for enhanced reliability of final assembly. For the coupling scheme with top mounted E/O devices as depicted in Figure 1 (c) substrate thinning from a standard thickness of 1,5mm to a thickness of below 150 μm is required in order to achieve low coupling losses without using additional collimation optics. Result of the thinning to a thickness of approx. 130 μm using mechanical grinding and polishing processes can be seen in Figure 3 (a). The next fabrication step of interposer realization includes the definition of metallization on the thinned top glass surface. The structuring of the metallization has been performed using a lift-off photolithographic process. Precise definition of pads for assembly of E/O devices is guaranteed, because of a high accuracy of this wafer-level process (mask exposure of lift-off resist using mask aligner).

Figure 4. Top view of glass interposer after fabrication a) transmitter Tx module, b) receiver Rx module and c) detailed picture of pad area for placement of active optoelectronic converter (VCSEL)

Figure 4 shows the top view of the glass interposer for the transmitter Tx (a) and receiver Rx (b) module after fabrication. Below the top metallization the embedded waveguides (straight vertical lines), the mirror Al metallization (light background) and the diced mirror (black horizontal strip) can be shown. In Figure 4 (c) a detailed picture of the pad area for the placement of active optoelectronic converter (VCSEL) is depicted, showing an illuminated mirror slope with out-coupled and redirected light from the waveguide. The last processing step includes singularization of the transceiver interposer.

3. OPTICAL TRANSCEIVER SUBASSEMBLY

3.1 Optical coupling scheme

For board-level interconnects the crucial point for the assembly of components in optical transceivers is the optical coupling scheme, which can support low-loss, robust and SMT-compatible assembly routines. The main goal is to ensure relaxed assembly tolerances, which mainly determine the overall economic feasibility of photonic system integration. In this work a simplified optoelectronic subassembly as depicted in Figure 5 (a) is considered.

Figure 5. a) Optoelectronic subassembly, a) schematic illustration of height alignment between glass and polymer waveguides and b) detail picture of in-coupling interface of polymeric waveguides

This optical coupling scheme has two coupling interfaces at each transceiver. The first interface represents the E/O-chip-to-glass coupling. Here, a flip-chip (FC) assembly of E/O-devices is deployed as a precise and surface mount compatible process. FC-assembly features low-parasitic interconnects, which makes this contacting method especially suitable for high bandwidth electrical interconnects. The second coupling interface is the waveguide coupling between glass and polymer waveguides. In order to overlap the optical axes of both waveguides a height alignment is realized by using landing pads as spacers. The schematic cross section of this coupling interface can be seen in the Figure 5 (b) illustrating that a good control of the thickness difference Δt between upper surface of SU-8 spacers and under-cladding material defines the accuracy of the alignment in z-direction. Figure 5 (c) shows a detail picture of the realized in-coupling interface of the polymeric waveguides. Assuming the burial depth of the glass waveguides of approx. $25\ \mu\text{m}$ (see Figure 3 (a)) and $(30 \times 30)\ \mu\text{m}$ cross sectional dimensions of the polymer waveguide, a thickness difference Δt of $10\ \mu\text{m}$ is aimed. To verify the calculated goal geometry confocal topography measurements have been performed.

3.2 Optical characterization - coupling tolerances

The optical characterization in regard to the optical coupling between link components defines the tolerances for the alignment process. This optical analysis is based on measurements of spatial coupling characteristics. For this purpose a dedicated modular set-up has been used. Figure 6 (a) shows a photograph of the experimental set-up for observation of out-of-plane coupling optics.

Figure 6. a) Photograph of measurement set-up, b) test glass optics sample and c) wire bonded VCSEL mounted on ceramic substrate for tolerance analysis

This set-up enables the adoption of its configuration for different measurement purposes. It consists of motorized translation stages with automated motion controlling (LabView), data acquisition (DAQ), vision systems and the measured DUT (Figure 6 (b) – out-of-plane coupling optics). Stepper motion motors, which drive the linear translation stages, allow for scanning measurement with a sub-micrometer resolution. For light detection a detecting fiber connected to an integrating sphere and a CCD-based beam profiler are used. The positioning of the optical parts is monitored with a camera-based vision system. The optical transmission measurement results strongly depend on the choice of the optical components for launching and detecting of the optical signal. In order to ensure realistic launching conditions a wire bonded VCSEL mounted on ceramic substrate has been used. Since the operating point of the laser has influence on the emitting characteristic an investigation on the influence of this parameter on the coupling tolerance has been performed.

Table 1. Comparison of lateral assembly tolerances in horizontal Δx and vertical Δy direction at 1st coupling interface for different laser currents at 1 dB-loss criteria.

I_{LD} [mA]	1 st coupling interface	
	Δx [μm]	Δy [μm]
1	64	30
2	82	50
4	86	52
6	84	52
8	82	48

In Figure 7 (a) the P-I-curve as well as the emitting beam for three different laser diode currents (1 mA, 2 mA and 6mA) are shown. For an increased current the beam profile changes from ring emission into an almost flat-hat beam profile at higher currents ($> 5\text{mA}$) takes place. This has an influence on the coupling tolerances at VCSEL to glass-PLC interface only at small currents near the lasing threshold as it can be seen in Figure 7(b). Table 1 summarizes the results of this tolerance investigation for a 1 dB-loss criteria.

Figure 7. Characterization of the laser source: a) influence of laser operating power on emitting characteristic and b) on coupling tolerances for glass out-of-plane optics (results of scanning tolerance measurement showing optical power transmission for different lateral displacement of VCSEL in front of a glass out-of-plane optics – 1 step = $2\mu\text{m}$).

Exemplary diagrams of assembly tolerances measurement for above mentioned currents are shown in Figure 8 (a). The geometrical and material parameters of the waveguides define the assembly tolerances for transceiver components. The analysis was performed for waveguide widths in the range of 30 μm to 50 μm and a NA variation of 0.14 up to 0.22. As to define the maximum allowable misalignment for the in-coupling interface (at Tx-side), the coupling losses are plotted in horizontal and vertical axis. The best coupling position corresponds to the maximum power transmission. Additionally, the influence of the axial displacement Δz on the coupling losses has been investigated for the out-coupling interface (at Rx-side). Exemplary diagrams of the assembly tolerances measurement for NA = 0.22 are shown in Figure 8 (b) and (c).

Figure 8. Results of assembly tolerances measurement for a) VCSEL to glass-PLC interface and for coupling between polymer (NA = 0.22) and glass waveguides for different core width b) for in-coupling and b) out-coupling interface.

The graph also contains the two tolerance criteria of 1 dB- and 3 dB-loss, which are used for the definition of tolerance thresholds for the alignment of the coupling partners. This procedure has been repeated for all variations of waveguide widths and numerical apertures. The respective horizontal Δx and vertical Δy misalignment tolerances at 1 dB-loss for all mentioned combinations are summarized in Table 2

Table 2. Comparison of lateral assembly tolerances for 1 dB-loss criteria.

NA [-]	width [μm]	in-coupling (Tx)		out-coupling (Rx)		
		Δx [μm]	Δy [μm]	Δx [μm]	Δy [μm]	Δz [μm]
0.14	30	23	12	19	22	211
	40	31	22	20	24	239
	50	43	19	22	27	220
0.18	30	31	18	20	24	240
	40	38	25	19	21	206
	50	47	24	25	30	317
0.22	30	32	17	20	25	255
	40	41	25	22	24	252
	50	43	19	21	26	246

The analysis of these results proves the expected increase of allowable tolerances with increased polymer waveguide’s width for the in-coupling interface. No significant influence of the refractive index difference on misalignment can be observed.

3.1 Assembly of transceiver components

For the realization of low-loss interconnects depicted in Figure 5 (a) two tolerance-critical assembly processes have to be performed. For the assembly of E/O devices thermosonic FC-bonding using an equipment (FINEPLACER® lambda) with high placement accuracy (down to $\pm 0.5 \mu\text{m}$) and a special tool for the handling of small components has been implemented (Figure 9 (a)). This FC-method features a flux-free assembly process, which is particularly important for optical devices in order to ensure clean optical coupling surfaces. The electrical interconnect is based on Au stud bumps

bonded on the E/O device. The E/O converters are single channel top-emitting VCSELs and GaAs PDs with chip areas of $(250 \times 250) \mu\text{m}^2$ and with $50 \mu\text{m}$ diameter pad openings. In order to optimize the bonding process of E/O-converters on the glass a test assembly with $(350 \times 250) \mu\text{m}^2$ VCSEL-chips and glass substrates without integrated WGs have been performed. In Figure 9 (b) results of these tests for optimized process parameters ($T = 120^\circ\text{C}$, $F = 1 \text{ N}$ (3 bumps), $P_{\text{US}} = 1 \text{ W}$ and $t_{\text{puls}} = 500 \text{ ms}$) are depicted.

Figure 9. Results of test assembly of VCSEL on glass using thermosonic FC-bonding: a) screenshot of controlling interface during FC-processing and b)

The second interface is the coupling between glass and polymer waveguides. In order to overlap the optical axes of both waveguides a height alignment is realized by using landing pads as spacers as shown in Figure 5 (b). The alignment process in the horizontal plane was realized by placing the glass optics using the die bonder (FINEPLACER®). A self-developed assembly tool has been used, which can be seen in Figure 10 (a), was used to place the interposer. This combines an optical in-/out-coupling fiber array and a vacuum applying nozzle for simultaneous placing and semi-active alignment of the glass interposer on the optical overlay with polymer waveguides. By overlapping the view of the flexible substrate and the bottom of the glass interposer, the core structures on both substrates can be aligned (see Figure 10 (b)). Figure 10 (c) shows the coupling interface between waveguides after placement and adhesive bonding of glass interposer using UV-curable adhesive.

Figure 10. Assembly of the glass interposer on the flexible substrate: a) self-developed assembly tool with combined optical and vacuum applying nozzle, b) view from the vision system of the die bonder showing the horizontal alignment procedure and c) coupling interface between the waveguides after placement.

This adhesive acts as mode matching material at the coupling interface between the polymer and glass waveguides in order to lower the reflection losses.

4. CONCLUSIONS

The paper presents an approach of multichannel optical network for the communication between computing nodes within a high-performance computer system. A packaging concept for fabrication and assembly of link components, which enables passive alignment have been described. A hybrid optoelectronic subassembly, which combines polymer and

glass waveguides respectively for board- and module-level integration is proposed in order to exploit specific advantages of both solution. Glass-PLC enables highly integrated and rugged optic solutions and wafer-level fabrication, which offers a high potential for cost-saving using high volume manufacturing. The used wafer dicing for micro-mirror features an easy and quick process, but it enables only the realization of straight cuts - no possibility for selective mirror fabrication as targeted for future work. Currently a laser ablation is evaluated for selective mirror fabrication. Basing on experimental optical characterization coupling tolerances for assembly of two main components – optoelectronic converters and glass interposer – revealed in relaxed misalignment tolerances of $> \pm 10 \mu\text{m}$, which can be assured with standard placement machines (FC-bonders or pick-and-place machines). Described technological platform is suitable for additional integration of another link components (driving/amplifier chips, electronic chips for digital signal processing, e.g. FBGAs and processor/memory chips) using 3D-stacking, which enhances the performance of the package by shortening the electrical interconnects. In the future work, we will evaluate the performance of the complete link by optical characterization, transmission tests and reliability analysis.

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