A Fast Switchable and Band-Tunable 5-7.5 GHz LNA in 45 nm CMOS SOI Technology for Multi-Standard Wake-up Radios

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Abstract—This work presents design and full implementation of a fast switchable and band-tunable 5-7.5 GHz low noise amplifier (LNA) in a 45 nm CMOS SOI technology. The target application are wake-up receivers that employ aggressive duty cycling. Based on a cascode topology, the LNA utilizes a transformer for its 50Ω input matching as well as a balun with a capacitor bank to realize 8 digitally selectable bands. According to measurement results, the fabricated LNA exhibits a voltage gain of 18-21 dB while drawing a current of merely 2.2 mA from a 1 V supply. At all the 8 bands from 5 to 7.5 GHz, the input reflection coefficient lies below -8 dB, and the noise figure ranges from 7.8 to 6.2 dB. The LNA is able to settle in less than 9.5 ns until the output signal reaches 90 % of its steady state amplitude.

Index Terms—Low noise amplifier, wake-up receiver, 45 nm CMOS SOI, tunable circuit, fast switching

I. INTRODUCTION

Energy availability is a major constraint in modern wireless sensor networks (WSN). Since radios are the most power-hungry components of a WSN, reduction of their power consumption can contribute to a dramatic decrease of the energy loss. One effective technique to reduce the radio's energy consumption is to use an ultra-low power wake-up receiver (WuRX) that detects short wake-up signals on its communication channel and wake up the main radio when the signals arrive. Otherwise, the main radio sleeps and consumes zero power. The WuRX's ultra-low power consumption is realized by aggressive duty cycling with a duty cycle $< 0.1\%$ [1].

Our project aims to design and implement a multi-standard WuRX between 5 to 7.5 GHz. Fig. 1 illustrates the WuRX's basic structure. The aggressive duty cycling used requires the WuRX's each component to be turned on/off and to settle within a small on-time. Here the first step undertaken which will be presented in this work is design and implementation of

Fig. 1. Simplified block diagram of the wake-up receiver

Fig. 2. Simplified schematic view of the designed LNA

an LNA for the WuRX. According to design specifications, the LNA should operate between 5 to 7.5 GHz with a low noise figure (NF) < 7 dB, a low DC power (P_{DC}) < 2.5 mW and a high voltage gain (G_V) > 18 dB. Here, since settling time (T_S) determines the on-time of the LNA and thus the duty cycle, a short T_S of < 15 ns is required for this work.

II. LNA DESIGN

Shown in Fig. 2, based on a single-stage cascode circuit, the designed LNA contains a transformer-based input matching network, an on/off switching unit and a LC-tank balun as its band selection unit. Table I summarizes the main component values for the LNA in Fig. 2. To achieve an insight into the LNA's work principle at its on-state, we first build a simplified small signal equivalent circuit (SSEC), as is shown in Fig. 3.

A. Input Matching

The input matching network is comprised by the capacitor C_1 and the transformer that consists of the coils L_1 and L_2 .

TABLE I
SUMMARY OF MAIN COMPONENT VALUES FOR THE LNA

Transistor	$N_{1,2}$	N_3	$N_{4,5}$	$N_{5,6}$	N_7	$P_{1,2}$
W/L/ μm	15/0.04	1.5/0.04	10/0.04	15/0.04	26/0.04	20/0.04
Inductor	L_1	L_2	M_{12}	L_3	L_4	M_{34}
/nH	2 - 2.6	0.8 - 1.2	0.75	1 - 1.3	1 - 1.3	0.8
Capacitor	C_1	C_2	C_3	C_4	C_5	C_6
/fF	530	480	50	60	120	210

Fig. 3. Simplified SSEC of the LNA at its on-state

This network not only provides the LNA with a single-ended 50Ω matching to the antenna, but also avoids large off-chip inductors. The decoupling capacitor C_2 is used to isolate the DC biasing voltage of $V_{DD}/2$ generated by the nMOS transistor N_3 and the resistor R_1 of $1.25\text{ k}\Omega$.

Based on the SSEC in Fig. 3 and with an assumption that the drain-source resistance of $N_{1,2}$ (r_o) as well as the impedance of the resonating LC-tank (Z_{LC}) are large, so that they are here considered as open, the LNA's input impedance Z_{in} can be analytically expressed as the following:

$$Z_{in} = \frac{1}{sC_1} + \frac{s^2(L_1L_2 - M_{12}^2)(g_m + sC_{GS}) + sL_1}{s^2C_{GS}(L_1 + M_{12}) + s(L_2 + M_{12})(g_m + sC_{GS}) + 1} \quad (1)$$

Here we obtain a good agreement for the magnitude of Z_{in} (Z_{in}) simulated with the same parameter values using Eq. (1), the SSEC in Fig. 3 and the schematic in Fig. 2 respectively, as is shown in Fig. 4. Then, after a careful analysis of the Z_{in} 's expression similar to the means in [2] and [3], we come to conclude, to obtain a real part of 50Ω for Z_{in} , values of L_1 and L_2 must fulfill the condition $L_1 > L_2$. Moreover, C_1 is needed to compensate imaginary part of Z_{in} to zero. Note although the input matching network used here is originally exploited for the narrow-band matching in [2] and [3], according to our simulation results, we find out it is applicable for our wide-band matching within the band from 5 to 7.5 GHz if the matching point ($S_{11,min}$) is set to around 5.8 GHz with the value smaller than -18 dB . Furthermore, many efforts were laid to design the transformer for a relatively large and constant Q factor and mutual inductance M_{12} of both the coils L_1 and L_2 . Finally, the post-layout simulated S_{11} is demonstrated in Fig. 5, which shows a good matching in the 8 required bands.

B. Band Selection

The tunable LC-tank load composed of the coils $L_{3,4}$ and the capacitor bank $C_{3,4,5,6}$ forms the LNA's differential output. To achieve a direct understanding on how the LC-tank impacts the LNA's band without much analysis complexity, here we ignore the input matching network, and the LNA's voltage gain $G_v = (V_{OP} - V_{ON})/V_{IN}$ can be simplified into:

$$G_v = 2g_m^2(r_o || \frac{r_o + Z_{LC}}{1 + g_m r_o})(r_o || Z_{LC}) \quad (2)$$

Fig. 4. Comparison of Z_{in} and G_v simulated with the same parameter values using schematic in Fig. 2, SSEC in Fig. 3 and Eq. (1) to (4), respectively.

Eq. (2) reveals a band-pass characteristic of the LNA due to the proposed LC-tank, which is essential to our need. Meanwhile, from the SSEC of the tunable LC-tank also shown in Fig. 3, we derived the analytical expression for Z_{LC} . When the LC-tank resonates, we obtain the resonance frequency f_0 from the condition $\text{Im}(Z_{LC}) = 0$:

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{1}{(L_3 + L_4 + 2M_{34})C_D} \left(1 - \frac{C_D(R_3 + R_4)^2}{L_3 + L_4 + 2M_{34}}\right)} \quad (3)$$

where C_D , $L_{3,4}$, M_{34} and $R_{3,4}$ represent the capacitance of the LC-tank, the self-inductance, mutual inductance and parasitic resistance of the two coils that form the balun. In order to change f_0 and thus have different bands, we build the capacitor bank composed by $C_{3,4,5,6}$ to digitally tune C_D with:

$$C_D = C_L + C_3 + \frac{1}{2}(V_A C_4 + V_B C_5 + V_C C_6) \quad (4)$$

where $V_{A,B,C}$ are digital signals and can be either 1 or 0, thus providing the LNA with 8 selectable pass bands. Here an additional parameter C_L with a value of 50 fF is used to model the impedance of the mixer's RF port. Meanwhile, a center-tapped octagon symmetrical differential inductor is implemented to realize the inductances $L_{3,4}$ and mutual inductance M_{34} . Finally, values of $C_{3,4,5,6}$ are chosen, so that the -3 dB bandwidth of every band can cover each other and that over the whole band of 5-9 GHz, G_v can be $> 20\text{ dB}$.

Fig. 5. Post-layout simulated LNA's G_v and S_{11}

To proof the correctness of Eq. (2) to (4), we also compared G_V obtained using these equations, the SSEC in Fig. 3, and the schematic in Fig. 2, respectively, which is shown in Fig. 4. Finally, Fig. 5 plots the post-layout simulated 8 G_V -versus-frequency relations.

C. On/Off Switching

The off and on switching of the LNA is realized by the MOS transistors $N_{4,5}$ and $P_{1,2}$. In the off-switching case, a high level of $\bar{V}_{EN}$ turns $N_{4,5}$ on and $P_{1,2}$ off. Thus, the gate potential of $N_{1,2}$ are pulled down to ground, turning them completely off. Meanwhile, P_1 cuts off the current flowing from V_{DD} to ground. After the off-switching, the LNA sleeps. In the on-switching case, a low level of $\bar{V}_{EN}$ switches $N_{4,5}$ off and turns $P_{1,2}$ on. Therefore, the bias voltage for N_1 generated by R_2 and N_3 , namely $V_{DD}/2$, as well as the bias voltage for N_2 , namely V_{DD} , are provided, which wakes up the LNA.

The settling time of the LNA depends mainly on how fast the bias voltages for $N_{1,2}$ can be fully loaded to their gates. As C_2 is connected to the gate of N_1 , the time to charge C_2 , reflected by the time constant factor $\tau = R_2 C_2$, dominates the settling time of the whole LNA. However, both R_2 and C_2 cannot be arbitrarily small, since they have a direct influence on the input matching, G_V and NF. Here, a trade-off with the result $R_2 = 7 \text{ k}\Omega$ and $C_2 = 0.48 \text{ pF}$ has been made so that the LNA can have a fast settling time and relatively high gain and a moderate NF.

In addition, we connect a large capacitor C_7 of 4 pF parallel to R_1 of 1.25 k Ω . C_7 stores the charge from V_{DD} in the sleep mode and, as the on-switching starts, it holds the gate potential of N_3 shortly to V_{DD} . This accelerates the on-switching of P_1 and N_3 , thus enhancing the building up of the charging path for C_2 . According to simulation results, the LNA's on-switching time of can be reduced by 2 ns thanks to C_7 .

D. Output Buffer

For the purpose of the characterization of the LNA, an output buffer that consists of two cascaded differential pairs is designed which mimics the 50 fF input impedance of the mixer, and also offers a 50 Ω output for 50 Ω input measurement tools. According to simulation results, this buffer that draws a DC current of 21 mA from another supply ($V_{CC} = 1.6 \text{ V}$) has a voltage gain of 0 dB at the band from 5 to 10 GHz.

III. EXPERIMENTAL RESULTS

Fig. 6 shows the photograph of the LNA together with its output buffer manufactured in the Globalfoundries' 45 nm CMOS SOI technology with a metal stack option of 11 metal layers. The size of the chip core without pads and wiring is 220 $\mu\text{m} \times 420 \mu\text{m}$. The LNA excluding the output buffer consumes 2.2 mA from a 1 V supply.

A. Characterization Of Wake-up Time

Fig. 7 shows the measurement setup to characterize the time response of the LNA. We used a signal generator Agilent E8257D PSG 60 GHz to output RF signals for the LNA's RF

Fig. 6. Chip photograph of the fabricated LNA

input V_{IN} , and another signal generator Keysight 33600A to output a square wave which modeled the on/off signal for the LNA. With a power divider and two identical cables, the generated square wave was split into two equal signals. One was applied to the LNA's negative enable pin $\bar{V}_{EN}$, while the other one triggered a sampling oscilloscope Tektronix DSA8300. Channel C1, C2 and C3 of the oscilloscope measured and saved the data of $\bar{V}_{EN}$, V_{ON} and V_{OP} .

For this test, a 20 MHz square wave was sent to the LNA's input $\bar{V}_{EN}$, and a 5.5 GHz sine wave with a power of -35 dBm to V_{IN} . Fig. 8 shows the time trace of the LNA's $\bar{V}_{EN}$ and its differential output $V_{ON} - V_{OP}$ registered in the oscilloscope. To make a fair comparison, here we use the definition of the term wake-up time in [2] for our characterization, which is the time from the moment when $\bar{V}_{EN}$ is applied until that when the RF output reaches 90 % of its steady state amplitude. From Fig. 8, a time slot of 12 ns can be observed, which, however, contains the delay time the LNA's output signal took to travel from the LNA's output pin to the oscilloscope. Since the distance between the LNA's output to the chip's pads V_{ON} and V_{OP} is of around 600 μm , we only measured and excluded the delay caused by the cable between the chip's pads and the oscilloscope, which is 2.5 ns. Thus, a wake-up time of 9.5 ns for the LNA is obtained.

B. Characterization Of S-Parameter and Noise Figure

With a 4-port vector analyzer Rohde&Schwarz ZVA-67 at -30 dBm input power, we obtained the S-parameters for the LNA's input V_{IN} and outputs V_{ON} and V_{OP} . The LNA's voltage gain G_V can be derived from the relation $G_V = S_{31}$ (or S_{21}) +

Fig. 7. Measurement setup to characterize the LNA's transient behavior

Fig. 8. Measured LNA output with $\bar{V}_{EN}$ being applied

6 dB. Fig. 9 shows the measured S_{11} and G_V of the LNA. It can be seen that the measured S_{11} is smaller than -8 dB between 5 to 7.5 GHz. Although it is 4 dB higher than its simulated counterpart, it satisfies the design specification. Still, despite of a decrease of G_V by approximately 4 dB at all the eight bands compared to the simulated results, $G_{V,max}$ at the center frequency of each band is greater than 18 dB which meets the specification. At last, we measured the NF of the LNA using a signal analyzer Rhode&Schwarz FSW-67. Fig. 10 shows the results. A minimal NF at the center frequency of each band ranges from 7.8 to 6.2 dB.

IV. CONCLUSION

A cascode LNA using an integrated transformer as its input matching network as well as an integrated LC balun as its

Fig. 9. Measured LNA's G_V and S_{11}

Fig. 10. Measured LNA's noise figure

band tuning unit was fully implemented in a 45 nm CMOS SOI technology. A trade-off between power consumption, wake-up time, gain, band and noise figure was made with a result of a very fast settling time, a high gain and a moderate noise figure. The performance of the LNA and comparison with prior works are summarized in Table II. In general, this LNA is competitive to the state-of-the-art LNAs. Specifically, this LNA achieves a remarkably short settling time of < 9.5 ns. Although the LNA in [4] has the fastest on-switching time of 1.3 ns ever reported in literature, during sleep mode, it still consumes a power of 0.8 mW. This is a critical drawback making the LNA in [4] neither applicable for WuRXs, nor comparable to this work.

With an on-time of 20 ns and at the mode of the aggressive duty cycling with a duty cycle of 0.1%, which corresponds to a data rate of 10 kbit/s, the LNA can achieve an ultra-low power consumption of $2.2 \mu\text{W}$.

TABLE II
COMPARISON WITH STATE OF THE ART

	This work	[2]	[3]	[4]	[5]
Technology	45 nm CMOS SOI	130 nm BiCMOS	28 nm CMOS	130 nm CMOS	45 nm CMOS
Settling Time/ns	9.5	32	-	1.3	-
P_{DC} / mW	2.2	1.85	5	18	5.3
Power / μW $T_D=0.1\%$	2.2	1.85	5000	817	5300
f / GHz	5-7.5	2.4	2.0	1-10.6	2.8-10
G_V / dB	18-21	20	24	16	14.2
NF/dB	6.2-7.8	3.3	1.9	3.9	5.1-6.3
S_{11} / dB	-8	-18	-22	-	-10

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