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Low Power Laser Driver Design in 28 nm CMOS for on-Chip and Chip-to-Chip Optical Interconnect

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ABSTRACT

This paper discusses the challenges and the trade-offs in the design of laser drivers for very-short distance optical communications. A prototype integrated circuit is designed and fabricated in 28 nm super-low-power CMOS technology. The power consumption of the transmitter is 17.2 mW excluding the VCSEL that in our test has a DC power consumption of 10 mW. The active area of the driver is only 0.0045 mm². The driver can achieve an error-free (BER < 10⁻¹²) electrical data-rate of 25 Gbit/s using a pseudo random bit sequence of 2⁷ - 1. When the driver is connected to the VCSEL module an open optical eye is reported at 15 Gbit/s. In the tested bias point the VCSEL module has a measured bandwidth of 10.7 GHz.

Keywords: Laser driver, VCSEL driver, VCSEL, CMOS integrated circuit

1. INTRODUCTION

With the development of cloud services, both storage and heavy computation continue to move into warehouse-scale datacenters. The datacenters are growing reaching dimensions in the order of 30 000 m² consuming megawatts of power.¹ Optical connections are since the 1980s widely used in high speed long distance communications. With the technology development the distance at which the use of optical connections instead of copper is beneficial, continuously decreases.² Moreover the silicon large scale integration (Si-LSI) is facing challenges due to the limited bandwidth caused by long electrical lines with high RC constant that leads to the large delay of global and local (on-chip) electrical interconnects.^{2,3} According to the IBM roadmap, nowadays optical connections are used for distances in the range of few centimeters (on-module) and in 2020 optical network on-chip are expected to replace copper for distances of few millimeters in intra-package and intra-chip optical interconnects.

This paper proposes the use of directly-modulated vertical-cavity surface-emitting lasers (VCSEL) for very short distances (< 1 m) optical connections. VCSEL diodes are widely used in optical links up to distances of hundreds meters. The main challenge of adopting this technology in very-short distance connection is the power consumption and hardware costs of the common-mode logic CML circuitry necessary for optical transceivers. These circuits include full-speed multiplexer and demultiplexer, retiming circuits, laser driver and transimpedance amplifier.⁴ It has been demonstrated that a single direct-modulated VCSEL-based link can operate error-free (BER < 10⁻¹²) at data-rate up to 71 Gbit/s. The transceiver is realized in a 130 nm BiCMOS SiGe process and uses feed-forward equalization in order to overcome the bottleneck given by the limited VCSEL bandwidth that is 26 GHz.⁵ Unfortunately such high speed comes at a cost of high power consumption. The transceiver⁵ which includes laser driver, transimpedance and limiting amplifier, has a power consumption of 1.8 W. Adopting bandwidth extension techniques such as feed forward equalization and decision feedback equalizer when the data-rate is higher than 25 Gbit/s results in a power hungry transceiver.⁶ Moreover, the circuit in⁵ is realized in a SiGe process. As the total cost of the final product is influenced by the material costs, the packaging and the testing, using a SiGe process the transceiver is going to be connected to the CMOS logic core increasing both material costs and packaging costs. In order to keep the costs low, the transceiver circuitry should be designed in the same technology of the CMOS digital core. This paper presents one example of laser driver highlighting the design challenges in using a highly scaled, low power, CMOS technology.

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2. DRIVER-TO-VCSEL INTERFACE

In the design of CML CMOS laser drivers up to 25 Gbit/s one of the major challenges is the driver-to-VCSEL interface. The driver needs to provide the bias current to the VCSEL as well as the modulation current. If the current in the VCSEL is less than the threshold, the optical power is small so the optical eye closes because the device does not operate as laser.⁴ The VCSEL can be biased as a common cathode or common anode. It is not always possible to choose the bias type of the VCSEL since it is already defined during the VCSEL design. Figure. 1 shows a comparison of different driver-to-VCSEL interface topologies for common anode (a,b,c) and common cathode (d,e,f) VCSELs. The last stage of the laser driver needs to provide modulation and bias current

Figure 1. Driver-to-VCSEL interface topologies. (a),⁷ (b)⁸ and (c)⁹ for common anode VCSELs and (d),¹⁰ (e)⁸ and (f) for common cathode VCSELs. I_{mod} is the modulation current and I_b is the bias current provided from the driver to the VCSEL.

to the VCSEL. The VCSEL can be represented by the equivalent circuit reported in Fig. 2. The impedance of high speed commercial VCSELs is in the order of 50 - 100 Ω .^{11,12} The impedance matching between the driver and the VCSEL becomes more critical as the data-rate increases. The physical distance between the VCSEL and driver plays an important role in the electrical transmission between driver and VCSEL. It is therefore important that the output impedance of the driver is similar to the VCSEL impedance. In Fig. 1 three different circuit topologies are proposed. In Fig. 1(a) and (d) the VCSEL is connected to the collector resistor R_{C2} of the differential amplifier. Since the drain source resistance of the transistor is high, it is easily possible to have a low impedance output choosing a low collector resistor R_{C2} . This characteristic makes this type of design suitable for high speed. The bandwidth of the differential amplifiers can be further increased using inductive peaking, emitter degeneration or negative miller compensation.¹³ The designs reported in Fig. 1(b) and (e) on one hand

Figure 2. VCSEL equivalent circuit. C_p and R_p are the pad parasitics, R_m is the mirror resistance and R_a , C_a are the equivalent circuit elements of the active region.

are not an optimum choice for very high speed since the driver has high output impedance. On the other hand they are more power efficient since the load of the transistor Q_{be} is only the laser and not the impedance of the laser in parallel to the collector resistance like in Fig. 1(a) and (d). In the designs of Fig. 1(c) and (f) the laser is connected to an inverter. If we consider this output circuit as a digital inverter with high impedance output the impedance matching between the laser and the circuit can create problems in this design. These problems can be solved if there is a dc current flowing through the transistor Q_{cf} , in this case the output impedance at the node X can be approximated with $1/g_{m-Q_{cf}}$ solving the mismatch problem.

Another challenge in the design of the common-cathode drivers is the output DC voltage. This voltage needs to match the V-I curve of the laser diode. Since the bias voltage of the laser often exceeds the breakdown voltage of the output transistor, the cathode of the VCSEL can be connected to a negative potential or the entire output stage can be placed in an independent well allowing high output DC voltage.⁷ The circuit proposed in this article uses the topology of Fig. 1(f) with the cathode of the VCSEL connected to a negative voltage since V_{DD} is 1.4 V and a higher voltage will increase the risk of transistor breakdown.

3. DRIVER IC

The proposed driver is realized in a 28 nm super-low power CMOS technology. The technology is usually used in the design of digital processors since the super-low power characteristic means that the transistors have a low leakage current. To design high-speed driver a high-performance RF version of the technology is beneficial but the integration of the driver with the digital circuitry is challenging or not possible.

The schematic of the driver is shown in Fig. 3. The proposed circuit topology is a four-stage differential-to-single-ended driver. Since the measurement equipment is matched to 50 Ω , between the input terminals $in+$ and $in-$ a parallel resistor of 125 Ω is added. The first differential amplifier has a negative feedback through 1 k Ω resistors. This feedback improves the input matching and provides the DC bias to the input transistors. It is therefore possible to use DC blocking capacitors in the measurement set-up as described in Section 4. In this driver design, the focus is on bandwidth, area and power consumption which trade-off with amplification and voltage swing. One technique that allows to increase the bandwidth is source degeneration in differential amplifiers.⁴ Using a capacitor C_S and a resistor R_S connected in parallel between the sources of the transistors in an ideal differential amplifier, the equivalent transconductance can be expressed as:

$$G_m = \frac{g_m}{1 + g_m \left(\frac{R_S}{2} \parallel \frac{1}{2sC_S} \right)} = \frac{g_m(1 + sR_SC_S)}{1 + g_mR_S/2 + sR_SC_S} \quad (1)$$

where g_m is the transistor transconductance. The equivalent transconductance G_m contains a zero at $1/(R_SC_S)$ and a pole at $(1 + g_mR_S/2)/(R_SC_S)$. Since the zero can cancel out the first pole of the differential amplifier, using this technique leads to a bandwidth increase by a factor f of $1 + g_mR_S/2$. The disadvantage of using this technique is the reduction of gain by the same factor f .⁴ A P-MOS transistor is used to realize the capacitor for the emitter degeneration. The W/L ratio for the P-MOS transistors is reported in Fig. 3. The bias current of

Figure 3. Schematic of the driver circuit. The capacitors are realized using P-MOS transistors with the reported W/L dimensions.

every differential amplifier I_{b1} , I_{b2} and I_{b3} is connected to a current mirror controlled using a single pad I_{bias} as it can be seen in Fig. 4.

The output stage is a push-pull topology.⁹ Two N-MOS transistors N1 and N2 are connected in a totem pole topology without level shifter.¹⁴ Both the output N-MOS transistors are biased in order to have a low output impedance and improve the output return losses and the driver-to-VCSEL reflections. In order to control the DC current through the transistors N1 and N2, a 53 Ω resistor is connected in the source of N2 as can be seen in Fig. 3. The output P-MOS transistor P1 is used in order to control the DC bias current of the VCSEL that can be connected in a common-cathode fashion using a negative potential.

4. MEASUREMENT AND SIMULATION RESULTS

Figure 4. Chip micrograph of the manufactured driver. The pitch between the RF and DC pads is 100 μm

The circuit of Fig. 3 was manufactured in a 28 nm super-low-power C-MOS technology. The fabricated chip micrograph can be seen in Fig. 4. The active area is only 0.0045 mm². This small area was achieved trading-off amplification with bandwidth using degeneration and avoiding the use of area inefficient passive inductors. The

circuit is supplied with a V_{DD} of 1.4 V. The schematic is carefully designed taking into account that V_{DD} , slightly higher than the drain-source breakdown voltage of the thin-oxide transistors, is never dropping on a single transistor. The pitch between the RF and DC pads is 100 μm and the chip area is pad-limited in order to enable on-chip testing with probes. In the left and the right hand side of Fig. 4 the 67 GHz GGB differential and single ended probes can be seen.

4.1 S-parameter measurements

The S-parameters are measured on-chip using a wafer probe and a 67 GHz Rohde&Schwarz vector network analyser (ZVA67). The parasitics of the measurement set-up (probes, cables, connectors, phase shifters etc.) are de-embedded using the short-open-load-through (SOLT) calibration. Since the differential GGB probe is equivalent to two single-ended GGB probes only one RF tip of the differential input probe was calibrated. The S-parameters (S_{21} and S_{22}) measured in this fashion for two samples are reported in Fig. 5. From the output

Figure 5. Chip micrograph of the manufactured driver.

return loss parameter S_{22} can be confirmed that the use of a biased inverter leads to a low output impedance. In fact the S_{22} parameter is below -15 dB for the whole bandwidth of interest that goes from DC to 15 GHz. The S_{21} single-ended gain is approximately -5 dB. The gain of this amplifier is traded-off with bandwidth and the 125 Ω matching-resistance connected between the inputs of the amplifier substantially reduces the gain. This resistor is only for measurement purposes, in case this driver is used after the multiplexer or the retimer circuit this resistor must be removed. The measured -3 dB bandwidth in the sample number 6 (meas.6 S_{21} in Fig. 4) is 14.33 GHz.

4.2 Large signal electrical measurements

A 55 GHz pseudo-random bit generator with a bit stream of 2^7-1 bits was used for the large signal measurement. The phase of the two inputs is aligned using broadband 67 GHz phase shifters. Unlike the S-parameter measurement, in the large signal measurement the parasitics of the measurement set-up directly deteriorate the eye diagram. In Fig. 6 the input and output eye diagrams at 10 Gbit/s and 25 Gbit/s are shown. It is visible that the input eye diagrams are already degraded from cable, connectors, DC blocking capacitors and phase shifters parasitics *. The output eye diagram at 25 Gbit/s is measured with an operation point where the driver consumes precisely 17.2 mW from a single 1.4 V source. It is possible to notice that the eye is still open at 25 Gbit/s achieving a BER $< 10^{-12}$. A larger input signal can improve the quality of the output eye due to saturation effect. Since one of the characteristic of this driver is the low power, the voltage swing of the input eye is kept low in order to allow a low power design of the block that will be placed before the driver.

* The probes are not included in the measurement of the input eye diagram

Figure 6. Single-ended input and output electrical eye diagram at 10 Gbit/s and 25 Gbit/s.

4.3 large signal optical measurements

In order to test the optical performance of the driver, a VCSEL module (Fig. 7) was attached to the output probe and biased to 5 mA using an external bias-T. The optical fiber was connected to a photodiode module (Fig. 7) that was biased by a bias-T as well. Instead of a transimpedance amplifier, a general measurement amplifier with 55 GHz bandwidth and 21 dB gain was connected to the photodiode. The high bandwidth of the amplifier

Figure 7. Optical test set-up including the VCSEL and the photodiode module.

and the oscilloscope (70 GHz) and the absence of a proper transimpedance amplifier lead to an increase in the noise of the received optical eye diagram. The VCSEL module biased at 5 mA has a measured bandwidth of 10.7 GHz. In Fig. 8 the received optical eyes at 10 Gbit/s and 15 Gbit/s are reported. After 15 Gbit/s the

limited bandwidth of the VCSEL, the noise in the received signal and the limited voltage swing of the driver do not allow an open eye.

Figure 8. Optical received eyes at 10 Gbit/s and 15 Gbit/s.

5. CONCLUSION

With the evolution of Internet and cloud services, there is an increase in the demands of bandwidth in short range optical connection within data-centres. As the distance between transmitter and receiver reduces, the optical connection should be made as cost-effective and energy-efficient as possible in order to compete with electrical connection. Hardware costs, packaging, testing and power consumption are the key factors. This paper proposes a driver that can be integrated directly with the digital processor since it is realized in 28 nm CMOS technology. Moreover the driver consumes only 17.2 mW of DC power and occupies 0.0045 mm². These characteristics makes the driver also suitable for parallel connection. The driver has an error-free (BER < 10⁻¹²), open electrical output eye at 25 Gbit/s. The connection to a VCSEL with 10.7 GHz of bandwidth results in an open optical eye at 15 Gbit/s. Table 1 compares this design with the state of the art of VCSEL drivers. Thanks to the use of source degeneration instead of inductive peaking, the proposed driver is the smallest in terms of area occupation, and compared to¹⁵ is the second best in terms of power consumption.

Table 1. Comparison with the state of the art VCSEL driver. * = common anode VCSEL diode

Ref.	Technology	data rate / Gbit/s	power FOM / mW/(Gbit/s)	Active area / mm ²
16*	90nm CMOS	16	3	0.017
this work	28nm CMOS	25	1.09	0.0045 mm ²
17	65nm CMOS	25	3	0.32
18*	90nm CMOS	25	1.45	0.014
7	90nm CMOS	25	2.4	0.006
15*	32nm SOI	35	0.856 @ 25 Gbit/s	n.a.
5	130nm BiCMOS	71	13.4	n.a.

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